TL494 Pulse-Width-Modulation Control Circuits

1 Features

- Complete PWM Power-Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance
- Circuit Architecture Allows Easy Synchronization

2 Applications

- Desktop PCs
- Microwave Ovens
- Power Supplies: AC/DC, Isolated, With or Without PFC
- Server PSUs
- Solar Micro-Inverters
- Washing Machines: Low-End and High-End
- E-Bikes
- Power: Telecom/Server AC/DC Supplies: Dual Controller: Analog
- Smoke Detectors
- Solar Power Inverters

3 Description

The TL494 device incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

The TL494 device contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from –0.3 V to V_{CC} – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 device provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

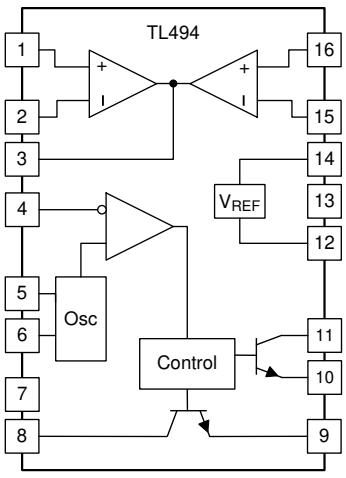
The TL494 device is characterized for operation from 0°C to 70°C. The TL494I device is characterized for operation from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE
TL494	SOIC (16)	9.90 mm × 3.91 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOP (16)	10.30 mm × 5.30 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2017) to Revision I (July 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision G (January 2015) to Revision H (March 2017)	Page
• Updated package illustration	1
• Corrected resistor polarity references in the *Current-Limiting Amplifier* section	15
• Updated Figure 12.	15

Changes from Revision F (January 2014) to Revision G (January 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, , *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision E (February 2005) to Revision F (January 2014)	Page
• Updated document to new TI data sheet format - no specification changes	1
• Removed *Ordering Information* table	1
• Added ESD warning	1

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6 Pin Configuration and Functions

D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

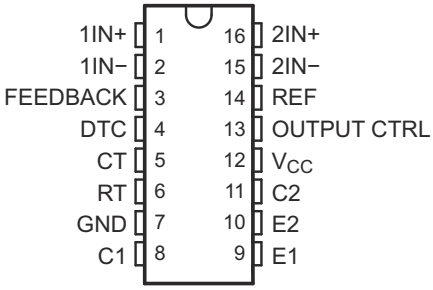


Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	1	I	Noninverting input to error amplifier 1
1IN-	2	I	Inverting input to error amplifier 1
2IN+	16	I	Noninverting input to error amplifier 2
2IN-	15	I	Inverting input to error amplifier 2
C1	8	O	Collector terminal of BJT output 1
C2	11	O	Collector terminal of BJT output 2
CT	5	—	Capacitor terminal used to set oscillator frequency
DTC	4	I	Dead-time control comparator input
E1	9	O	Emitter terminal of BJT output 1
E2	10	O	Emitter terminal of BJT output 2
FEEDBACK	3	I	Input pin for feedback
GND	7	—	Ground
OUTPUT CTRL	13	I	Selects single-ended/parallel output or push-pull operation
REF	14	O	5-V reference regulator output
RT	6	—	Resistor terminal used to set oscillator frequency
V_{CC}	12	—	Positive Supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		41	V
V_I	Amplifier input voltage		V_{CC} + 0.3	V
V_O	Collector output voltage		41	V
I_O	Collector output current		250	mA
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the network ground terminal.

7.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	200	

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		7	40	V
V_I	Amplifier input voltage		–0.3	V_{CC} – 2	V
V_O	Collector output voltage			40	V
	Collector output current (each transistor)			200	mA
	Current into feedback terminal			0.3	mA
f_{OSC}	Oscillator frequency		1	300	kHz
C_T	Timing capacitor		0.47	10000	nF
R_T	Timing resistor		1.8	500	kΩ
T_A	Operating free-air temperature	TL494C	0	70	°C
		TL494I	–40	85	

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TL494					UNIT
		D	DB	N	NS	PW	
$R_{\theta JA}$	Package thermal impedance(1) (2)	73	82	67	64	108	°C/W

(1) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

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7.5 Electrical Characteristics, Reference Section

over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)	TL494C, TL494I			UNIT
		MIN	TYP(2)	MAX	
Output voltage (REF)	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25	mV
Output regulation	I_O = 1 mA to 10 mA		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		2	10	mV/V
Short-circuit output current(3)	REF = 0 V		25		mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values, except for parameter changes with temperature, are at T_A = 25°C.
(3) Duration of short circuit should not exceed one second.

7.6 Electrical Characteristics, Oscillator Section

C_T = 0.01 µF, R_T = 12 kΩ (see Figure 8-1)

PARAMETER	TEST CONDITIONS(1)	TL494C, TL494I			UNIT
		MIN	TYP(2)	MAX	
Frequency			10		kHz
Standard deviation of frequency(3)	All values of V_{CC}, C_T, R_T, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1		Hz/kHz
Frequency change with temperature(4)	ΔT_A = MIN to MAX			10	Hz/kHz

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values, except for parameter changes with temperature, are at T_A = 25°C.
(3) Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} \left(x_n - \overline{X}\right)^2}{N-1}}$$

(4) Temperature coefficient of timing capacitor and timing resistor are not taken into account.

7.7 Electrical Characteristics, Error-Amplifier Section

See Figure 8-2

PARAMETER	TEST CONDITIONS	TL494C, TL494I			UNIT
		MIN	TYP(1)	MAX	
Input offset voltage	V_O (FEEDBACK) = 2.5 V		2	10	mV
Input offset current	V_O (FEEDBACK) = 2.5 V		25	250	nA
Input bias current	V_O (FEEDBACK) = 2.5 V		0.2	1	µA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	–0.3 to V_{CC} – 2			V
Open-loop voltage amplification	ΔV_O = 3 V, V_O = 0.5 V to 3.5 V, R_L = 2 kΩ	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V, T_A = 25°C	65	80		dB
Output sink current (FEEDBACK)	V_{ID} = –15 mV to –5 V, V (FEEDBACK) = 0.7 V	0.3	0.7		mA
Output source current (FEEDBACK)	V_{ID} = 15 mV to 5 V, V (FEEDBACK) = 3.5 V	–2			mA

(1) All typical values, except for parameter changes with temperature, are at T_A = 25°C.

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7.8 Electrical Characteristics, Output Section

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Collector off-state current		V_{CE} = 40 V, V_{CC} = 40 V		2	100	µA
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0			–100	µA
Collector-emitter saturation voltage	Common emitter	V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter follower	$V_{O(C1 \text{ or } C2)}$ = 15 V, I_E = –200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}			3.5	mA

(1) All typical values, except for temperature coefficient, are at T_A = 25°C.

7.9 Electrical Characteristics, Dead-Time Control Section

See Figure 8-1

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Input bias current (DEAD-TIME CTRL)	V_I = 0 to 5.25 V		–2	–10	µA
Maximum duty cycle, each output	V_I (DEAD-TIME CTRL) = 0, C_T = 0.01 µF, R_T = 12 kΩ		45%		—
Input threshold voltage (DEAD-TIME CTRL)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

(1) All typical values, except for temperature coefficient, are at T_A = 25°C.

7.10 Electrical Characteristics, PWM Comparator Section

See Figure 8-1

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Input threshold voltage (FEEDBACK)	Zero duty cyle		4	4.5	V
Input sink current (FEEDBACK)	V (FEEDBACK) = 0.7 V	0.3	0.7		mA

(1) All typical values, except for temperature coefficient, are at T_A = 25°C.

7.11 Electrical Characteristics, Total Device

PARAMETER	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
Standby supply current	R_T = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10	mA
		V_{CC} = 40 V		9	15	
Average supply current	V_I (DEAD-TIME CTRL) = 2 V, See Figure 8-1			7.5		mA

(1) All typical values, except for temperature coefficient, are at T_A = 25°C.

7.12 Switching Characteristics

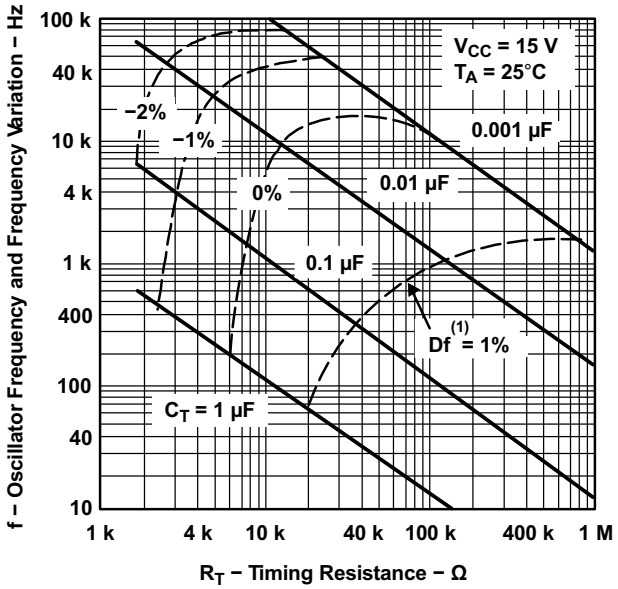
T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Rise time	Common-emitter configuration, See Figure 8-3		100	200	ns
Fall time			25	100	ns
Rise time	Emitter-follower configuration, See Figure 8-4		100	200	ns
Fall time			40	100	ns

(1) All typical values, except for temperature coefficient, are at T_A = 25°C.

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7.13 Typical Characteristics



Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 7-1. Oscillator Frequency and Frequency Variation vs Timing Resistance

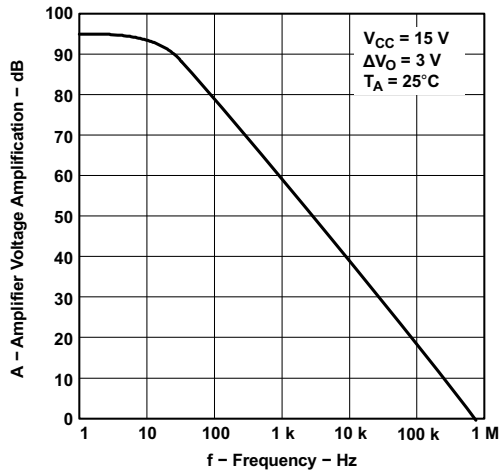


Figure 7-2. Amplifier Voltage Amplification vs Frequency

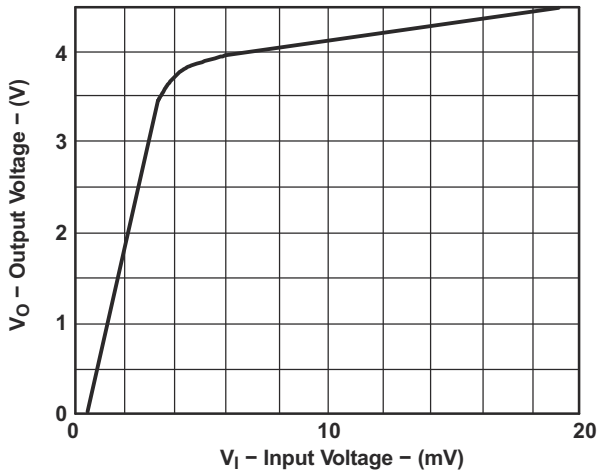


Figure 7-3. Error Amplifier Transfer Characteristics

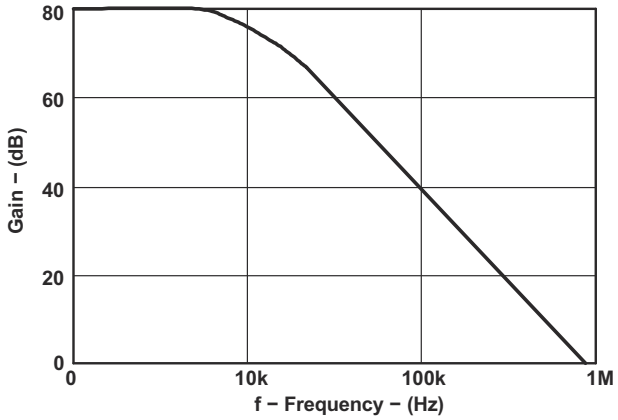


Figure 7-4. Error Amplifier Bode Plot

8 Parameter Measurement Information

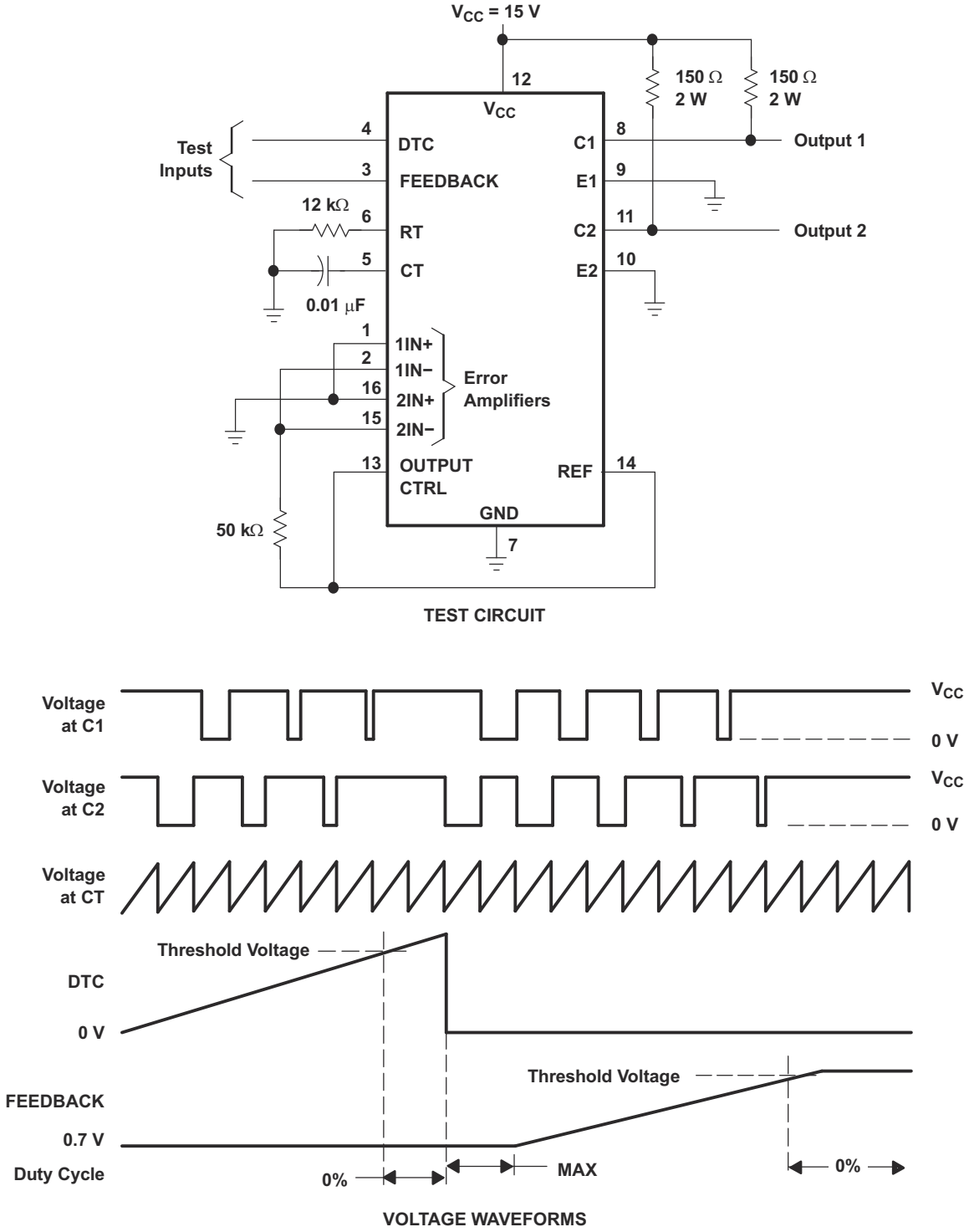


Figure 8-1. Operational Test Circuit and Waveforms

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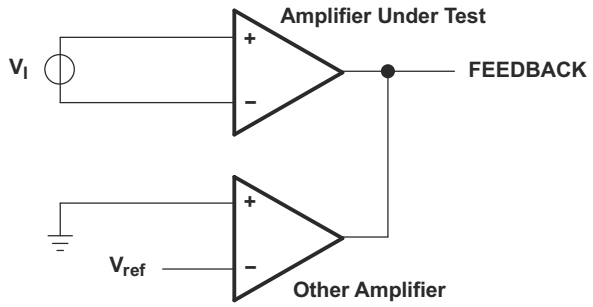
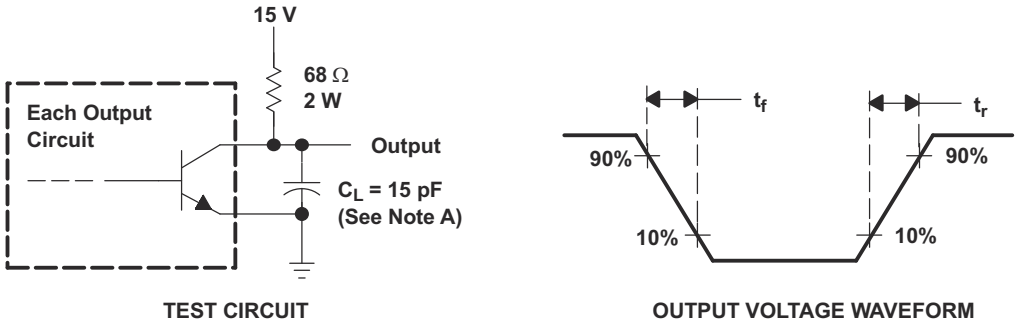
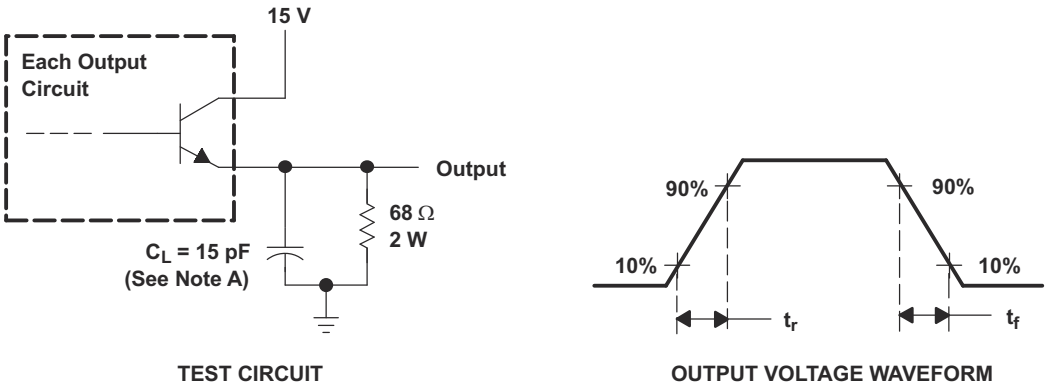


Figure 8-2. Amplifier Characteristics



NOTE A: C_L includes probe and jig capacitance.

Figure 8-3. Common-Emitter Configuration



NOTE A: C_L includes probe and jig capacitance.

Figure 8-4. Emitter-Follower Configuration

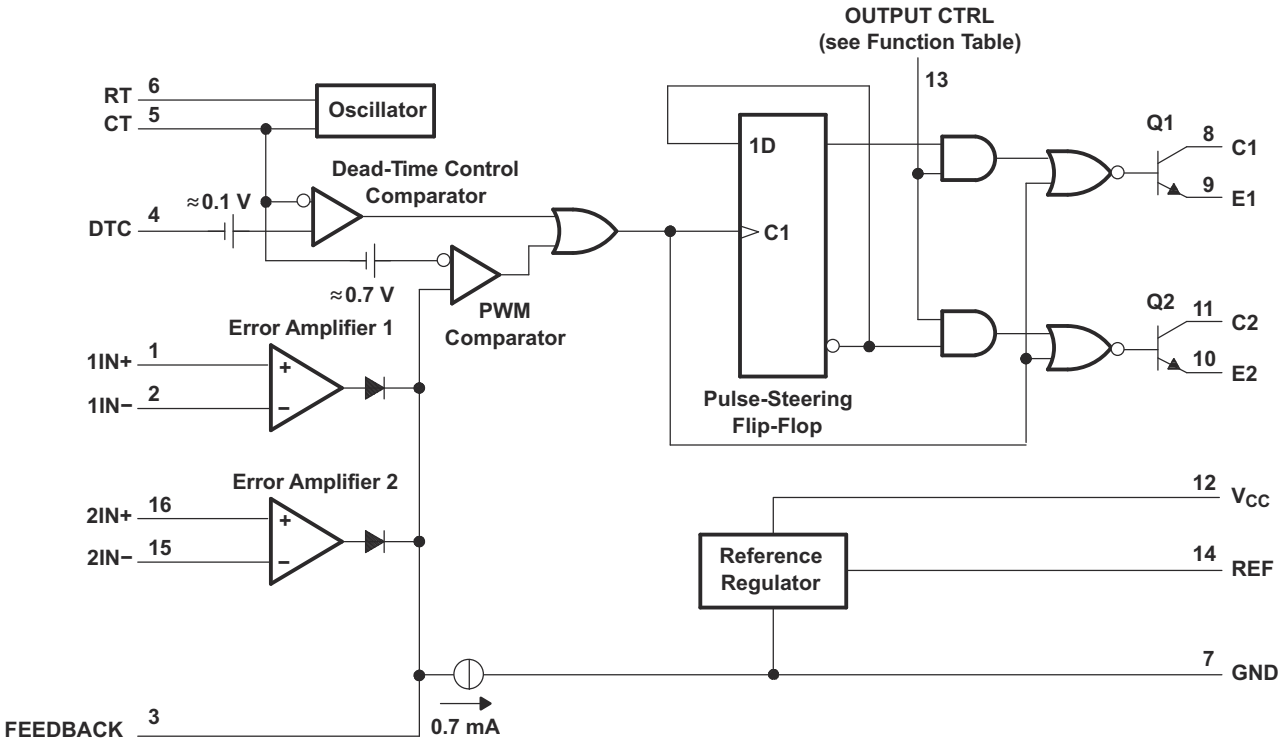
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9 Detailed Description

9.1 Overview

The design of the TL494 not only incorporates the primary building blocks required to control a switching power supply, but also addresses many basic problems and reduces the amount of additional circuitry required in the total design. The TL494 is a fixed-frequency pulse-width-modulation (PWM) control circuit. Modulation of output pulses is accomplished by comparing the sawtooth waveform created by the internal oscillator on the timing capacitor (CT) to either of two control signals. The output stage is enabled during the time when the sawtooth voltage is greater than the voltage control signals. As the control signal increases, the time during which the sawtooth input is greater decreases; therefore, the output pulse duration decreases. A pulse-steering flip-flop alternately directs the modulated pulse to each of the two output transistors. For more information on the operation of the TL494, see the application notes located on ti.com.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 5-V Reference Regulator

The TL494 internal 5-V reference regulator output is the REF pin. In addition to providing a stable reference, it acts as a preregulator and establishes a stable supply from which the output-control logic, pulse-steering flip-flop, oscillator, dead-time control comparator, and PWM comparator are powered. The regulator employs a band-gap circuit as its primary reference to maintain thermal stability of less than 100-mV variation over the operating free-air temperature range of 0°C to 70°C. Short-circuit protection is provided to protect the internal reference and preregulator; 10 mA of load current is available for additional bias circuits. The reference is internally programmed to an initial accuracy of ±5% and maintains a stability of less than 25-mV variation over an input voltage range of 7 V to 40 V. For input voltages less than 7 V, the regulator saturates within 1 V of the input and tracks it.

9.3.2 Oscillator

The oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison to the various control signals.

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The frequency of the oscillator is programmed by selecting timing components R_T and C_T. The oscillator charges the external timing capacitor, C_T, with a constant current, the value of which is determined by the external timing resistor, R_T. This produces a linear-ramp voltage waveform. When the voltage across C_T reaches 3 V, the oscillator circuit discharges it, and the charging cycle is reinitiated. The charging current is determined by the formula:

$$I_{CHARGE} = \frac{3\,V}{R_T} \tag{1}$$

The period of the sawtooth waveform is:

$$T = \frac{3\,V \times C_T}{I_{CHARGE}} \tag{2}$$

The frequency of the oscillator becomes:

$$f_{OSC} = \frac{1}{R_T \times C_T} \tag{3}$$

However, the oscillator frequency is equal to the output frequency only for single-ended applications. For push-pull applications, the output frequency is one-half the oscillator frequency.

Single-ended applications:

$$f = \frac{1}{R_T \times C_T} \tag{4}$$

Push-pull applications:

$$f = \frac{1}{2R_T \times C_T} \tag{5}$$

9.3.3 Dead-time Control

The dead-time control input provides control of the minimum dead time (off time). The output of the comparator inhibits switching transistors Q1 and Q2 when the voltage at the input is greater than the ramp voltage of the oscillator. An internal offset of 110 mV ensures a minimum dead time of ~3% with the dead-time control input grounded. Applying a voltage to the dead-time control input can impose additional dead time. This provides a linear control of the dead time from its minimum of 3% to 100% as the input voltage is varied from 0 V to 3.3 V, respectively. With full-range control, the output can be controlled from external sources without disrupting the error amplifiers. The dead-time control input is a relatively high-impedance input (I_I < 10 µA) and should be used where additional control of the output duty cycle is required. However, for proper control, the input must be terminated. An open circuit is an undefined condition.

9.3.4 Comparator

The comparator is biased from the 5-V reference regulator. This provides isolation from the input supply for improved stability. The input of the comparator does not exhibit hysteresis, so protection against false triggering near the threshold must be provided. The comparator has a response time of 400 ns from either of the control-signal inputs to the output transistors, with only 100 mV of overdrive. This ensures positive control of the output within one-half cycle for operation within the recommended 300-kHz range.

9.3.5 Pulse-Width Modulation (PWM)

The comparator also provides modulation control of the output pulse width. For this, the ramp voltage across timing capacitor C_T is compared to the control signal present at the output of the error amplifiers. The timing capacitor input incorporates a series diode that is omitted from the control signal input. This requires the control

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signal (error amplifier output) to be ~0.7 V greater than the voltage across C_T to inhibit the output logic, and ensures maximum duty cycle operation without requiring the control voltage to sink to a true ground potential. The output pulse width varies from 97% of the period to 0 as the voltage present at the error amplifier output varies from 0.5 V to 3.5 V, respectively.

9.3.6 Error Amplifiers

Both high-gain error amplifiers receive their bias from the V_I supply rail. This permits a common-mode input voltage range from –0.3 V to 2 V less than V_I. Both amplifiers behave characteristically of a single-ended single-supply amplifier, in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With both outputs ORed together at the inverting input node of the PWM comparator, the amplifier demanding the minimum pulse out dominates. The amplifier outputs are biased low by a current sink to provide maximum pulse width out when both amplifiers are biased off.

9.3.7 Output-Control Input

The output-control input determines whether the output transistors operate in parallel or push-pull. This input is the supply source for the pulse-steering flip-flop. The output-control input is asynchronous and has direct control over the output, independent of the oscillator or pulse-steering flip-flop. The input condition is intended to be a fixed condition that is defined by the application. For parallel operation, the output-control input must be grounded. This disables the pulse-steering flip-flop and inhibits its outputs. In this mode, the pulses seen at the output of the dead-time control/PWM comparator are transmitted by both output transistors in parallel. For push-pull operation, the output-control input must be connected to the internal 5-V reference regulator. Under this condition, each of the output transistors is enabled, alternately, by the pulse-steering flip-flop.

9.3.8 Output Transistors

Two output transistors are available on the TL494. Both transistors are configured as open collector/open emitter, and each is capable of sinking or sourcing up to 200 mA. The transistors have a saturation voltage of less than 1.3 V in the common-emitter configuration and less than 2.5 V in the emitter-follower configuration. The outputs are protected against excessive power dissipation to prevent damage, but do not employ sufficient current limiting to allow them to be operated as current-source outputs.

9.4 Device Functional Modes

When the OUTPUT CTRL pin is tied to ground, the TL494 is operating in single-ended or parallel mode. When the OUTPUT CTRL pin is tied to V_{REF}, the TL494 is operating in normal push-pull operation.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The following design example uses the TL494 to create a 5-V/10-A power supply. This application was taken from application note SLVA001.

10.2 Typical Application

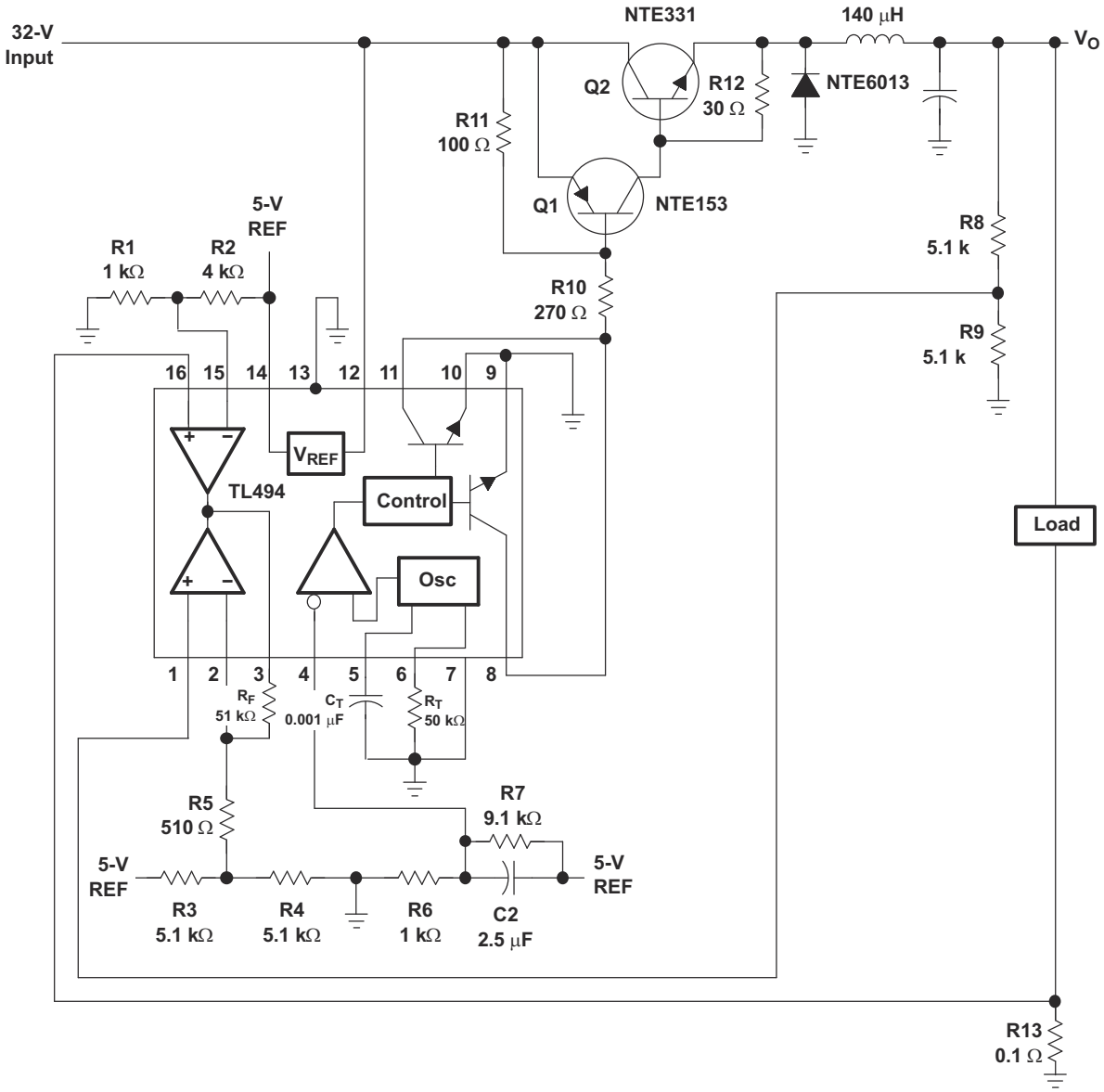


Figure 10-1. Switching and Control Sections

10.2.1 Design Requirements

- V_I = 32 V
- V_O = 5 V
- I_O = 10 A
- f_{OSC} = 20-kHz switching frequency
- V_R = 20-mV peak-to-peak (V_{RIPPLE})
- ΔI_L = 1.5-A inductor current change

10.2.2 Detailed Design Procedure

10.2.2.1 Input Power Source

The 32-V dc power source for this supply uses a 120-V input, 24-V output transformer rated at 75 VA. The 24-V secondary winding feeds a full-wave bridge rectifier, followed by a current-limiting resistor (0.3 Ω) and two filter capacitors (see Figure 10-2).

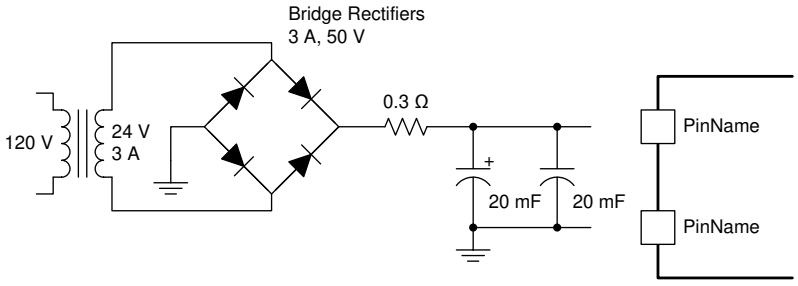


Figure 10-2. Input Power Source

The output current and voltage are determined by Equation 6 and Equation 7:

$$V_{RECTIFIER} = V_{SECONDARY} \times \sqrt{2} = 24\,V \times \sqrt{2} = 34\,V \tag{6}$$

$$I_{RECTIFIER(AVG)} \approx \frac{V_O}{V_I} \times I_O \approx \frac{5\,V}{32\,V} \times 10\,A = 1.6\,A \tag{7}$$

The 3-A/50-V full-wave bridge rectifier meets these calculated conditions. Figure 10-1 shows the switching and control sections.

10.2.2.2 Control Circuits

10.2.2.2.1 Oscillator

Connecting an external capacitor and resistor to pins 5 and 6 controls the TL494 oscillator frequency. The oscillator is set to operate at 20 kHz, using the component values calculated by Equation 8 and Equation 9:

$$f_{OSC} = \frac{1}{R_T \times C_T} \tag{8}$$

Choose C_T = 0.001 µF and calculate R_T:

$$R_T = \frac{1}{f_{OSC} \times C_T} = \frac{1}{(20 \times 10^3) \times (0.001 \times 10^{-6})} = 50\ k\Omega \tag{9}$$

10.2.2.2.2 Error Amplifier

The error amplifier compares a sample of the 5-V output to the reference and adjusts the PWM to maintain a constant output current (see Figure 10-3).

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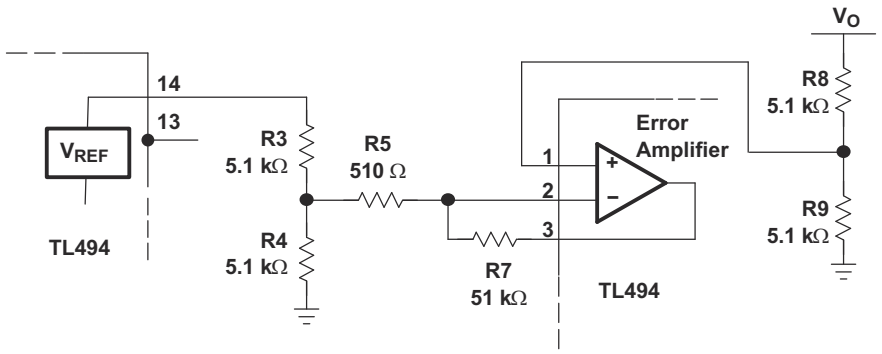


Figure 10-3. Error-Amplifier Section

The TL494 internal 5-V reference is divided to 2.5 V by R3 and R4. The output-voltage error signal also is divided to 2.5 V by R8 and R9. If the output must be regulated to exactly 5.0 V, a 10-kΩ potentiometer can be used in place of R8 to provide an adjustment.

To increase the stability of the error-amplifier circuit, the output of the error amplifier is fed back to the inverting input through R_T, reducing the gain to 101.

10.2.2.2.3 Current-Limiting Amplifier

The power supply was designed for a 10-A load current and an I_L swing of 1.5 A, therefore, the short-circuit current should be:

$$I_{SC} = I_O + \frac{I_L}{2} = 10.75\,A \tag{10}$$

The current-limiting circuit is shown in Figure 10-4.

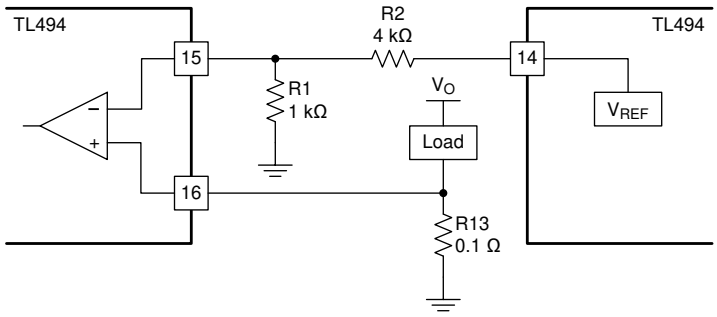


Figure 10-4. Current-Limiting Circuit

Resistors R1 and R2 set the reference of approximately 1 V on the inverting input of the current-limiting amplifier. Resistor R13, in series with the load, applies 1 V to the non-inverting terminal of the current-limiting amplifier when the load current reaches 10 A. The output pulse width reduces accordingly. The value of R13 is calculated in Equation 11.

$$R13 = \frac{1V}{10\,A} = 0.1\Omega \tag{11}$$

10.2.2.2.4 Soft Start and Dead Time

To reduce stress on the switching transistors at the start-up time, the start-up surge that occurs as the output filter capacitor charges must be reduced. The availability of the dead-time control makes implementation of a soft-start circuit relatively simple (see Figure 10-5).

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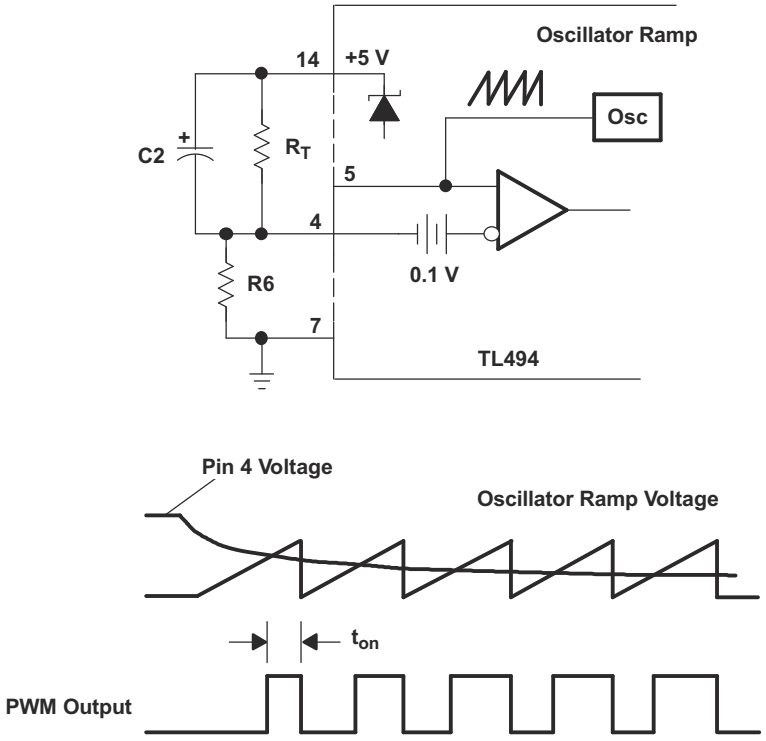


Figure 10-5. Soft-Start Circuit

The soft-start circuit allows the pulse width at the output to increase slowly (see Figure 10-5) by applying a negative slope waveform to the dead-time control input (pin 4).

Initially, capacitor C2 forces the dead-time control input to follow the 5-V regulator, which disables the outputs (100% dead time). As the capacitor charges through R6, the output pulse width slowly increases until the control loop takes command. With a resistor ratio of 1:10 for R6 and R7, the voltage at pin 4 after start-up is 0.1 × 5 V, or 0.5 V.

The soft-start time generally is in the range of 25 to 100 clock cycles. If 50 clock cycles at a 20-kHz switching rate is selected, the soft-start time is:

$$t = \frac{1}{f} = \frac{1}{20\,kHz} = 50\,\mu s\,per\,clock\,cycle \tag{12}$$

The value of the capacitor then is determined by:

$$C2 = \frac{soft-start\,time}{R6} = \frac{50\,\mu s \times 50\,cycles}{1\,k\Omega} = 2.5\,\mu F \tag{13}$$

This helps eliminate any false signals that might be created by the control circuit as power is applied.

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10.2.2.3 Inductor Calculations

The switching circuit used is shown in Figure 39.

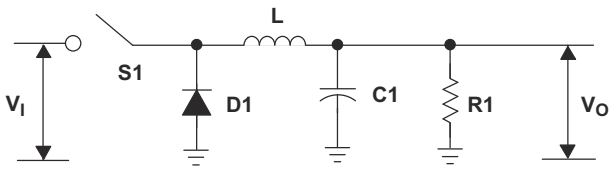


Figure 10-6. Switching Circuit

The size of the inductor (L) required is:

d	=	duty cycle = V_O/V_I = 5 V/32 V = 0.156
f	=	20 kHz (design objective)
t_{on}	=	time on (S1 closed) = (1/f) × d = 7.8 µs
t_{off}	=	time off (S1 open) = (1/f) – ton = 42.2 µs
L	≠	$(V_I – V_O) \times t_{on}/\Delta I_L$
	≠	[(32 V – 5 V) × 7.8 µs]/1.5 A
	≠	140.4 µH

10.2.2.4 Output Capacitance Calculations

Once the filter inductor has been calculated, the value of the output filter capacitor is calculated to meet the output ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important. So, the two components of interest are the capacitance and the effective series resistance (ESR). The maximum ESR is calculated according to the relation between the specified peak-to-peak ripple voltage and the peak-to-peak ripple current.

$$\text{ESR(max)} = \frac{\Delta V_{O(\text{ripple})}}{\Delta I_L} = \frac{V}{1.5\,A} \approx 0.067\,\Omega \tag{14}$$

The minimum capacitance of C3 necessary to maintain the V_O ripple voltage at less than the 100-mV design objective is calculated according to Equation 15:

$$C3 = \frac{\Delta I_L}{8f\,\Delta V_O} = \frac{1.5\,A}{8 \times 20 \times 10^3 \times 0.1\,V} = 94\,\mu F \tag{15}$$

A 220-mF, 60-V capacitor is selected because it has a maximum ESR of 0.074 Ω and a maximum ripple current of 2.8 A.

10.2.2.5 Transistor Power-Switch Calculations

The transistor power switch was constructed with an NTE153 pnp drive transistor and an NTE331 npn output transistor. These two power devices were connected in a pnp hybrid Darlington circuit configuration (see Figure 10-7).

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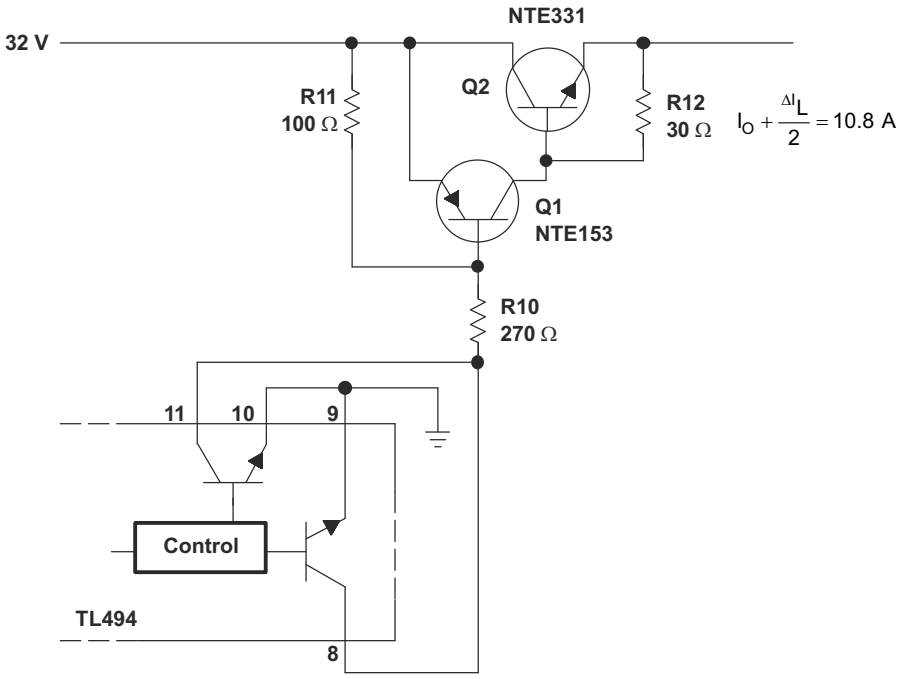


Figure 10-7. Power-Switch Section

The hybrid Darlington circuit must be saturated at a maximum output current of I_O + $\Delta I_L/2$ or 10.8 A. The Darlington h_{FE} at 10.8 A must be high enough not to exceed the 250-mA maximum output collector current of the TL494. Based on published NTE153 and NTE331 specifications, the required power-switch minimum drive was calculated by Equation 16 through Equation 18 to be 144 mA:

$$h_{FE}(Q1) \text{ at } I_C \text{ of } 3\,A = 15 \tag{16}$$

$$h_{FE}(Q2) \text{ at } I_C \text{ of } 10.0\,A = 5 \tag{17}$$

$$i_B \geq \frac{I_O + \frac{I_L}{2}}{h_{FE}(Q2) \times h_{FE}(Q1)} \geq 144\,mA \tag{18}$$

The value of R10 was calculated by:

$$R10 \leq \frac{V_I - [V_{BE}(Q1) + V_{CE}(TL494)]}{i_B} = \frac{32 - (1.5 + 0.7)}{0.144}$$

$$R10 \leq 207\,\Omega \tag{19}$$

Based on these calculations, the nearest standard resistor value of 220 Ω was selected for R10. Resistors R11 and R12 permit the discharge of carriers in switching transistors when they are turned off.

The power supply described demonstrates the flexibility of the TL494 PWM control circuit. This power-supply design demonstrates many of the power-supply control methods provided by the TL494, as well as the versatility of the control circuit.

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10.2.3 Application Curves for Output Characteristics

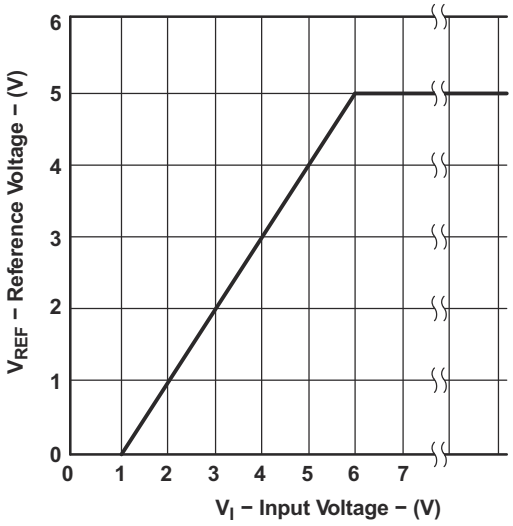


Figure 10-8. Reference Voltage vs Input Voltage

11 Power Supply Recommendations

The TL494 is designed to operate from an input voltage supply range between 7 V and 40 V. This input supply should be well regulated. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 47 µF is a typical choice, however this may vary depending upon the output power being delivered.

12 Layout

12.1 Layout Guidelines

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

12.1.1 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

12.1.2 Input/Output Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the VCC pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case it should also be positioned as close to the IC as possible. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

12.1.3 Compensation Components

External compensation components for stability should also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

12.1.4 Traces and Ground Planes

- Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere.
- The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.
- The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor.
- For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance.
- On multi-layer boards the use of vias will be required to connect traces and different planes.
- It is good practice to use one standard via per 200 mA of current if the trace will need to conduct a significant amount of current from one plane to the other.
- Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting

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in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

12.2 Layout Example

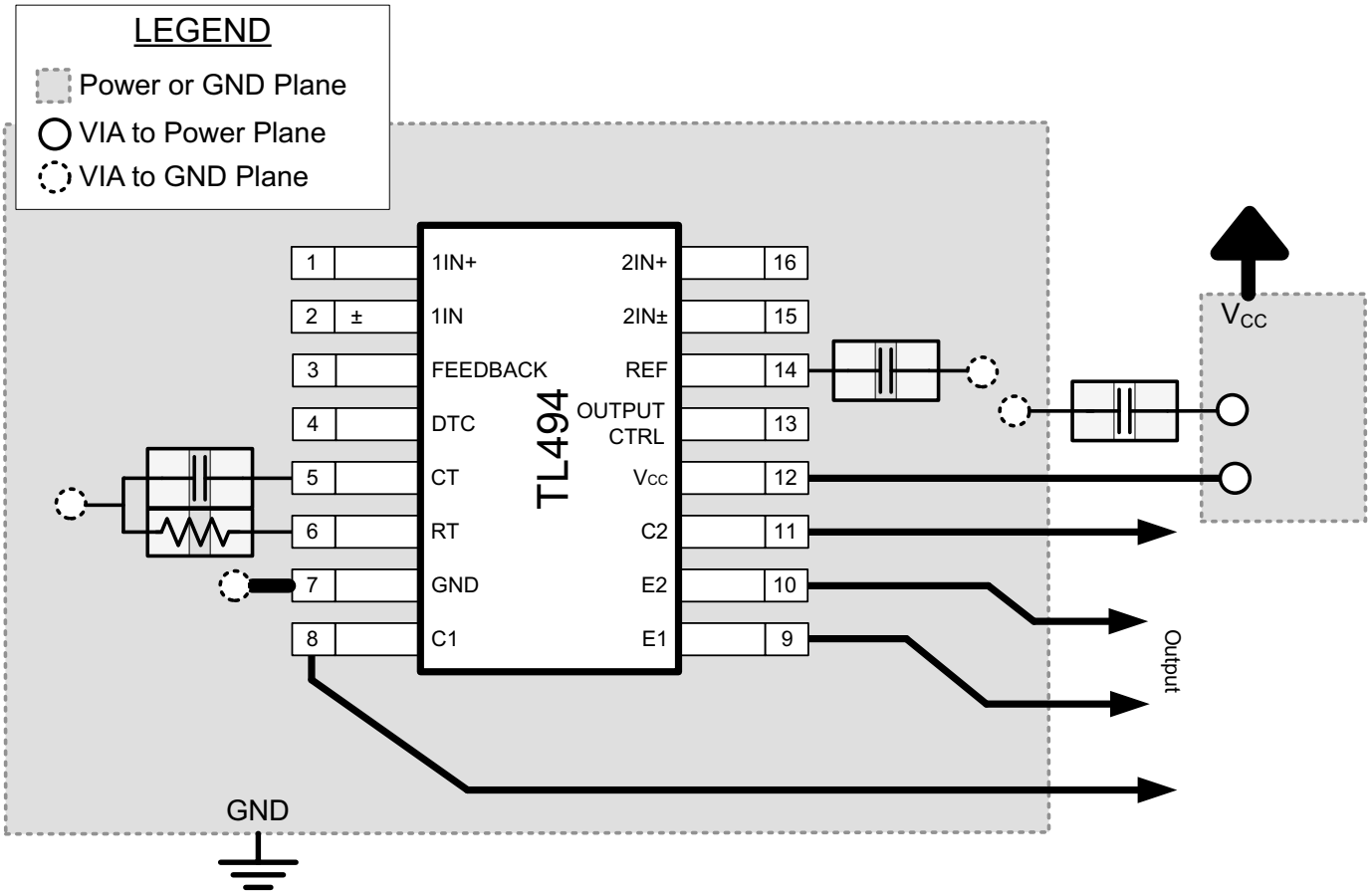


Figure 12-1. Operational Amplifier Board Layout for Noninverting Configuration

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.3 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL494CD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	Samples
TL494CDG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	Samples
TL494CDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	TL494C	Samples
TL494CDRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	Samples
TL494CDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	Samples
TL494CN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL494CN	Samples
TL494CNE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL494CN	Samples
TL494CNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494	Samples
TL494CNSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494	Samples
TL494CPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	Samples
TL494CPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	Samples
TL494ID	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	Samples
TL494IDG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	Samples
TL494IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	TL494I	Samples
TL494IDRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	Samples
TL494IDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	Samples
TL494IN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL494IN	Samples
TL494INE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL494IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

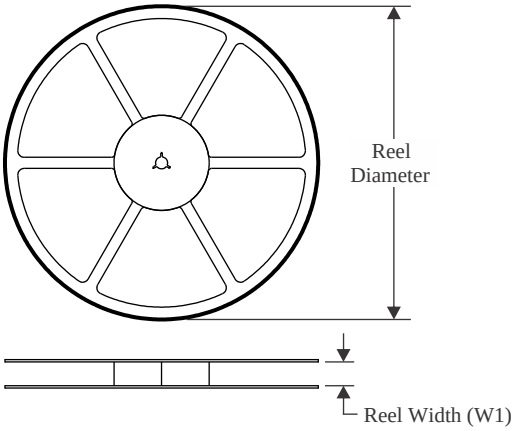
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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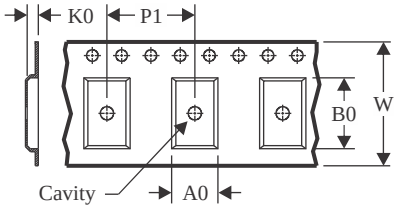
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

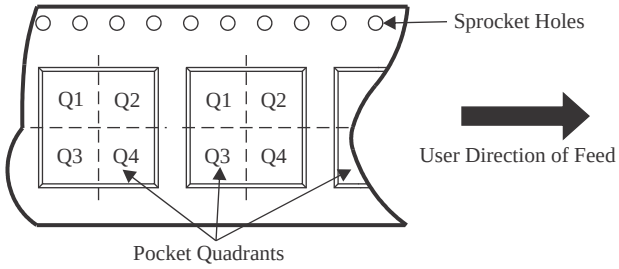


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

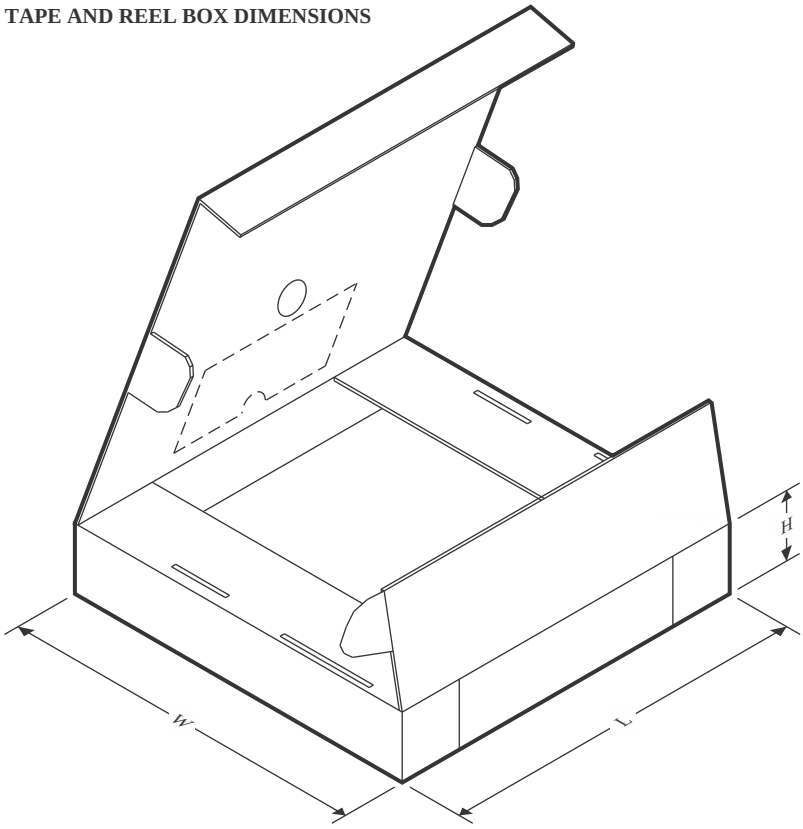
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL494CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL494CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL494IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494IDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

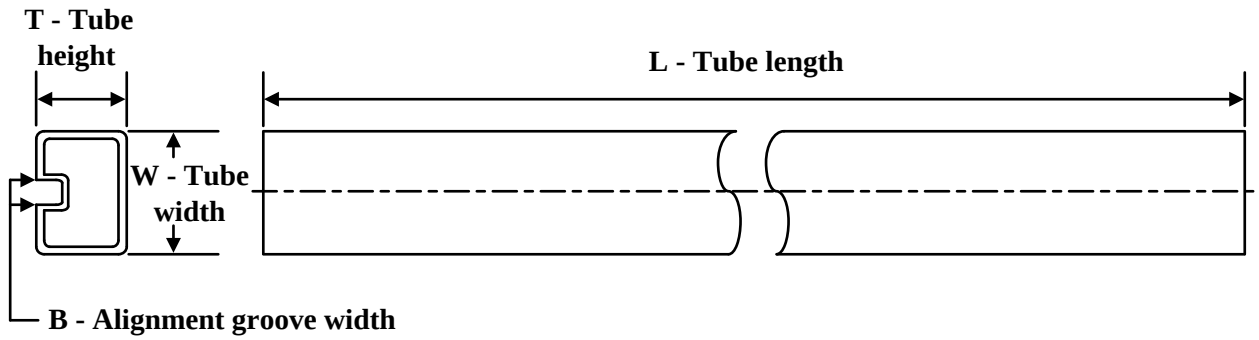
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

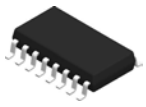
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL494CDR	SOIC	D	16	2500	340.5	336.1	32.0
TL494CDRG4	SOIC	D	16	2500	356.0	356.0	35.0
TL494CDRG4	SOIC	D	16	2500	340.5	336.1	32.0
TL494CNSR	SO	NS	16	2000	356.0	356.0	35.0
TL494CPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TL494IDR	SOIC	D	16	2500	340.5	336.1	32.0
TL494IDRG4	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL494CD	D	SOIC	16	40	507	8	3940	4.32
TL494CD	D	SOIC	16	40	506.6	8	3940	4.32
TL494CDG4	D	SOIC	16	40	506.6	8	3940	4.32
TL494CDG4	D	SOIC	16	40	507	8	3940	4.32
TL494CN	N	PDIP	16	25	506	13.97	11230	4.32
TL494CN	N	PDIP	16	25	506	13.97	11230	4.32
TL494CNE4	N	PDIP	16	25	506	13.97	11230	4.32
TL494CNE4	N	PDIP	16	25	506	13.97	11230	4.32
TL494CPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TL494ID	D	SOIC	16	40	507	8	3940	4.32
TL494IDG4	D	SOIC	16	40	507	8	3940	4.32
TL494IN	N	PDIP	16	25	506	13.97	11230	4.32
TL494IN	N	PDIP	16	25	506	13.97	11230	4.32
TL494INE4	N	PDIP	16	25	506	13.97	11230	4.32
TL494INE4	N	PDIP	16	25	506	13.97	11230	4.32

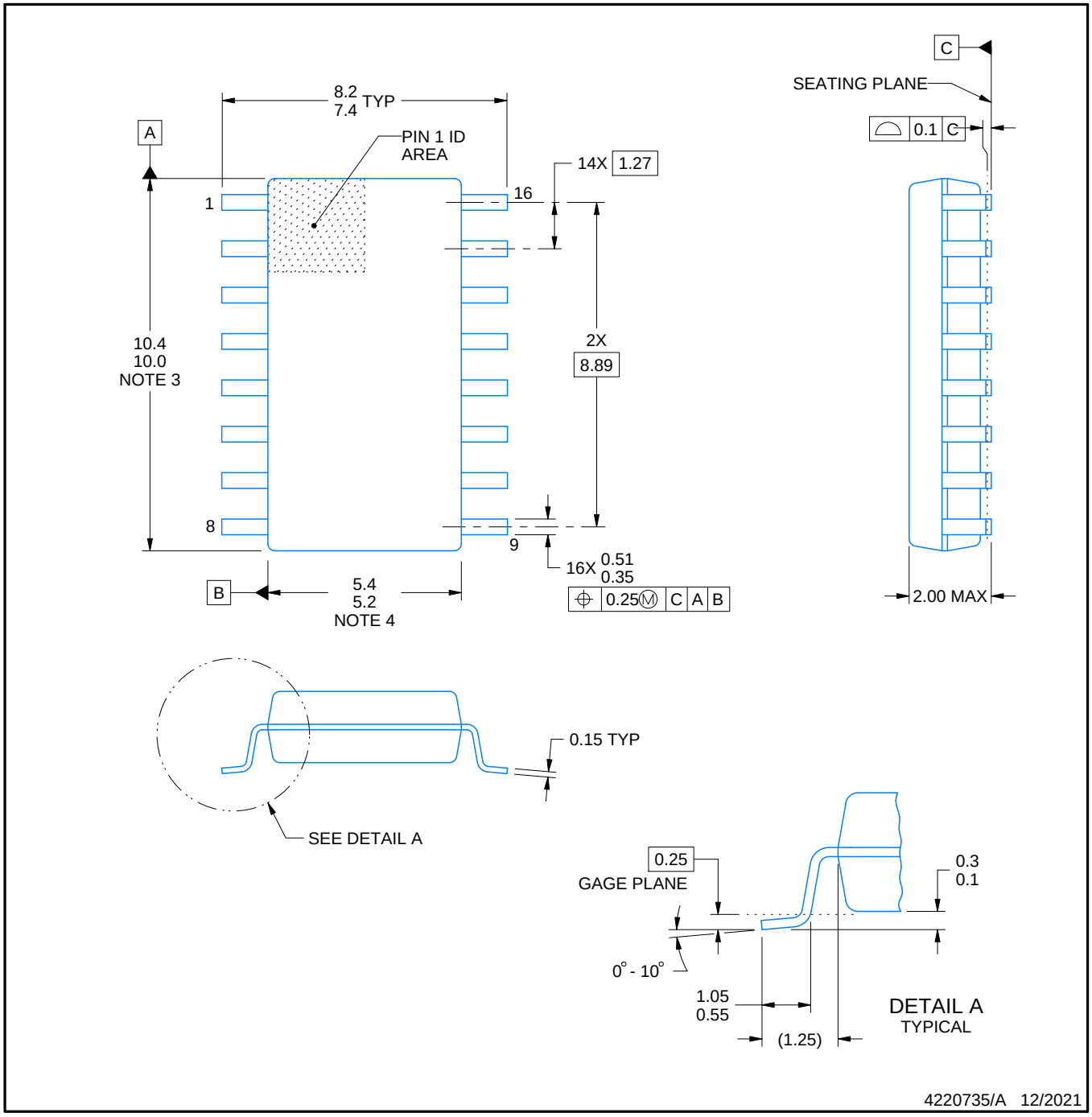


PACKAGE OUTLINE

NS0016A

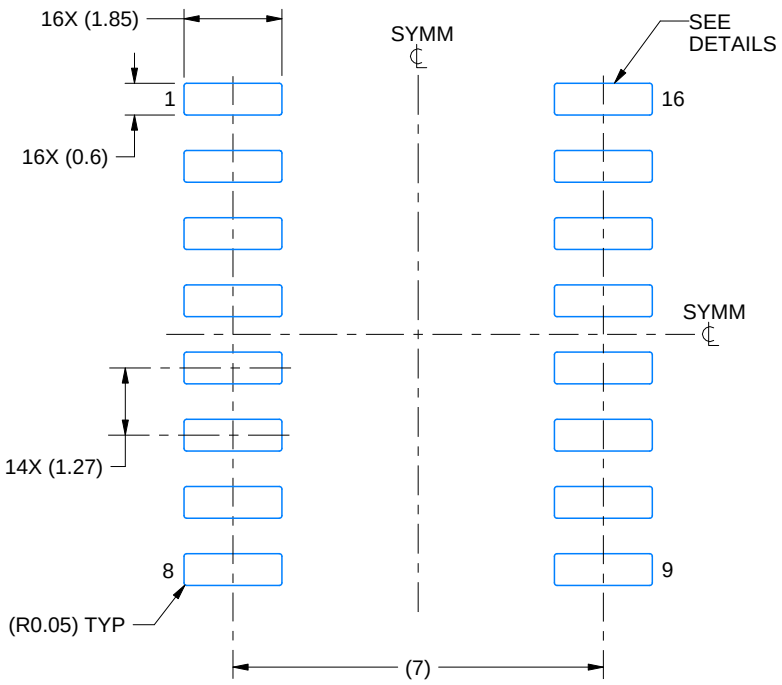
SOP - 2.00 mm max height

SOP

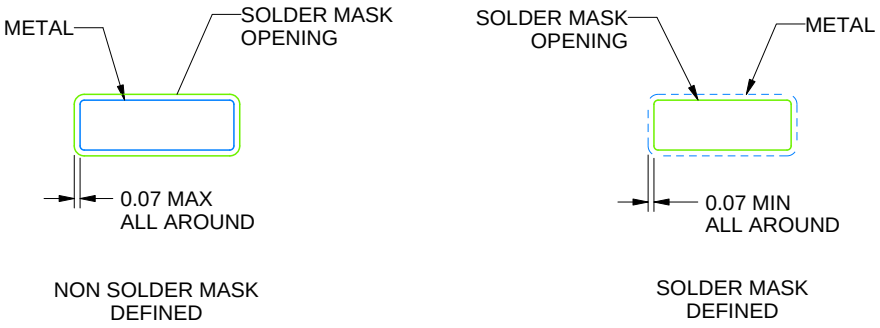


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

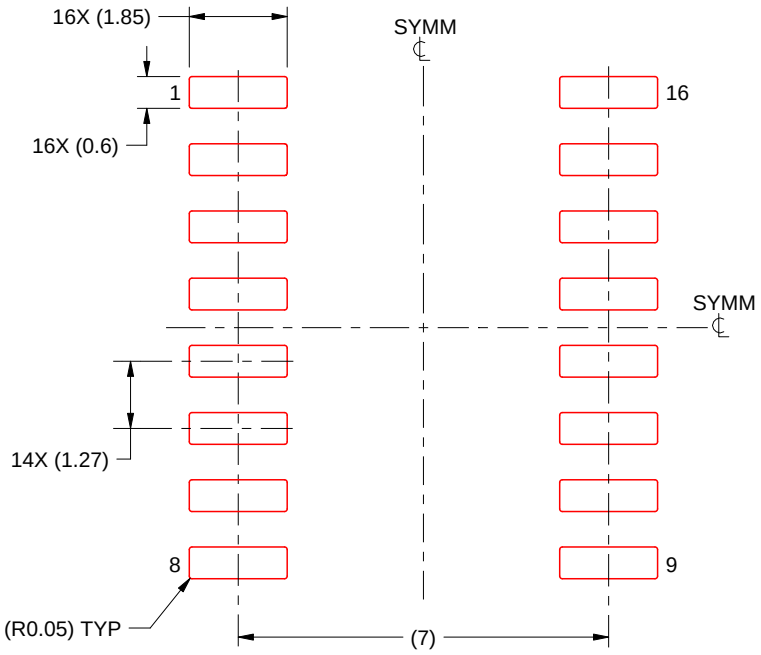
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



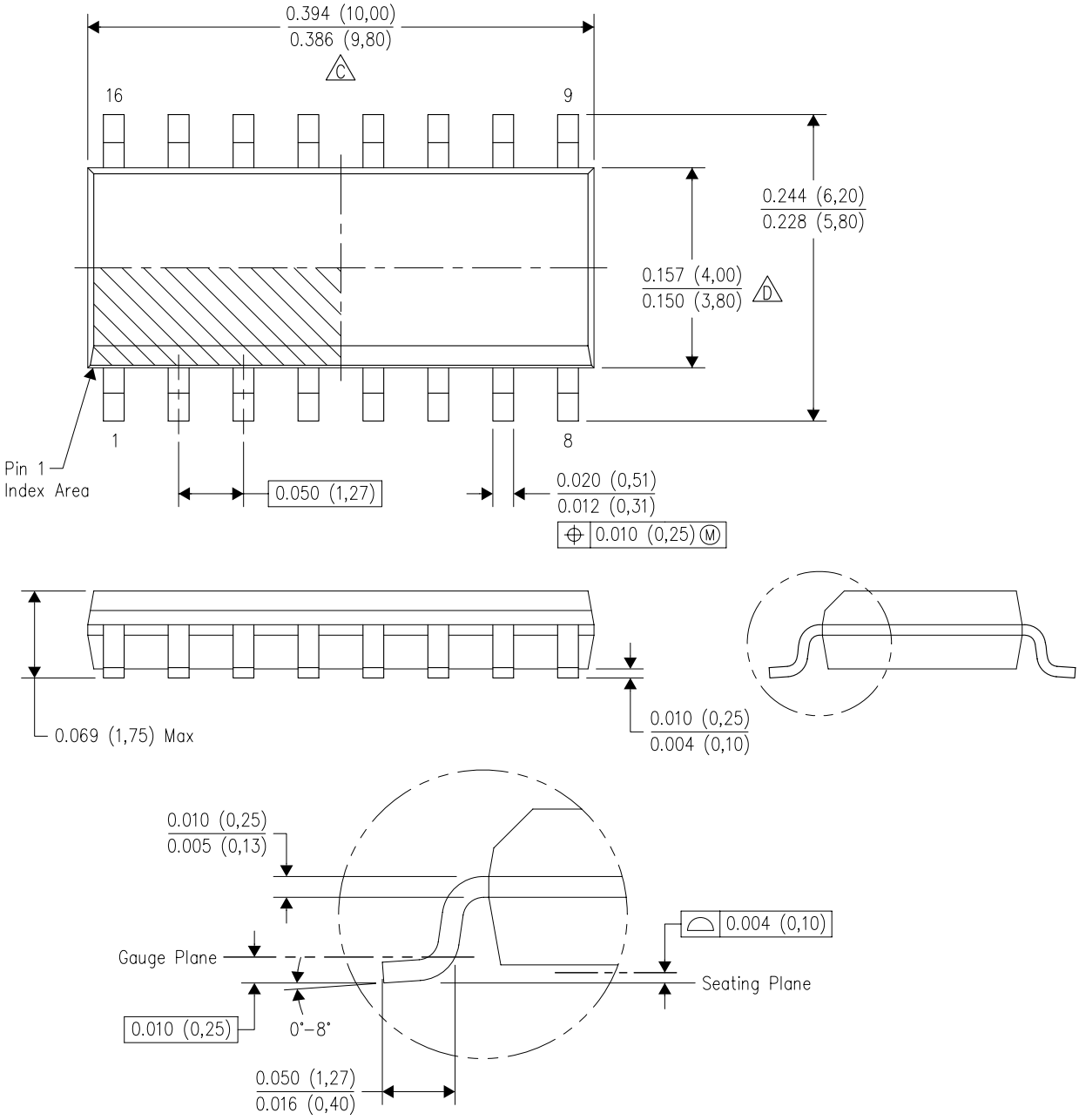
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

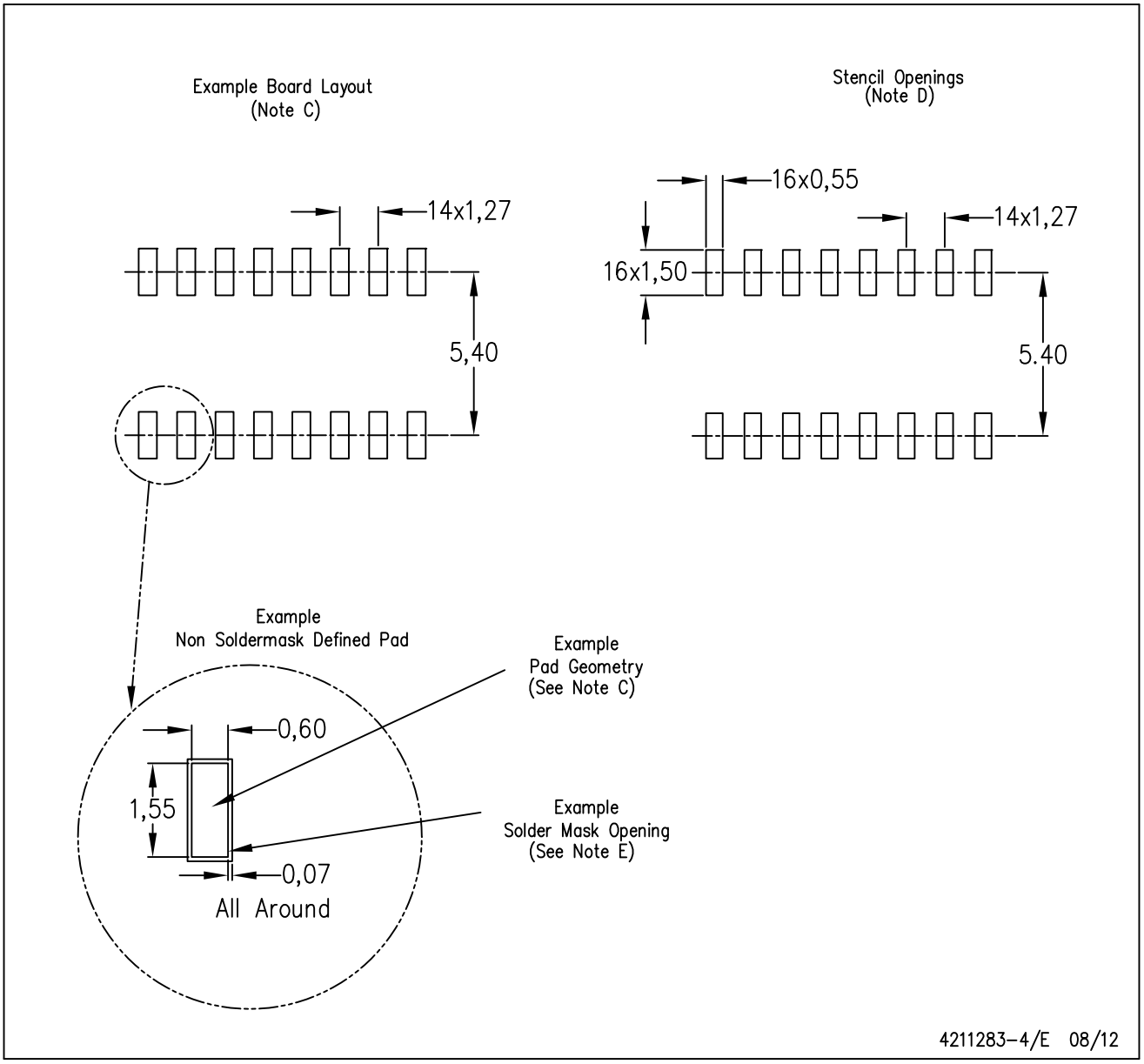
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



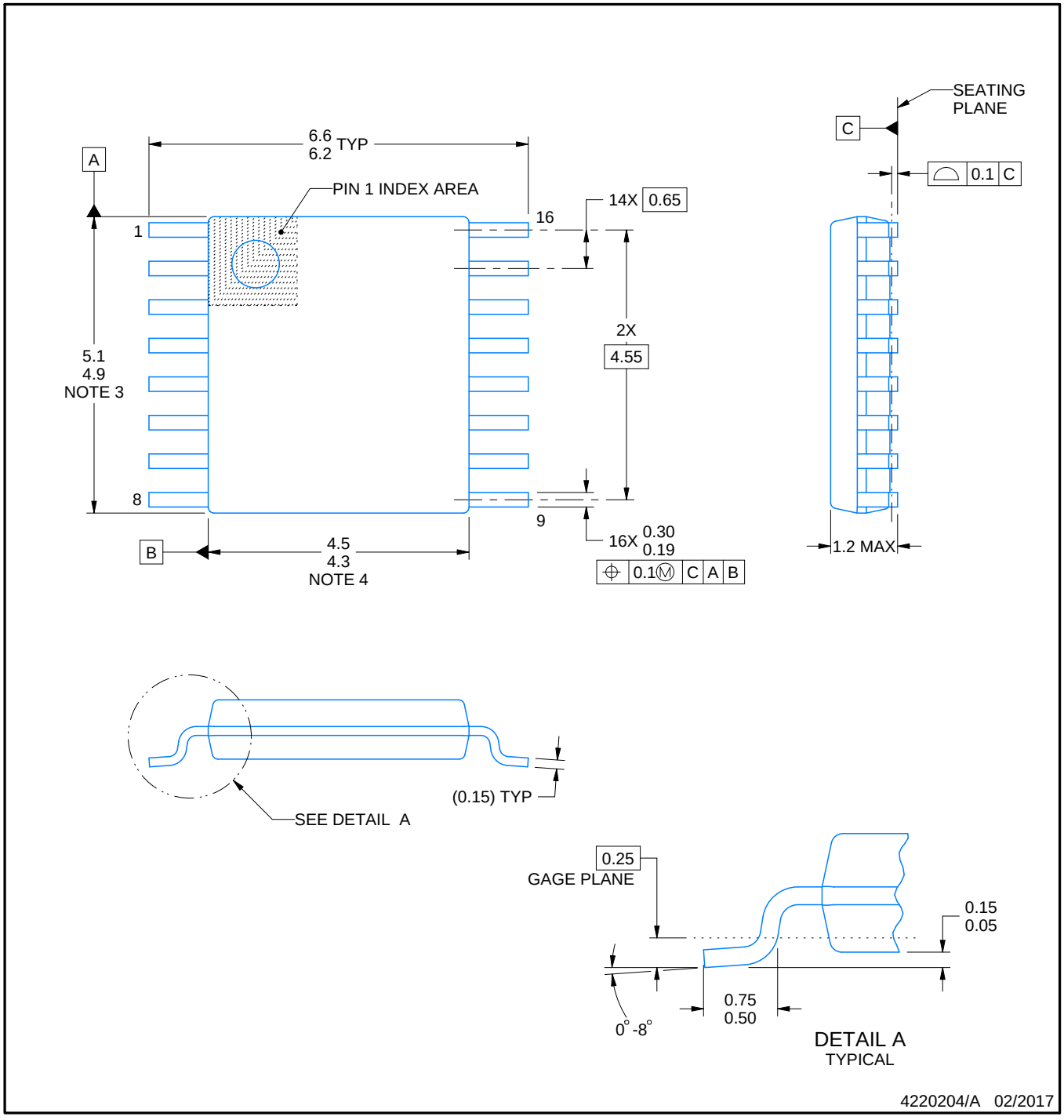
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

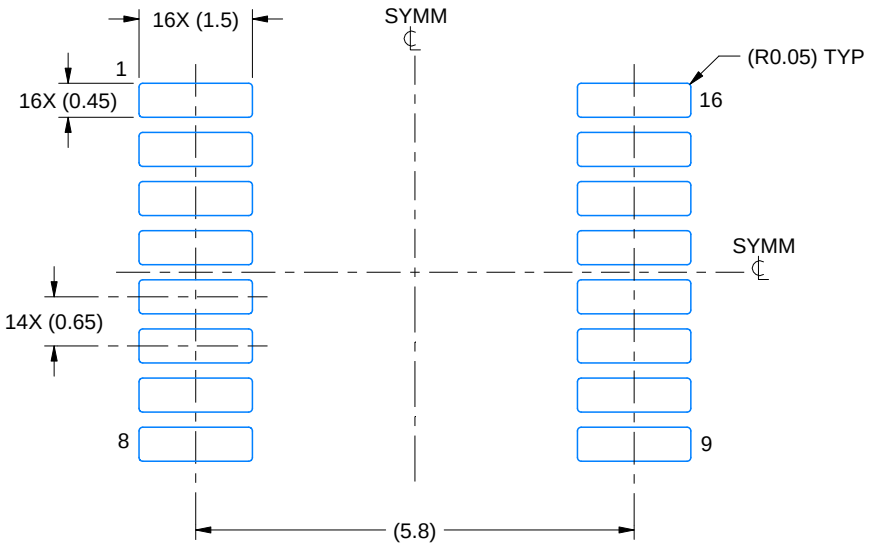
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

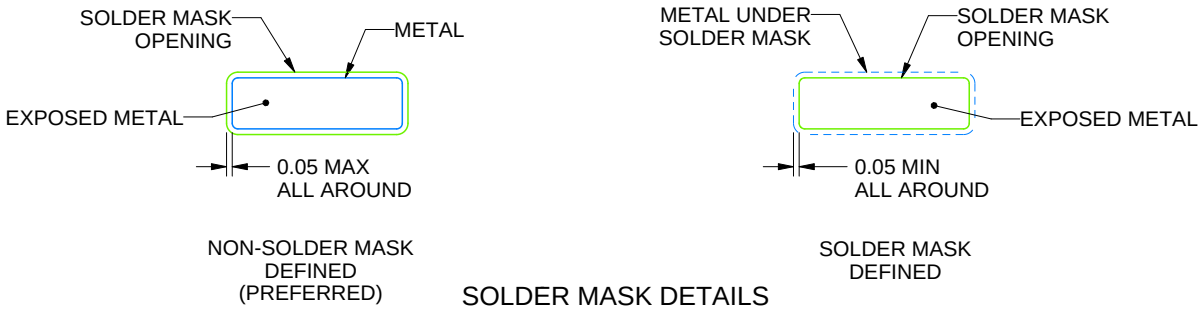


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

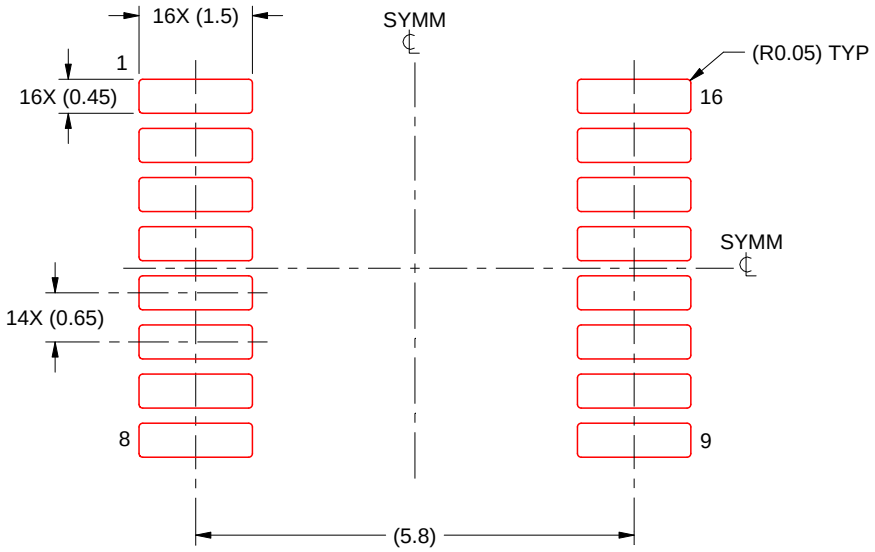


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

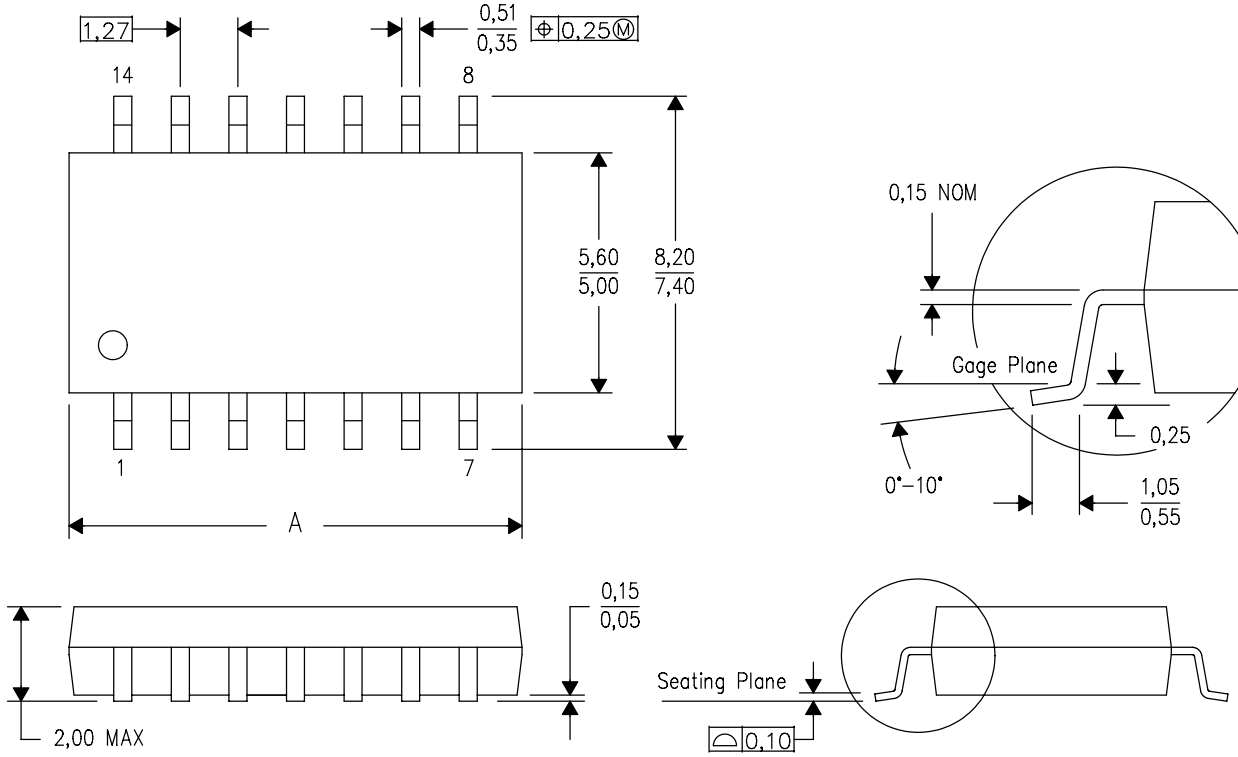
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

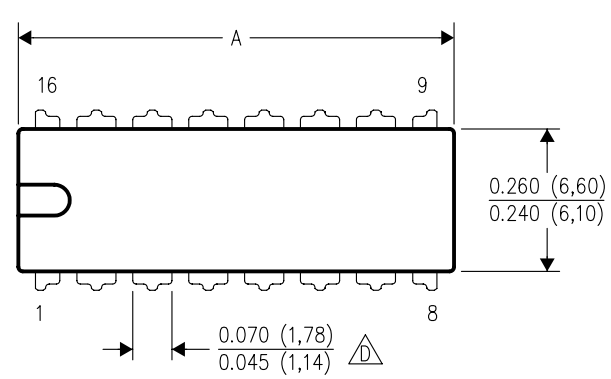
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

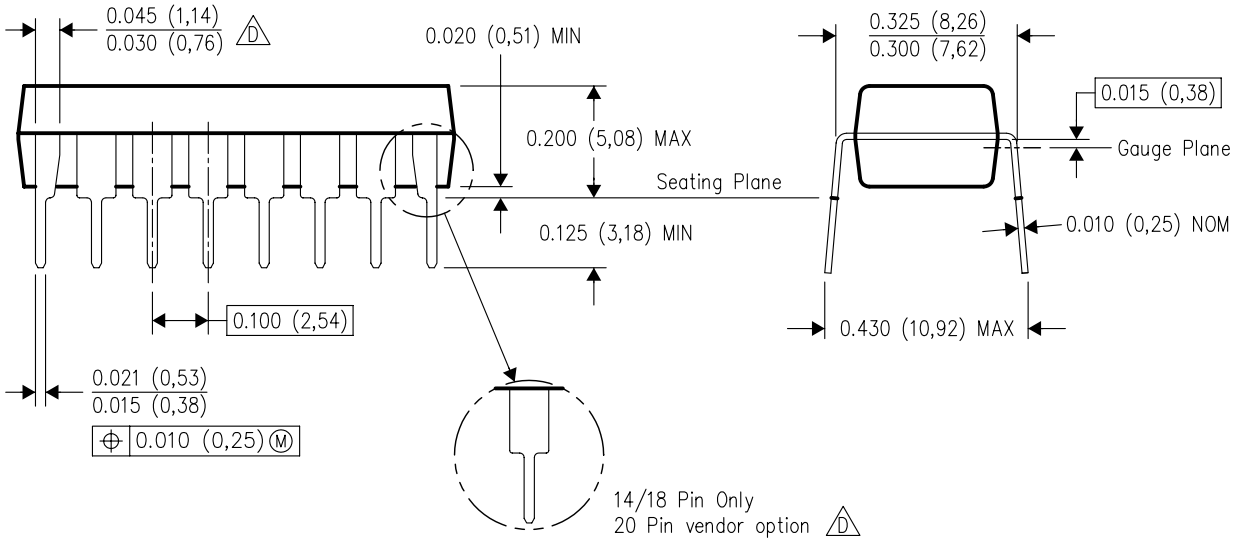
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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