



M95160 M95080

16 Kbit and 8 Kbit serial SPI bus EEPROM
with high speed clock

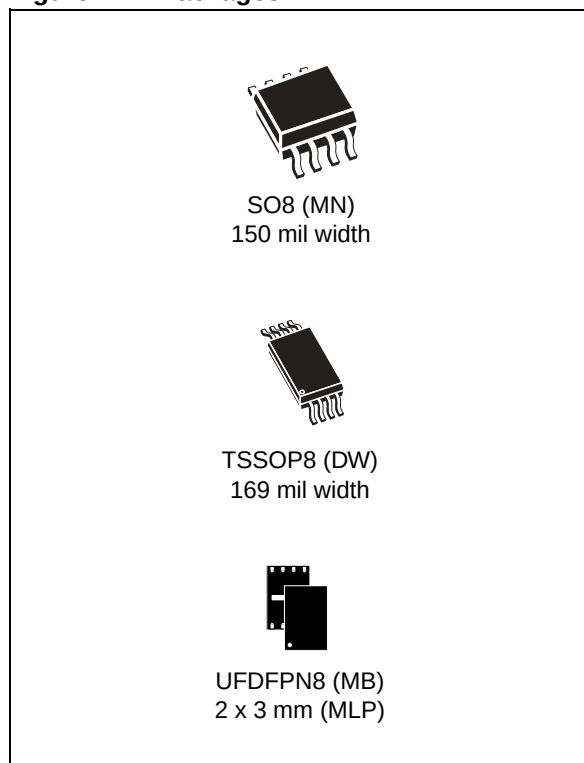
Features

- Compatible with SPI bus serial interface (positive clock SPI modes)
- Single supply voltage:
 - 4.5 V to 5.5 V for M95xxx
 - 2.5 V to 5.5 V for M95xxx-W
 - 1.8 V to 5.5 V for M95xxx-R
- High Speed: 10 MHz
- Status Register
- Hardware Protection of the Status Register
- Byte and page write (up to 32 bytes)
- Self-timed programming cycle
- Adjustable size read-only EEPROM area
- Enhanced ESD protection
- More than 1 million Erase/Write cycles
- More than 40-year data retention
- Packages
 - ECOPACK® (RoHS compliant)

Table 1. Device summary

Reference	Part number
M95160	M95160
	M95160-W
	M95160-R
M95080	M95080
	M95080-W
	M95080-R

Figure 1. Packages



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1 Description

These electrically erasable programmable memory (EEPROM) devices are accessed by a high speed SPI-compatible bus. The memory array is organized as 2048 x 8 bit (M95160), and 1024 x 8 bit (M95080).

The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in [Table 2.](#) and [Figure 2.](#)

The device is selected when Chip Select ($\overline{S}$) is taken Low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

In order to meet environmental requirements, ST offers the M95xxx in ECOPACK® packages. ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. Logic diagram

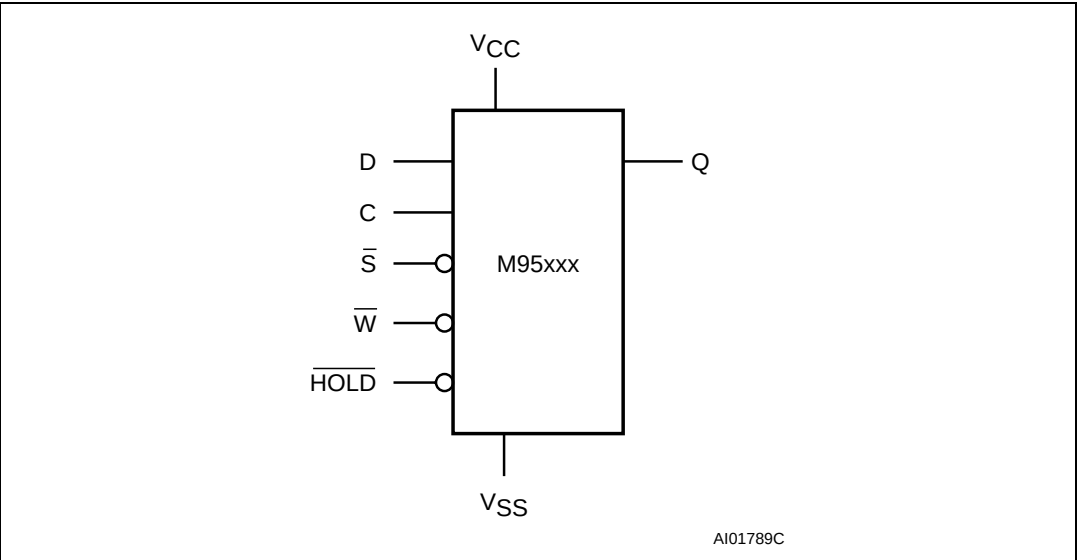
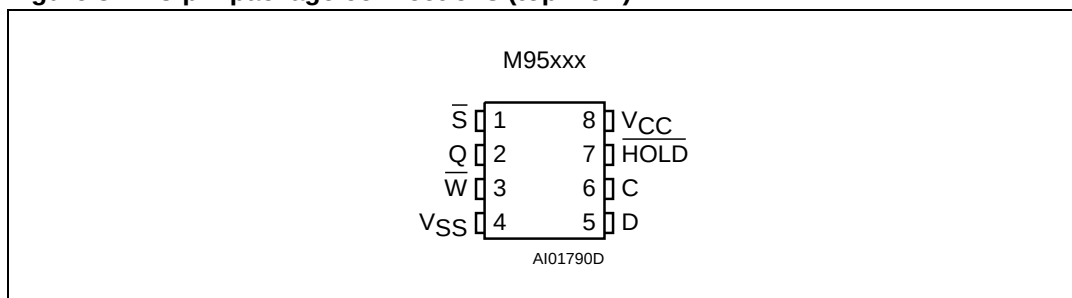


Table 2. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V _{CC}	Supply voltage	
V _{SS}	Ground	

Figure 3. 8-pin package connections (top view)

1. See [Package mechanical](#) section for package dimensions, and how to identify pin-1.

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: $V_{CC}(\min)$ to $V_{CC}(\max)$.

All of the input and output signals must be held High or Low (according to voltages of V_{IH} , V_{OH} , V_{IL} or V_{OL} , as specified in [Table 13](#) to [Table 18](#)). These signals are described next.

2.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) Low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

2.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either High or Low, and must be stable during all write instructions.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 Connecting to the SPI bus

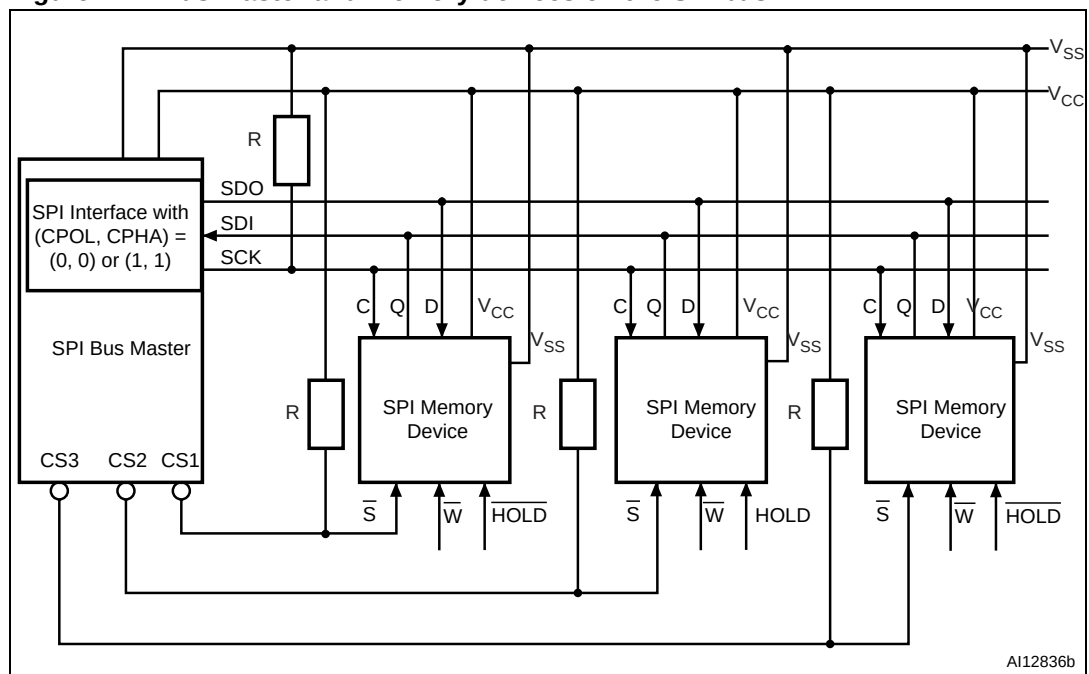
These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes Low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

[Figure 4](#) shows three devices, connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, all the others being high impedance.

Figure 4. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

[Figure 4](#) shows an example of three memory devices connected to an MCU, on an SPI bus. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time, the other memory devices are high impedance.

The pull-up resistor R (represented in [Figure 4](#)) ensures that a device is not selected if the Bus Master leaves the $\overline{S}$ line in the high impedance state.

In applications where the Bus Master may be in a state where all input/output SPI buses are high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled Low (while the $\overline{S}$ line is pulled High): this ensures that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 k Ω .

3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

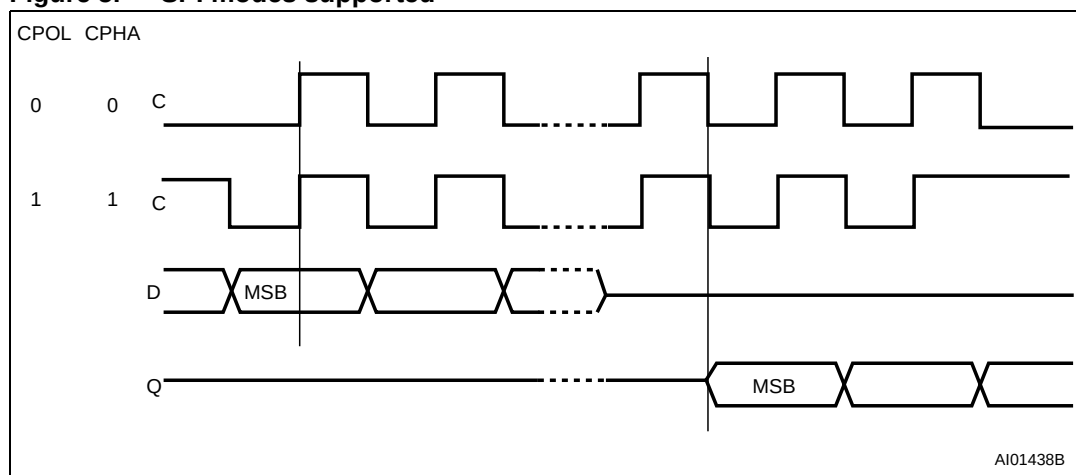
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in [Figure 5.](#), is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. SPI modes supported



4 Operating features

4.1 Supply voltage (V_{CC})

4.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC}(\min)$, $V_{CC}(\max)$] range must be applied (see [Table 9](#), [Table 10](#) and [Table 11](#)). In order to secure a stable dc supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

4.1.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC} . During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage, it is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor.

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been High, prior to going Low to start the first operation.

The V_{CC} rise time must not vary faster than 1 V/ μ s.

4.1.3 Power-up and device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in [Table 9](#), [Table 10](#) and [Table 11](#)).

Once V_{CC} has passed the POR threshold, the device is reset and is in the following state:

- Standby Power mode
- deselected (at next power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started)
- not in the Hold condition

Status Register state:

- the Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0. The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

4.1.4 Power-down

At Power-down (continuous decrease of V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it.

During Power-down, the device must be deselected and in Standby Power mode (that is there should be no internal Write cycle in progress). Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC} .

4.2 Active Power and Standby Power Modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the Active Power mode. The device consumes I_{CC} , as specified in [Table 13](#). to [Table 18](#).

When Chip Select ($\overline{S}$) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to I_{CC1} .

4.3 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven Low at the same time as Serial Clock (C) already being Low.

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven High at the same time as Serial Clock (C) already being Low.

4.4 Status Register

[Figure 6](#). shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See [Section 6.3: Read Status Register \(RDSR\)](#) for a detailed description of the Status Register bits

4.5 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
 - Power-up
 - Write Disable (WRDI) instruction completion
 - Write Status Register (WRSR) instruction completion
 - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP1, BP0) bits of the Status Register to be protected.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points need to be noted in the previous sentence:

- The 'last bit of the instruction' can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The 'next rising edge of Serial Clock (C)' might (or might not) be the next bus transaction for some other device on the SPI bus.

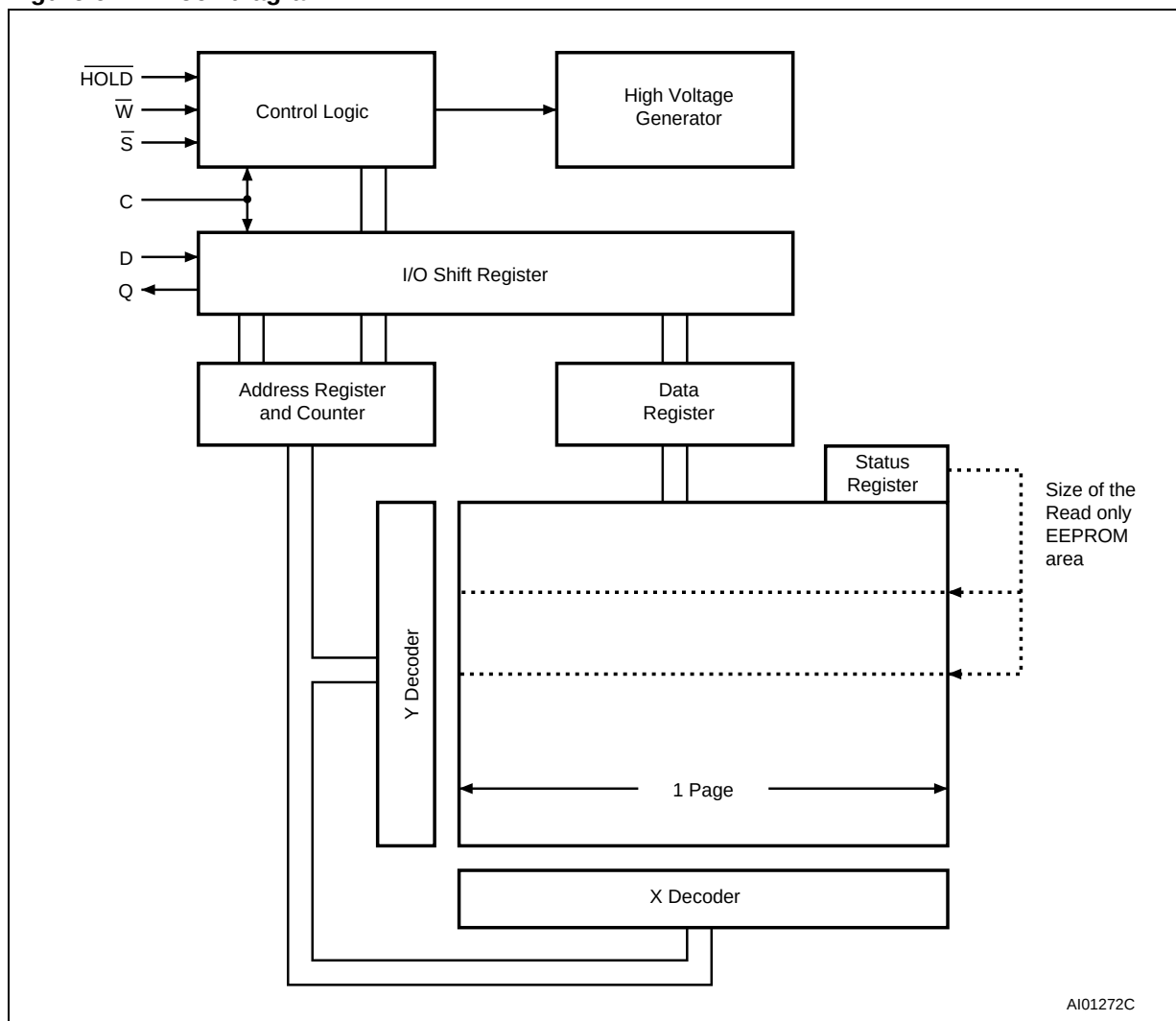
Table 3. Write-Protected block size

Status Register Bits		Protected Block	Array Addresses Protected	
BP1	BP0		M95160	M95080
0	0	none	none	none
0	1	Upper quarter	0600h - 07FFh	0300h - 03FFh
1	0	Upper half	0400h - 07FFh	0200h - 03FFh
1	1	Whole memory	0000h - 07FFh	0000h - 03FFh

5 Memory organization

The memory is organized as shown in [Figure 6](#).

Figure 6. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in [Table 4](#).
 If an invalid instruction is sent (one not contained in [Table 4](#)), the device automatically deselects itself.

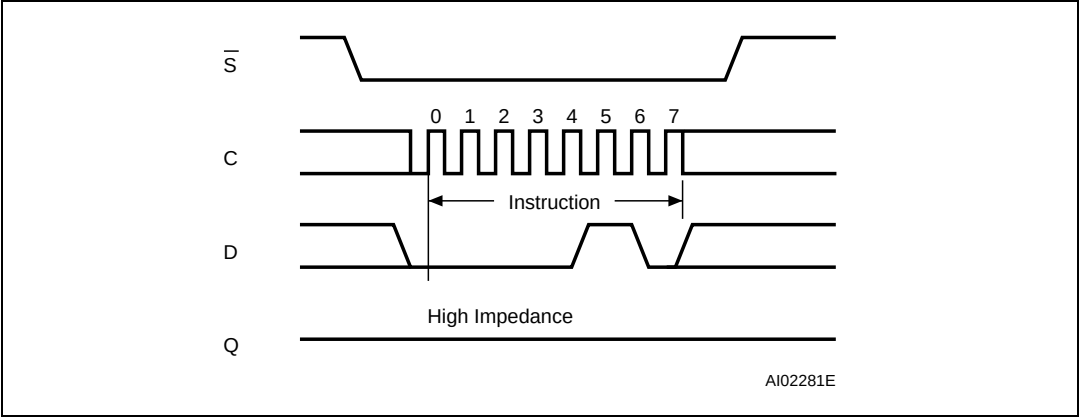
Table 4. Instruction set

Instruction	Description	Instruction Format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.
 As shown in [Figure 7](#), to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

Figure 7. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

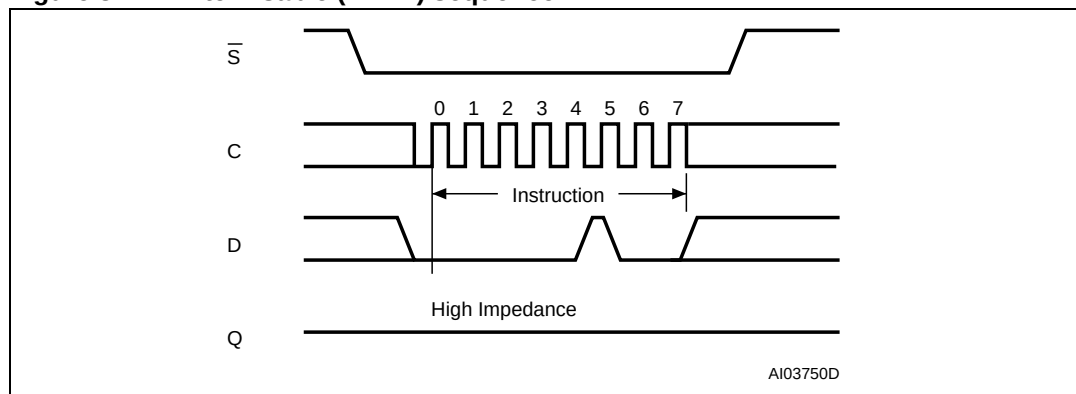
As shown in [Figure 8](#), to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in [Figure 9](#).

The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in [Table 5](#)) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

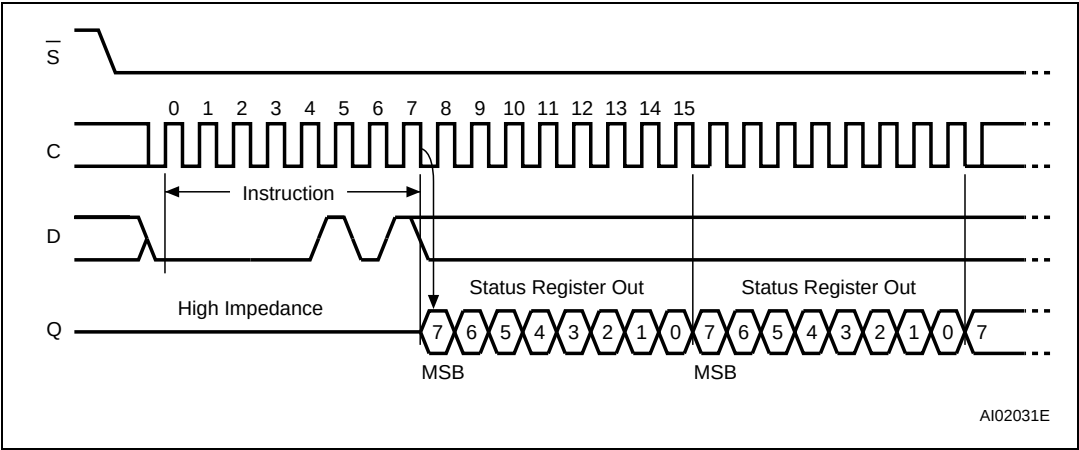
6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 5. Status Register format

b7				b0			
SRWD	0	0	0	BP1	BP0	WEL	WIP
Status Register Write Protect				Block Protect Bits		Write Enable Latch Bit	Write In Progress Bit

Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on Serial Data Input (D). The instruction is terminated by driving Chip Select ($\overline{S}$) High at a byte boundary of the input data. The self-timed Write cycle then starts, and continues for a period t_W (as specified in [Table 19](#), [Table 20](#), [Table 21](#), [Table 22](#) and [Table 23](#)), at the end of which the Write in Progress (WIP) bit is reset to 0. The instruction sequence is shown in [Figure 10](#).

The Write Status Register (WRSR) instruction has no effect on b6, b5, b4, b1 and b0 of the Status Register. b6, b5 and b4 are always read as 0.

Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in [Table 5](#).

The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

The contents of the Status Register Write Disable (SRWD) and Block Protect (BP1, BP0) bits are frozen at their current values from just before the start of the execution of Write Status Register (WRSR) instruction. The new, updated, values take effect at the moment of completion of the execution of Write Status Register (WRSR) instruction.

Table 6. Protection modes

$\overline{W}$ Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory content	
				Protected area ⁽¹⁾	Unprotected area ⁽¹⁾
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write Protected	Ready to accept Write instructions
0	0				
1	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Write Protected	Ready to accept Write instructions
0	1				

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in [Table 6](#).

The protection features of the device are summarized in [Table 3](#).

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of whether Write Protect ($\overline{W}$) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect ($\overline{W}$) is driven Low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low
- or by driving Write Protect ($\overline{W}$) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

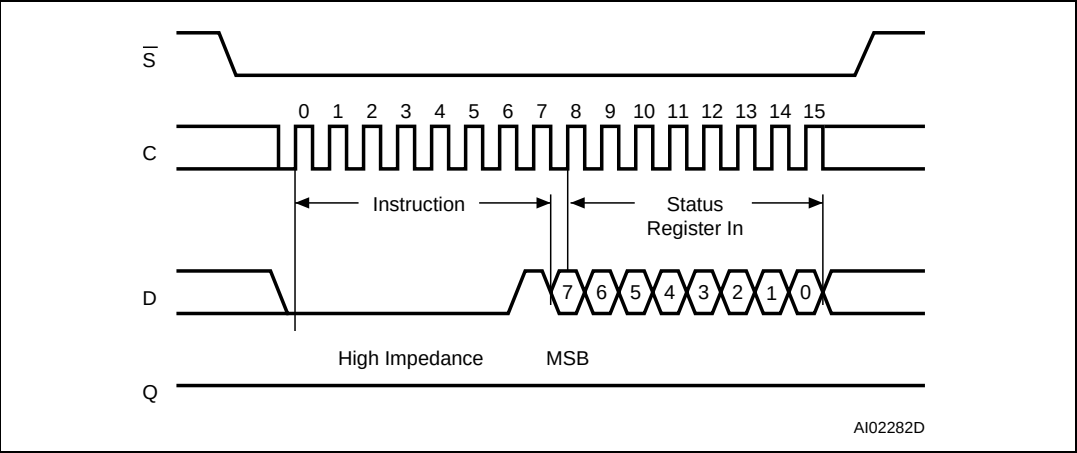
If Write Protect ($\overline{W}$) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP1, BP0) bits of the Status Register, can be used.

Table 7. Address range bits⁽¹⁾

Device	M95160	M95080
Address Bits	A10-A0	A9-A0

1. b15 to b11 are Don't Care on the M95160.
b15 to b10 are Don't Care on the M95080.

Figure 10. Write Status Register (WRSR) sequence



6.5 Read from Memory Array (READ)

As shown in [Figure 11](#), to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven Low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

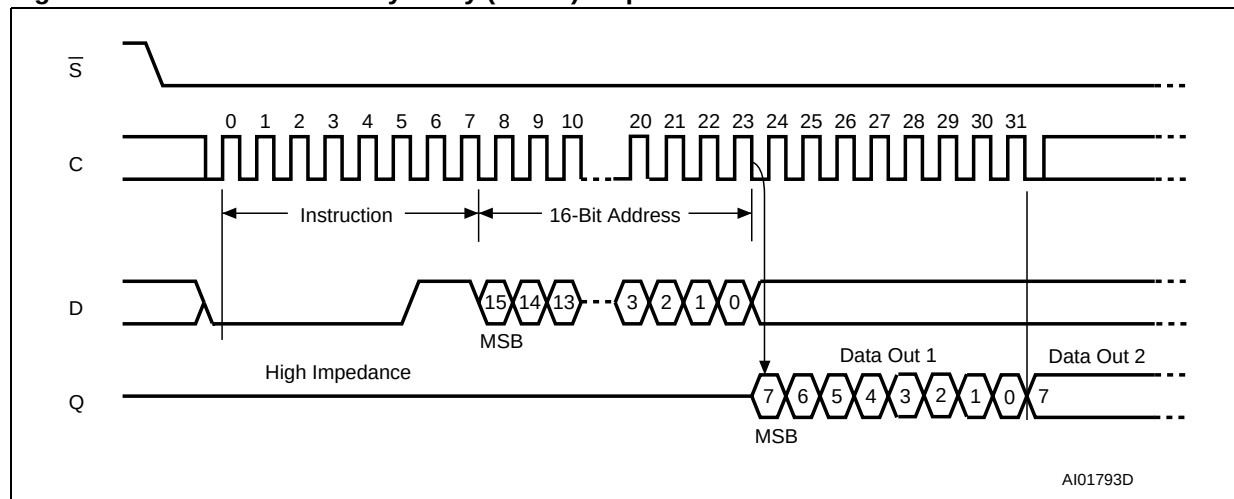
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) High. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in [Table 7](#), the most significant address bits are Don't Care.

6.6 Write to Memory Array (WRITE)

As shown in [Figure 12.](#), to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High at a byte boundary of the input data. In the case of [Figure 12.](#), this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts, and continues for a period t_{WC} (as specified in [Table 20.](#) to [Table 23.](#)), at the end of which the Write in Progress (WIP) bit is reset to 0.

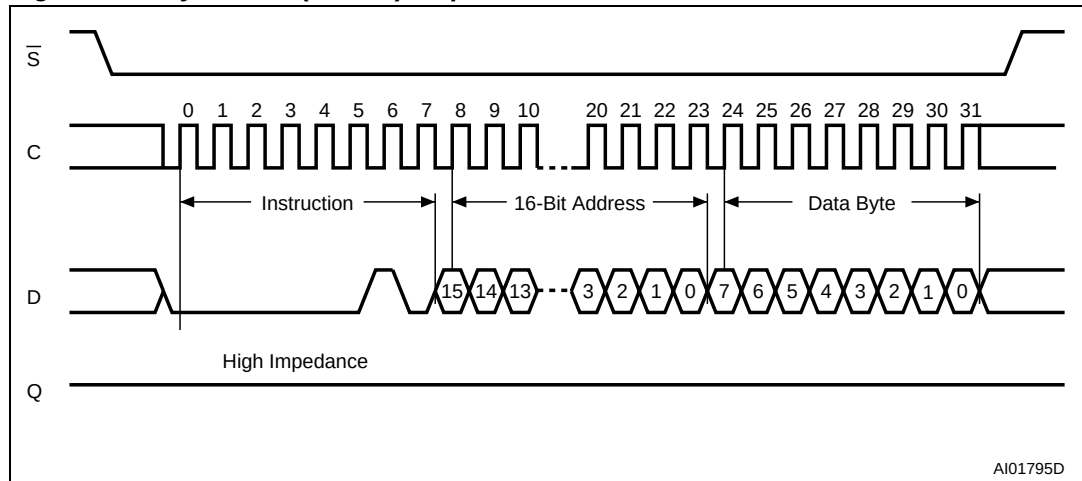
If, though, Chip Select ($\overline{S}$) continues to be driven Low, as shown in [Figure 13.](#), the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

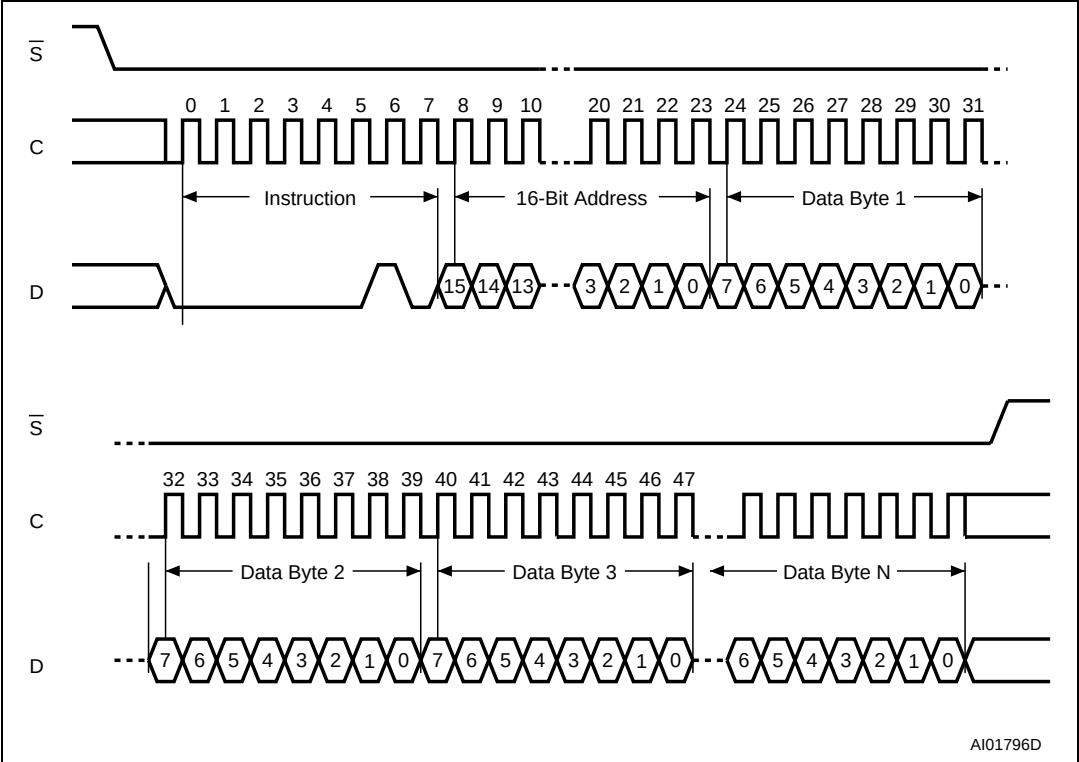
- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in [Table 7.](#), the most significant address bits are Don't Care.

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in [Table 7.](#), the most significant address bits are Don't Care.

7 Delivery state

7.1 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in [Table 8](#), may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	−40	130	
T_{STG}	Storage temperature	−65	150	°C
T_{LEAD}	Lead temperature during soldering	See note ⁽¹⁾		°C
V_O	Output voltage	−0.50	$V_{CC}+0.6$	V
V_I	Input voltage	−0.50	6.5	V
V_{CC}	Supply voltage	−0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model) ⁽²⁾	−4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK[®] 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU

2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100 pF, R1=1500 Ω , R2=500 Ω)

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the dc and ac characteristics of the device. The parameters in the dc and ac characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 9. Operating conditions (M95160 and M95080)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	-40	85	°C
	Ambient operating temperature (device grade 3)	-40	125	°C

Table 10. Operating conditions (M95160-W and M95080-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	-40	85	°C
	Ambient operating temperature (device grade 3)	-40	125	°C

Table 11. Operating conditions (M95160-R and M95080-R)

Symbol	Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	-40	85	°C

1. This product is under development. For more information, please contact your nearest ST sales office.

Table 12. AC measurement conditions⁽¹⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_L	Load capacitance		30		pF
	Input rise and fall times			50	ns
	Input pulse voltages	0.2V _{CC} to 0.8V _{CC}			V
	Input and output timing reference voltages	0.3V _{CC} to 0.7V _{CC}			V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 14. AC measurement I/O waveform

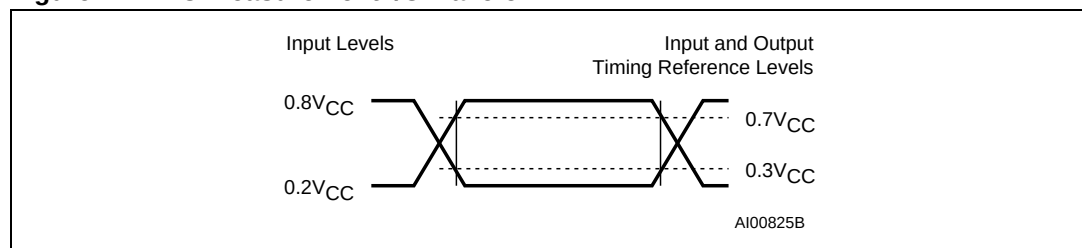


Table 13. Capacitance⁽¹⁾

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	$V_{OUT} = 0\text{ V}$		8	pF
C_{IN}	Input capacitance (D)	$V_{IN} = 0\text{ V}$		8	pF
	Input capacitance (other pins)	$V_{IN} = 0\text{ V}$		6	pF

1. Sampled only, not 100% tested, at $T_A = 25\text{ °C}$ and a frequency of 5 MHz.

Table 14. DC characteristics (M95160 and M95080, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	μA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	μA
I_{CC}	Supply current	$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 5\text{ V}$, Q = open		3	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, $V_{CC} = 5\text{ V}$, $V_{IN} = V_{SS}$ or V_{CC}		5	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
$V_{OL}^{(1)}$	Output low voltage	$I_{OL} = 2\text{ mA}$, $V_{CC} = 5\text{ V}$		0.4	V
$V_{OH}^{(1)}$	Output high voltage	$I_{OH} = -2\text{ mA}$, $V_{CC} = 5\text{ V}$	$0.8 V_{CC}$		V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 15. DC characteristics (M95160 and M95080, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	μA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	μA
I_{CC}	Supply current	$C = 0.1V_{CC}/0.9V_{CC}$ at 10 MHz, $V_{CC} = 5\text{ V}$, Q = open		5	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, $V_{CC} = 5\text{ V}$, $V_{IN} = V_{SS}$ or V_{CC}		2	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
$V_{OL}^{(1)}$	Output low voltage	$I_{OL} = 2\text{ mA}$, $V_{CC} = 5\text{ V}$		0.4	V
$V_{OH}^{(1)}$	Output high voltage	$I_{OH} = -2\text{ mA}$, $V_{CC} = 5\text{ V}$	$0.8 V_{CC}$		V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 16. DC characteristics (M95160-W and M95080-W, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	μA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	μA
I_{CC}	Supply current	$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 2.5$ V, Q = open		2	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, $V_{CC} = 2.5$ V, $V_{IN} = V_{SS}$ or V_{CC}		2	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 1.5$ mA, $V_{CC} = 2.5$ V		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -0.4$ mA, $V_{CC} = 2.5$ V	$0.8 V_{CC}$		V

Table 17. DC characteristics (M95160-W and M95080-W, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	μA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	μA
I_{CC}	Supply current	$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 2.5$ V, Q = open, Process SA		2	mA
		$C = 0.1V_{CC}/0.9V_{CC}$ at 10 MHz, $V_{CC} = 2.5$ V, Q = open, Process GB or SB		5	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, $2.5 V < V_{CC} < 5.5 V$ $V_{IN} = V_{SS}$ or V_{CC}		2	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 1.5$ mA, $V_{CC} = 2.5$ V		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -0.4$ mA, $V_{CC} = 2.5$ V	$0.8 V_{CC}$		V

Table 18. DC characteristics (M95160-R and M95080-R)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}, V_{OUT} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{CC}	Supply current	$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 1.8 \text{ V}$, Q = open		3	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC},$ $1.8 < V_{CC} < 2.5 \text{ V}$		1	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 0.15 \text{ mA}, V_{CC} = 1.8 \text{ V}$		0.3	V
V_{OH}	Output high voltage	$I_{OH} = -0.1 \text{ mA}, V_{CC} = 1.8 \text{ V}$	$0.8 V_{CC}$		V

Table 19. AC characteristics (M95160 and M95080, device grade 3)

Test conditions specified in Table 12. and Table 9.					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
$t_{CH}^{(1)}$	t_{CLH}	Clock high time	90		ns
$t_{CL}^{(1)}$	t_{CLL}	Clock low time	90		ns
$t_{CLCH}^{(2)}$	t_{RC}	Clock rise time		1	μs
$t_{CHCL}^{(2)}$	t_{FC}	Clock fall time		1	μs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
$t_{SHQZ}^{(2)}$	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(2)}$	t_{RO}	Output rise time		50	ns
$t_{QHQL}^{(2)}$	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
$t_{HLQZ}^{(2)}$	t_{HZ}	$\overline{HOLD}$ low to output High-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C(\max)$.

2. Value guaranteed by characterization, not 100% tested in production.

Table 20. AC characteristics (M95160 and M95080, device grade 6)

Test conditions specified in Table 12. and Table 9.					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	25		ns
t_{CHSL}		$\overline{S}$ not active hold time	15		ns
$t_{CH}^{(1)}$	t_{CLH}	Clock high time	40		ns
$t_{CL}^{(1)}$	t_{CLL}	Clock low time	40		ns
$t_{CLCH}^{(2)}$	t_{RC}	Clock rise time		1	μs
$t_{CHCL}^{(2)}$	t_{FC}	Clock fall time		1	μs
t_{DVCH}	t_{DSU}	Data in setup time	15		ns
t_{CHDX}	t_{DH}	Data in hold time	15		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	20		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
$t_{SHQZ}^{(2)}$	t_{DIS}	Output disable time		25	ns
t_{CLQV}	t_V	Clock low to output valid		35	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(2)}$	t_{RO}	Output rise time		20	ns
$t_{QHQL}^{(2)}$	t_{FO}	Output Fall Time		20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		25	ns
$t_{HLQZ}^{(2)}$	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		35	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C(\max)$.

2. Value guaranteed by characterization, not 100% tested in production.

Table 21. AC characteristics (M95160-W and M95080-W, device grade 3)

Test conditions specified in Table 12. and Table 10.					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
$t_{CH}^{(1)}$	t_{CLH}	Clock high time	90		ns
$t_{CL}^{(1)}$	t_{CLL}	Clock low time	90		ns
$t_{CLCH}^{(2)}$	t_{RC}	Clock rise time		1	μs
$t_{CHCL}^{(2)}$	t_{FC}	Clock fall time		1	μs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
$t_{SHQZ}^{(2)}$	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(2)}$	t_{RO}	Output rise time		50	ns
$t_{QHQL}^{(2)}$	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
$t_{HLQZ}^{(2)}$	t_{HZ}	$\overline{HOLD}$ low to output High-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C(\max)$.

2. Value guaranteed by characterization, not 100% tested in production.

Table 22. AC characteristics (M95160-W and M95080-W, device grade 6)

Test conditions specified in Table 12. and Table 10.							
Symbol	Alt.	Parameter	Process SA		Process GB or SB ⁽¹⁾		Unit
			Min.	Max.	Min.	Max.	
f_C	f_{SCK}	Clock frequency	D.C.	5	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		30		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		30		ns
$t_{CH}^{(2)}$	t_{CLH}	Clock high time	90		40		ns
$t_{CL}^{(2)}$	t_{CLL}	Clock low time	90		40		ns
$t_{CLCH}^{(3)}$	t_{RC}	Clock rise time		1		2	μs
$t_{CHCL}^{(3)}$	t_{FC}	Clock fall time		1		2	μs
t_{DVCH}	t_{DSU}	Data in setup time	20		10		ns
t_{CHDX}	t_{DH}	Data in hold time	30		10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		30		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0		ns
$t_{SHQZ}^{(3)}$	t_{DIS}	Output disable time		100		40	ns
t_{CLQV}	t_V	Clock low to output valid		60		40	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		ns
$t_{QLQH}^{(3)}$	t_{RO}	Output rise time		50		40	ns
$t_{QHQL}^{(3)}$	t_{FO}	Output fall time		50		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50		40	ns
$t_{HLQZ}^{(3)}$	t_{HZ}	$\overline{HOLD}$ low to output High-Z		100		40	ns
t_W	t_{WC}	Write time		5		5	ms

1. Preliminary data

2. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C(\max)$.

3. Value guaranteed by characterization, not 100% tested in production.

Table 23. AC characteristics (M95160-R and M95080-R)

Test conditions specified in Table 12. and Table 11.					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60		ns
t_{CHSL}		$\overline{S}$ not active hold time	60		ns
$t_{CH}^{(1)}$	t_{CLH}	Clock high time	80		ns
$t_{CL}^{(1)}$	t_{CLL}	Clock low time	80		ns
$t_{CLCH}^{(2)}$	t_{RC}	Clock rise time		2	μs
$t_{CHCL}^{(2)}$	t_{FC}	Clock fall time		2	μs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	20		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0
$t_{SHQZ}^{(2)}$	t_{DIS}	Output disable time		80	ns
t_{CLQV}	t_V	Clock low to output valid		80	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(2)}$	t_{RO}	Output rise time		80	ns
$t_{QHQL}^{(2)}$	t_{FO}	Output fall time		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		80	ns
$t_{HLQZ}^{(2)}$	t_{HZ}	$\overline{HOLD}$ low to output High-Z		80	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C(\max)$.

2. Value guaranteed by characterization, not 100% tested in production.

Figure 15. Serial input timing

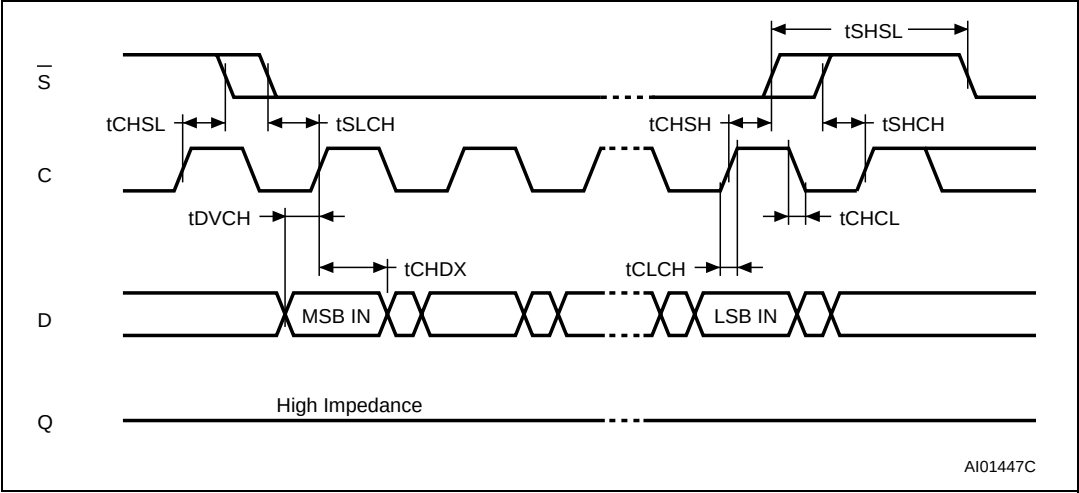


Figure 16. Hold timing

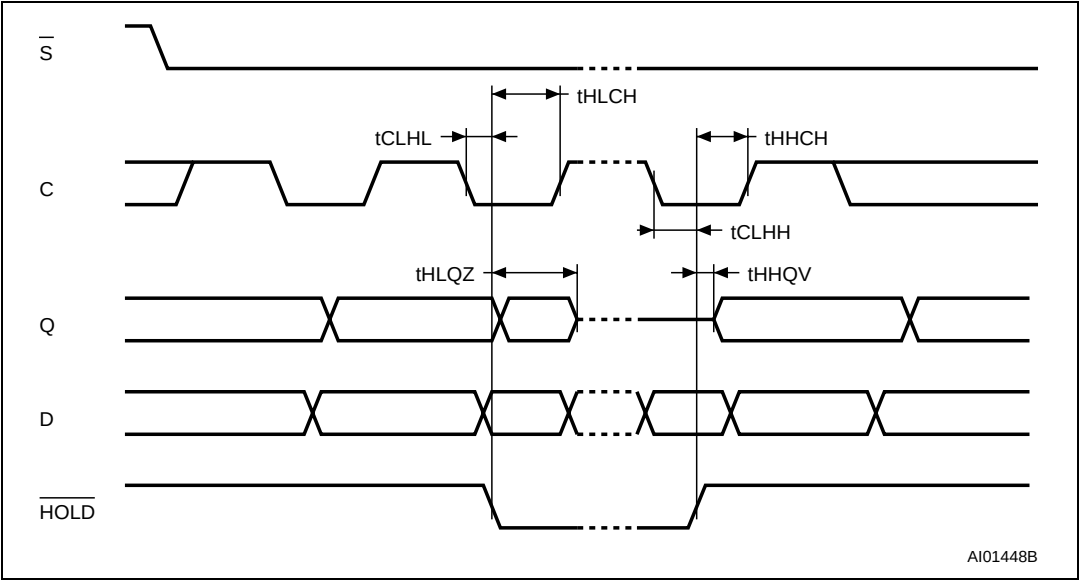
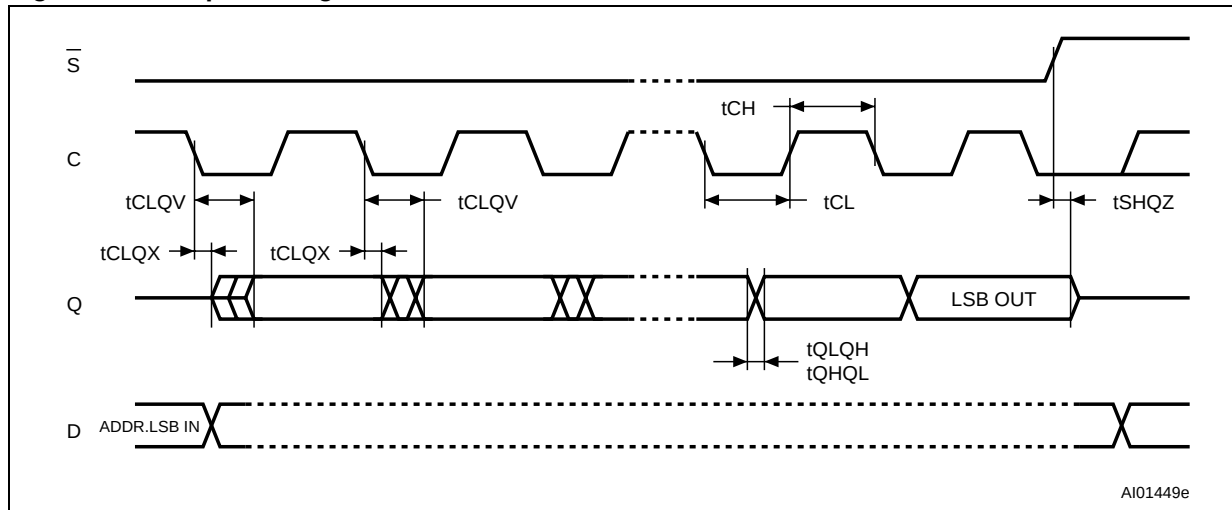
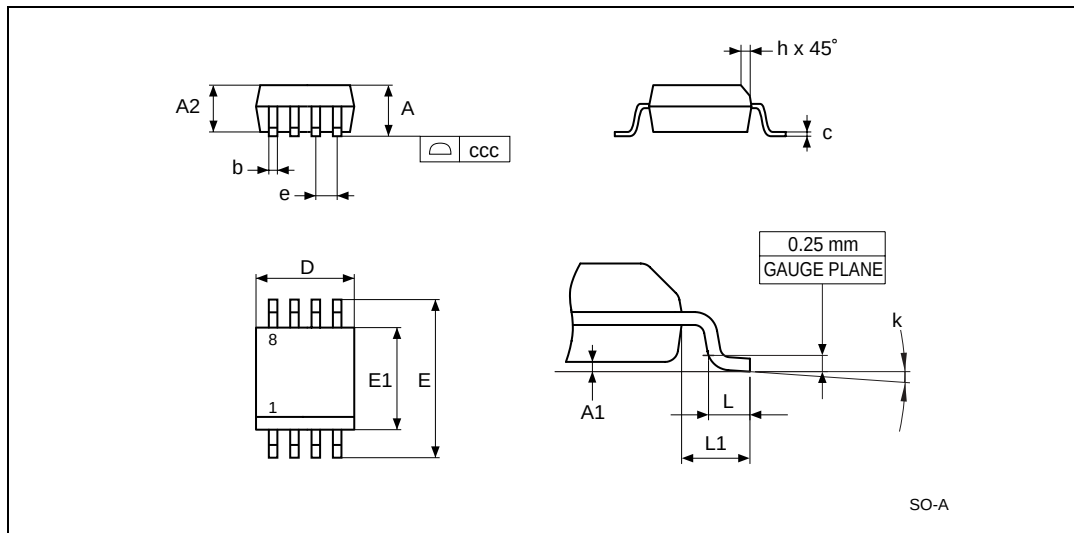


Figure 17. Output timing



10 Package mechanical

Figure 18. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, package outline

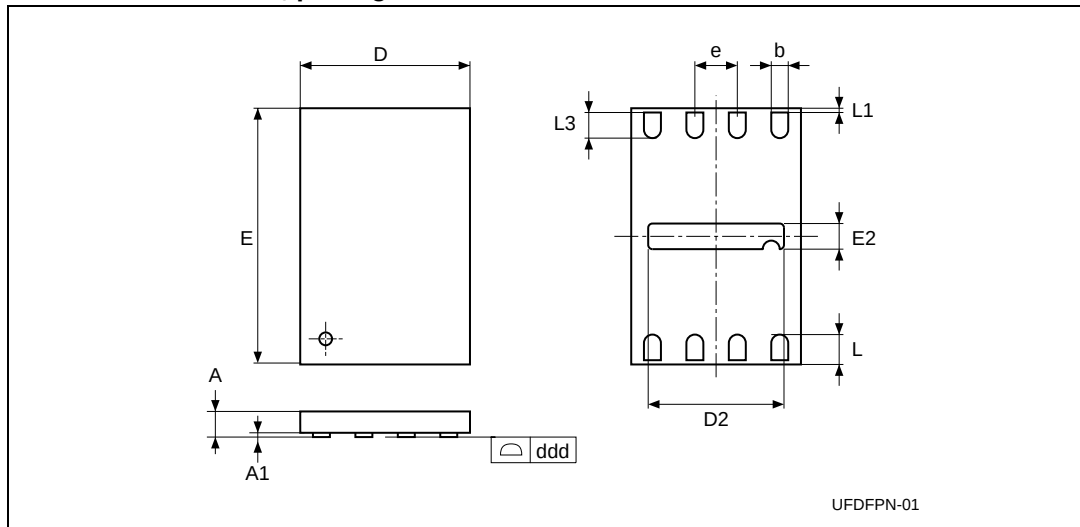


1. Drawing is not to scale.

Table 24. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

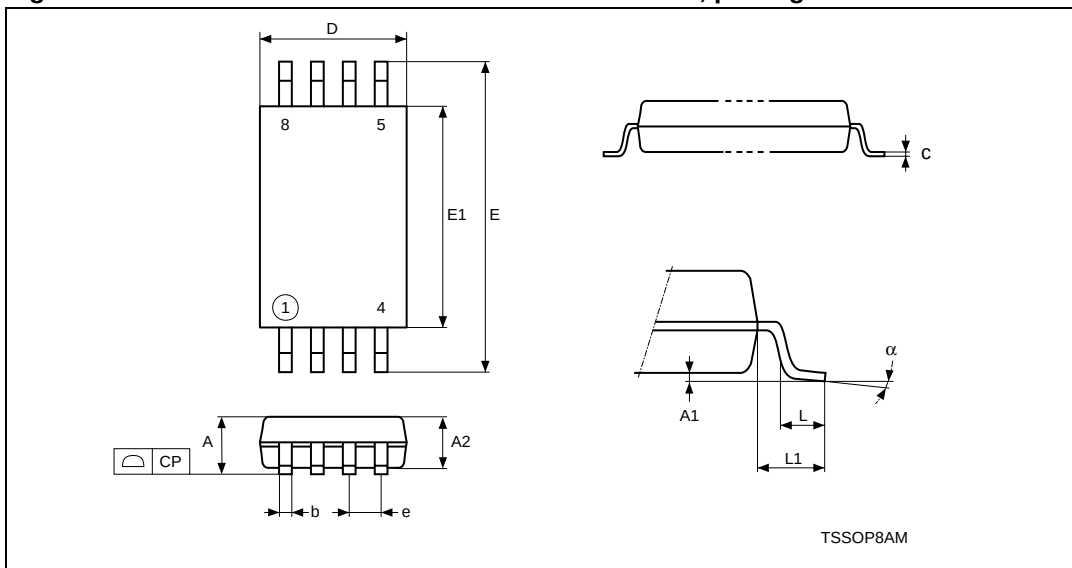
**Figure 19. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead
2 x 3 mm², package outline**



1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is pulled, internally, to V_{SS} . It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.

**Table 25. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead
2 x 3 mm, package mechanical data**

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.50	0.60	0.022	0.020	0.024
A1	0.02	0.00	0.05	0.001	0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00	1.90	2.10	0.079	0.075	0.083
D2	1.60	1.50	1.70	0.063	0.059	0.067
ddd			0.08			0.003
E	3.00	2.90	3.10	0.118	0.114	0.122
E2	0.20	0.10	0.30	0.008	0.004	0.012
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	

Figure 20. TSSOP8 – 8 lead Thin Shrink Small Outline, package outline

1. Drawing is not to scale.

Table 26. TSSOP8 – 8 lead Thin Shrink Small Outline, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

11 Part numbering

Table 27. Ordering information scheme

Example:	M95160	–	W	MN	6	T	P	/S
Device type								
M95 = SPI serial access EEPROM								
Device function								
160 = 16 Kbit (2048 x 8)								
080 = 8 Kbit (1024 x 8)								
Operating voltage								
blank = $V_{CC} = 4.5$ to 5.5 V								
W = $V_{CC} = 2.5$ to 5.5 V								
R = $V_{CC} = 1.8$ to 5.5 V								
Package								
MN = SO8 (150 mil width)								
DW = TSSOP8								
MB = MLP8 (UFDFPN8)								
Device grade								
6 = Industrial temperature range, -40 to 85 °C.								
Device tested with standard test flow								
3 = Device tested with High Reliability Certified Flow ⁽¹⁾ .								
Automotive temperature range (-40 to 125 °C)								
Option								
blank = Standard Packing								
T = Tape and Reel Packing								
Plating technology								
G or P = ECOPACK® (RoHS compliant)								
Process⁽²⁾								
/G or /S = F6SP36%								

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. The Process letter (/G or /S) applies only to Range 3 devices. For Range 6 devices, the process letters do not appear in the Ordering Information but only appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office. For more information on how to identify products by the Process Identification Letter, please refer to AN2043: Serial EEPROM Device Marking.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Table 28. Available M95160 products (package, voltage range, temperature grade)

Package	M95160 4.5 V to 5.5 V	M95160-W 2.5 V to 5.5 V	M95160-R 1.8 V to 5.5 V
SO8 (MN)	Range 6 Range3	Range 6 Range3	Range 6
TSSOP (DW)	NA ⁽¹⁾	Range 6 Range3	Range 6
MLP 2x3mm (MB)	NA ⁽¹⁾	NA ⁽¹⁾	Range 6

1. NA = Not available

Table 29. Available M95080 products (package, voltage range, temperature grade)

Package	M95080 4.5 V to 5.5 V	M95080-W 2.5 V to 5.5 V	M95080-R 1.8 V to 5.5 V
SO8 (MN)	Range 6 Range3	Range 6 Range3	Range 6
TSSOP (DW)	NA ⁽¹⁾	Range 6 Range3	Range 6
MLP 2x3mm (MB)	NA ⁽¹⁾	Range 6	Range 6

1. NA = Not available

12 Revision history

Table 30. Document revision history

Date	Revision	Changes
19-Jul-2001	1.0	Document written from previous M95640/320/160/080 datasheet
06-Feb-2002	1.1	Announcement made of planned upgrade to 10MHz clock for the 5V, –40 to 85°C, range
18-Oct-2002	1.2	TSSOP8 (3x3mm body size, MSOP8) package added
04-Nov-2002	1.3	New products, identified by the process letter W, added
13-Nov-2002	1.4	Correction to footnote in Ordering Information table
21-Nov-2003	2.0	Table of contents, and Pb-free options added. $V_{IL}(\text{min})$ improved to –0.45V
08-Jun-2004	3.0	MLP8 package added. Absolute Maximum Ratings for $V_{IO}(\text{min})$ and $V_{CC}(\text{min})$ improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade 3 clarified, with reference to HRCF and automotive environments. Process identification letter “G” information added. SO8 narrow and TSSOP8 Package mechanical specifications updated.
07-Oct-2004	4.0	Product List summary table added. AEC-Q100-002 compliance. tHHQX corrected to tHHQV. 10MHz, 5ms Write is now the present product. tCH+tCL<1/fC constraint clarified
21-Sep-2005	5.0	Added 20MHz and -S product information. Removed DIP package. Info on Pull-up resistors, VCC lines and Note 2. added to Figure 4.: Bus master and memory devices on the SPI bus . Device internal reset paragraph clarified. Packages compliant with the JEDEC Std J-STD-020C. Process info updated in DC and AC parameters and Table 27.: Ordering information scheme .

Table 30. Document revision history

Date	Revision	Changes
24-May-2007	6	Document reformatted. Small text changes. TSSOP8 3 x 3 mm (DS) package removed, 1.65 V to 5.5 V operating voltage range removed (M95080-S and M95160-S removed). Figure 4: Bus master and memory devices on the SPI bus updated, note 2 removed and explanatory paragraph added (see Section 3: Connecting to the SPI bus). Section 2.7: VCC supply voltage and Section 2.8: VSS ground added. Power-up, Device Internal Reset and Power-down replaced by Section 4.1: Supply voltage (VCC). Command termination specified in Section 6.4: Write Status Register (WRSR). Blank process no longer available for M95160, M95080, M95160-W and M95080-W in the device grade 3 range. L, GB and SB processes no longer available for M95160 and M95080, in the device grade 6 range. L process no longer available for M95160-W and M95080-W in the device grade 6 range. I_{CC1} value and test conditions modified in Table 18: DC characteristics (M95160-R and M95080-R). End timing line of t_{SHQZ} modified in Figure 17: Output timing. SO8N and UDFPN8 package specifications updated. All packages are ECOPACK® compliant. Blank option removed below Plating technology and Note 2 modified in Table 27: Ordering information scheme. Table 28: Available M95160 products (package, voltage range, temperature grade) and Table 29: Available M95080 products (package, voltage range, temperature grade) added.

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