

MAC97A8; MAC97A6

Logic level triac

Rev. 01 — 29 March 2001

Product specification

1. Description

Logic level sensitive gate triac intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

Product availability:

MAC97A8 in SOT54 (TO-92)

MAC97A6 in SOT54 (TO-92) available on request - contact your sales representative.

2. Features

- Blocking voltage to 600 V (MAC97A8)
- RMS on-state current to 0.6 A
- Sensitive gate in all four quadrants
- Low cost package.

3. Applications

- General purpose bidirectional switching
- Phase control applications
- Solid state relays.

4. Pinning information

Table 1: Pinning - SOT54 (TO-92), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	main terminal 2	SOT54 (TO-92)	
2	gate		
3	main terminal 1		

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage				
	MAC97A8	$T_j = 25 \text{ to } 125 \text{ }^\circ\text{C}$	–	600	V
	MAC97A6	$T_j = 25 \text{ to } 125 \text{ }^\circ\text{C}$	–	400	V
$I_{\text{T(RMS)}}$	on-state current (RMS value)	full sine wave; $T_{\text{lead}} \leq 50 \text{ }^\circ\text{C}$; Figure 5	–	0.6	A
I_{TSM}	non-repetitive peak on-state current		–	8.0	A

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

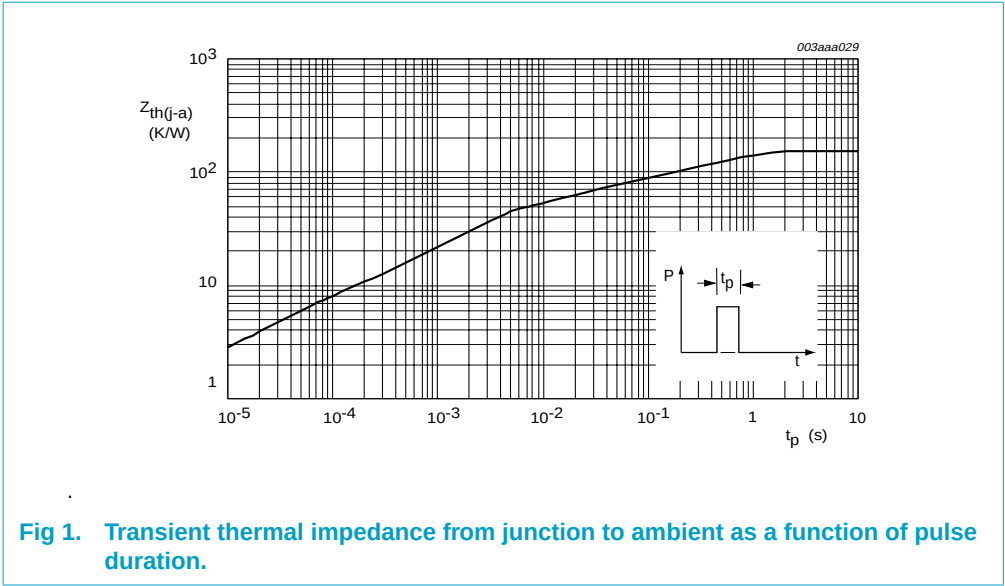
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage				
	MAC97A8	$T_j = 25 \text{ to } 125 \text{ }^\circ\text{C}$	–	600	V
	MAC97A6	$T_j = 25 \text{ to } 125 \text{ }^\circ\text{C}$	–	400	V
$I_{\text{T(RMS)}}$	on-state current (RMS value)	full sine wave; $T_{\text{lead}} \leq 50 \text{ }^\circ\text{C}$; Figure 5	–	0.6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_j = 25 \text{ }^\circ\text{C}$ prior to surge			
		$t = 20 \text{ ms}$	–	8.0	A
		$t = 16.7 \text{ ms}$	–	8.8	A
I^2t	I^2t for fusing	$t = 10 \text{ ms}$	–	0.32	A ² s
di_T/dt	repetitive rate of rise of on-state current after triggering	$I_{\text{TM}} = 1.0 \text{ A}$; $I_G = 0.2 \text{ A}$; $di_G/dt = 0.2 \text{ A}/\mu\text{s}$			
		T2+ G+	–	50	A/ μs
		T2+ G–	–	50	A/ μs
		T2– G–	–	50	A/ μs
		T2– G+	–	10	A/ μs
I_{GM}	gate current (peak value)	$t = 2 \text{ } \mu\text{s}$ max	–	1	A
V_{GM}	gate voltage (peak value)	$t = 2 \text{ } \mu\text{s}$ max		5	V
P_{GM}	gate power (peak value)	$t = 2 \text{ } \mu\text{s}$ max	–	5	W
$P_{\text{G(AV)}}$	average gate power	$T_{\text{case}} = 80 \text{ }^\circ\text{C}$; $t = 2 \text{ } \mu\text{s}$ max	–	0.1	W
T_{stg}	storage temperature		–40	+150	$^\circ\text{C}$
T_j	operating junction temperature		–40	+125	$^\circ\text{C}$

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle	60	K/W
		half cycle	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; lead length = 4 mm; Figure 1	150	K/W

7.1 Transient thermal impedance

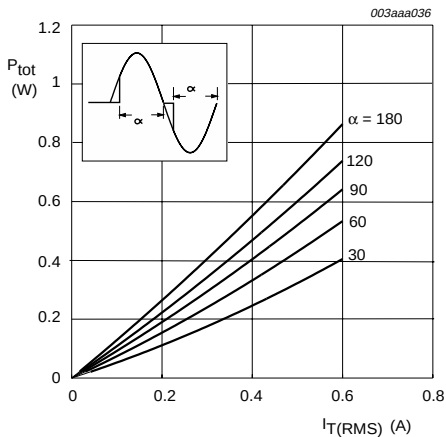


8. Characteristics

Table 5: Characteristics

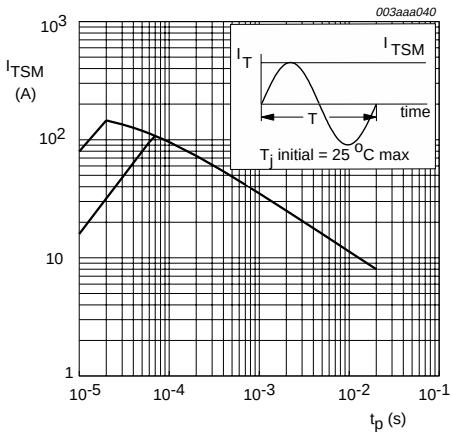
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; Figure 8				
		T2+ G+	–	1	5	mA
		T2+ G–	–	2	5	mA
		T2– G–	–	2	5	mA
		T2– G+	–	4	7	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$; Figure 9				
		T2+ G+	–	1	10	mA
		T2+ G–	–	5	10	mA
		T2– G–	–	1	10	mA
		T2– G+	–	2	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$; Figure 10	–	1	10	mA
V_T	on-state voltage	$I_T = 0.85\text{ A}$; Figure 11	–	1.4	1.9	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; Figure 7	–	0.9	2	V
		$V_D = V_{DRM}$; $I_T = 0.1\text{ A}$; $T_j = 110\text{ }^{\circ}\text{C}$	0.1	0.7	–	V
I_D	off-state leakage current	$V_D = V_{DRM(max)}$; $T_j = 110\text{ }^{\circ}\text{C}$	–	3	100	μA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	$V_D = 67\%$ of $V_{DM(max)}$; $T_{case} = 110\text{ }^{\circ}\text{C}$; exponential waveform; gate open circuit; Figure 12	30	45	–	V/ μs
dV_{com}/dt	critical rate of rise of commutation voltage	$V_D = \text{rated } V_{DRM}$; $T_{case} = 50\text{ }^{\circ}\text{C}$; $I_{TM} = 0.84\text{ A}$; commutating $di/dt = 0.3\text{ A/ms}$	–	5	–	V/ μs
t_{gt}	gate controlled turn-on time	$I_{TM} = 1.0\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 25\text{ mA}$; $di_G/dt = 5\text{ A}/\mu\text{s}$	–	2	–	μs



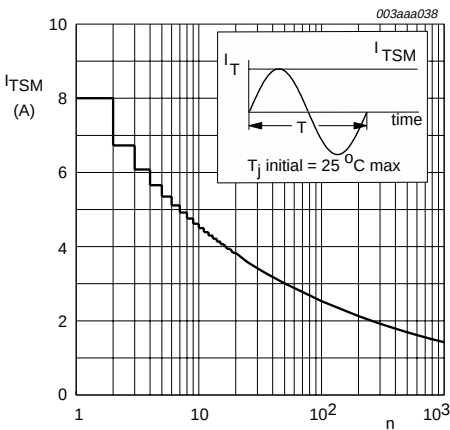
α = conduction angle

Fig 2. Maximum on-state dissipation as a function of RMS on-state current; typical values.



$t_p \leq 20 \text{ ms}$

Fig 3. Maximum permissible non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; typical values.



n = number of cycles at $f = 50 \text{ Hz}$

Fig 4. Maximum permissible non-repetitive peak on-state current as a function of number of cycles for sinusoidal currents; typical values.

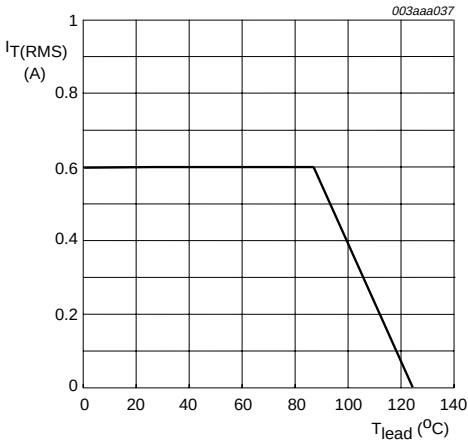
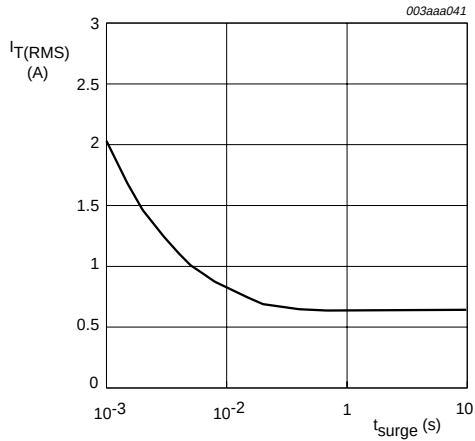
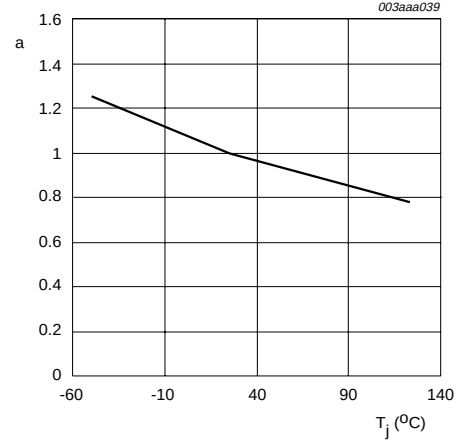


Fig 5. Maximum permissible RMS current as a function of lead temperature; typical values.



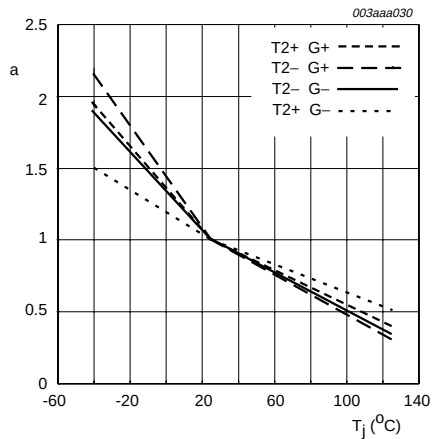
$f = 50 \text{ Hz}$; $T_{\text{lead}} \leq 50^\circ\text{C}$

Fig 6. Maximum permissible repetitive RMS on-state current as a function of surge duration for sinusoidal currents; typical values.



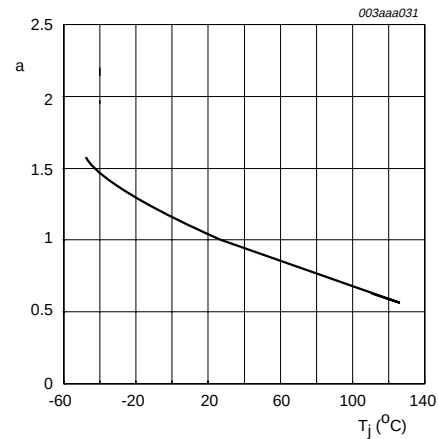
$$a = \frac{V_{GT}(T_j)}{V_{GT}(25^\circ\text{C})}$$

Fig 7. Normalized gate trigger voltage as a function of junction temperature; typical values.



$$a = \frac{I_{GT}(T_j)}{I_{GT}(25^\circ\text{C})}$$

Fig 8. Normalized gate trigger current as a function of junction temperature; typical values.



$$a = \frac{I_L(T_j)}{I_L(25^\circ\text{C})}$$

Fig 9. Normalized latching current as a function of junction temperature; typical values.

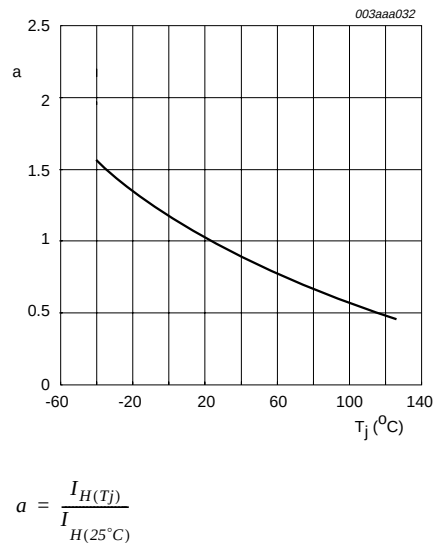


Fig 10. Normalized holding current as a function of junction temperature; typical values.

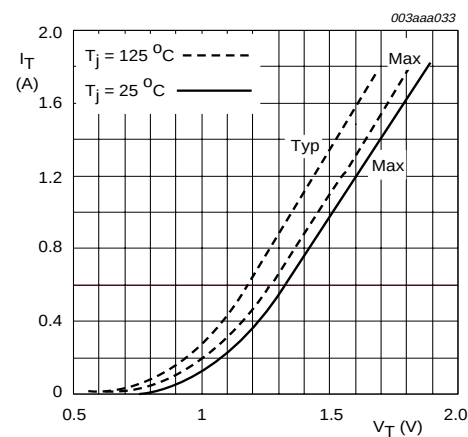


Fig 11. On-state current as a function of on-state voltage; typical and maximum values.

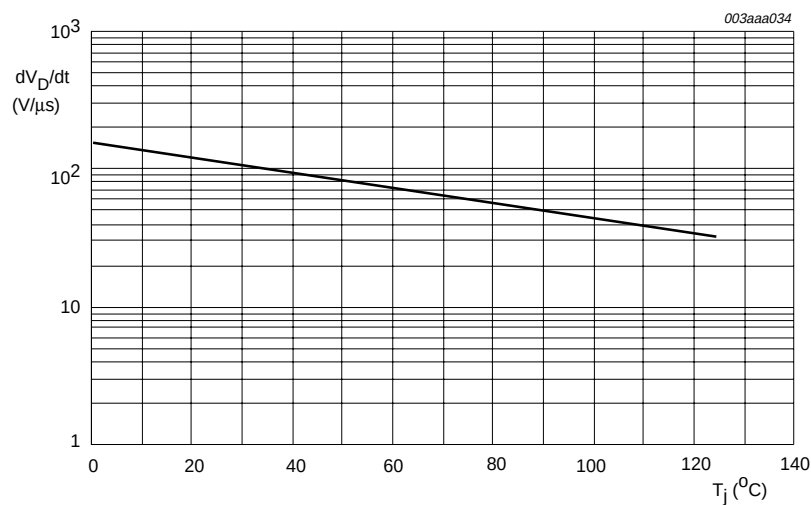
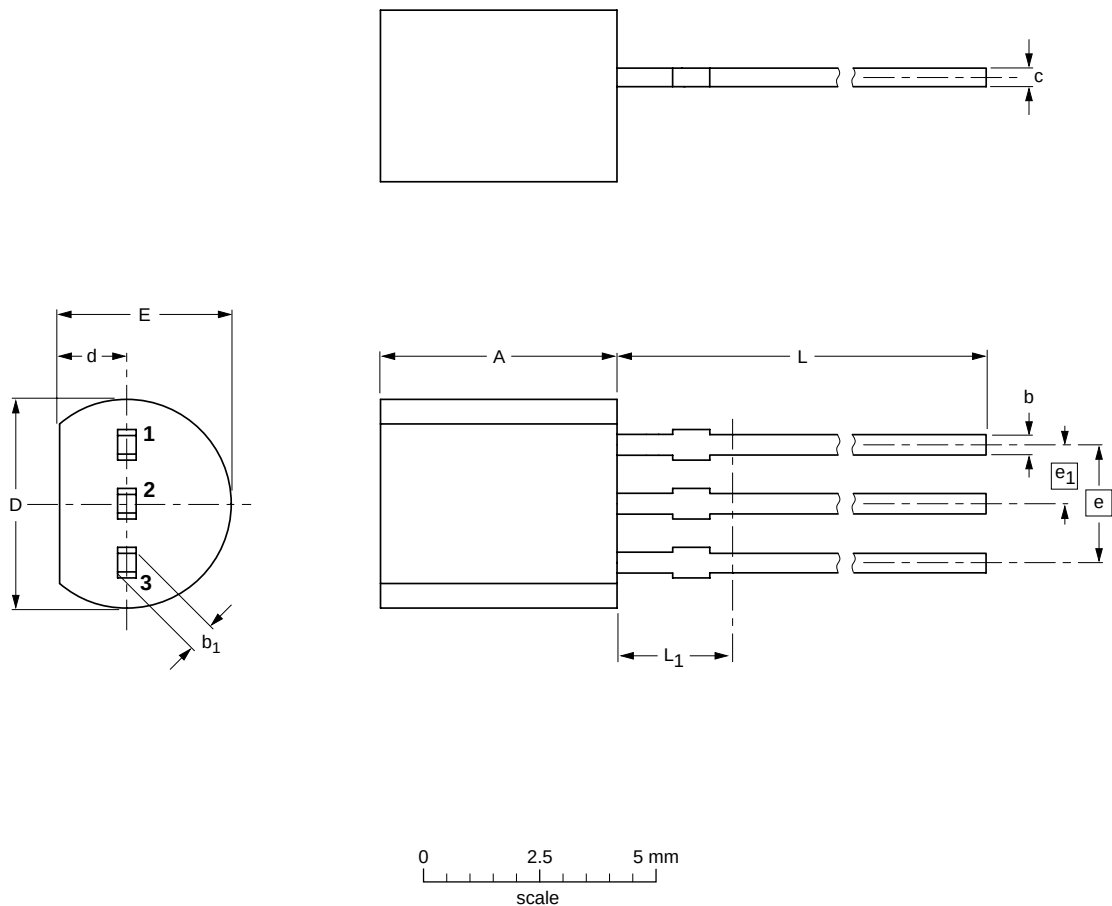


Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values.

9. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Fig 13. SOT54 (TO-92).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010329	-	Product specification; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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(SCA72)

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