

General Description

The AO4420 uses advanced trench technology to provide excellent $R_{DS(ON)}$, shoot-through immunity and body diode characteristics. This device is suitable for use as a synchronous switch in PWM applications.

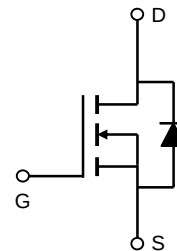
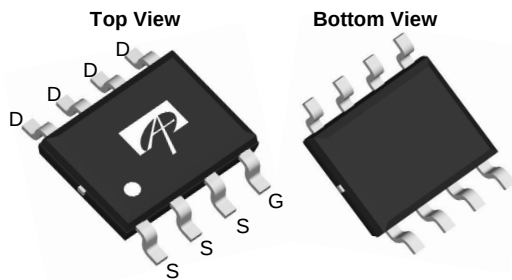
Product Summary

V_{DS} (V) = 30V
 I_D = 13.7A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 10.5m Ω (V_{GS} = 10V)
 $R_{DS(ON)}$ < 12m Ω (V_{GS} = 4.5V)

100% UIS Tested
 100% Rg Tested



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^A	I_D	13.7	A
	$T_A=70^\circ\text{C}$	9.7	
Pulsed Drain Current ^B	I_{DM}	60	
Power Dissipation	P_D	3.1	W
	$T_A=70^\circ\text{C}$	2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	28	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		54	75	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	21	30	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =55°C		0.004	1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.6	1.1	2	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	40			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =13.7A T _J =125°C		8.3 12.5	10.5 15	mΩ
		V _{GS} =4.5V, I _D =12.7A		9.7	12	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =13.7A	30	37		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		3656	4050	pF
C _{oss}	Output Capacitance			256		pF
C _{rss}	Reverse Transfer Capacitance			168		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.86	1.1	Ω
SWITCHING PARAMETERS						
Q _{g(4.5V)}	Total Gate Charge	V _{GS} =4.5V, V _{DS} =15V, I _D =13.7A		30.5	36	nC
Q _{gs}	Gate Source Charge			4.6		nC
Q _{gd}	Gate Drain Charge			8.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.1Ω, R _{GEN} =3Ω		5.5	9	ns
t _r	Turn-On Rise Time			3.4	7	ns
t _{D(off)}	Turn-Off DelayTime			49.8	75	ns
t _f	Turn-Off Fall Time			5.9	11	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =13.7A, dI/dt=100A/μs		22.5	28	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =13.7A, dI/dt=100A/μs		12.5	16	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

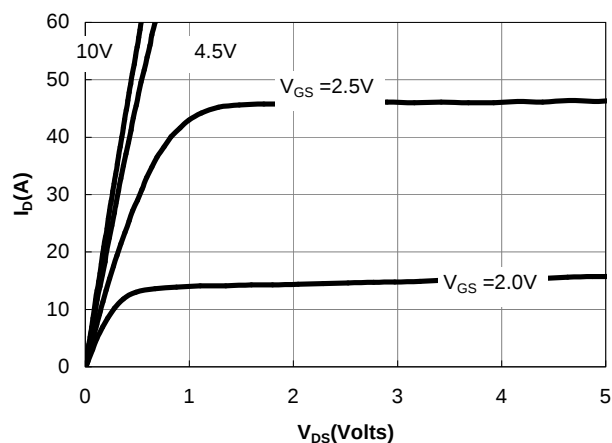


Figure 1: On-Regions Characteristics

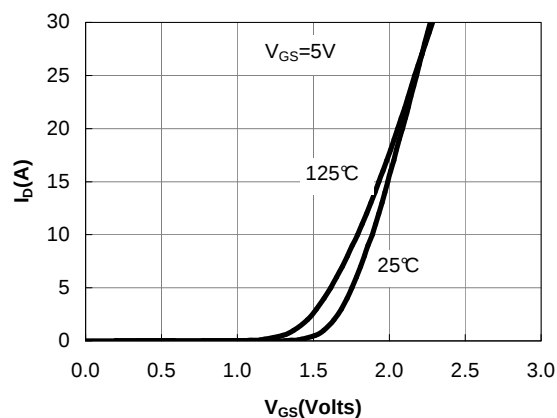


Figure 2: Transfer Characteristics

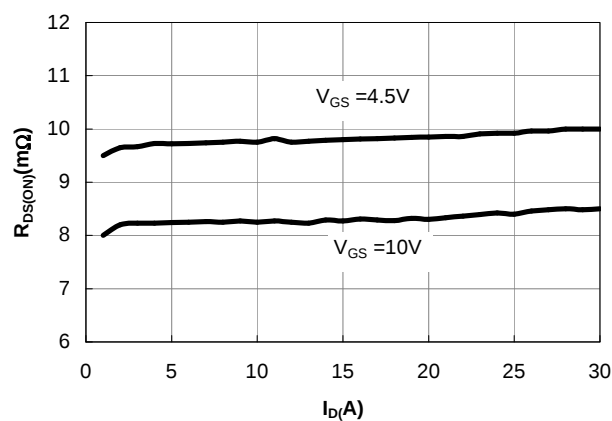


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

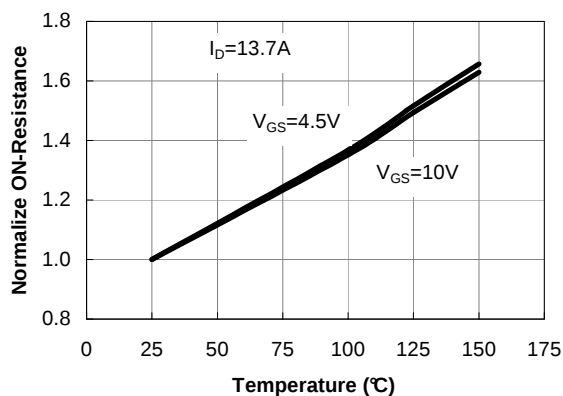


Figure 4: On-Resistance vs. Junction Temperature

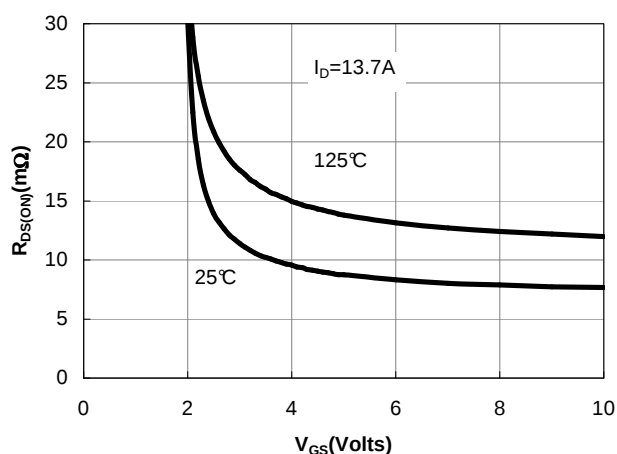


Figure 5: On-Resistance vs. Gate-Source Voltage

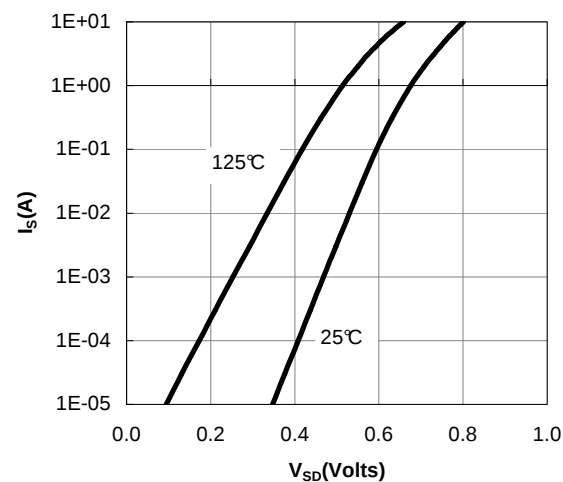


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

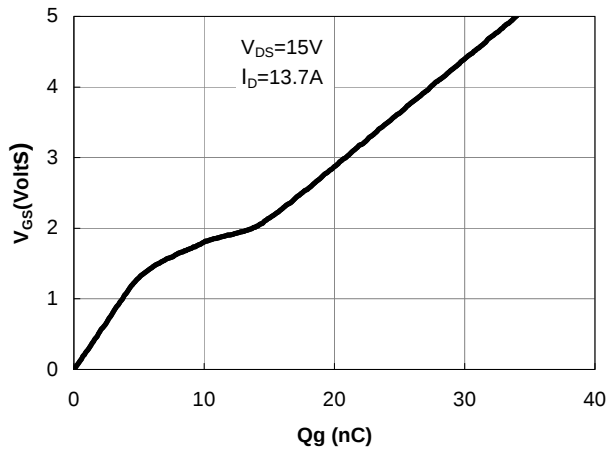


Figure 7: Gate-Charge Characteristics

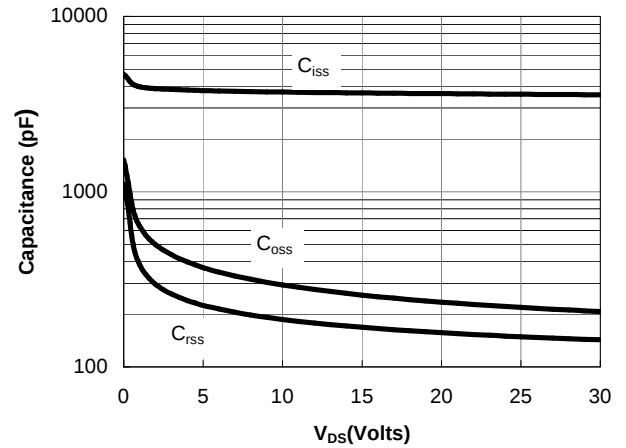


Figure 8: Capacitance Characteristics

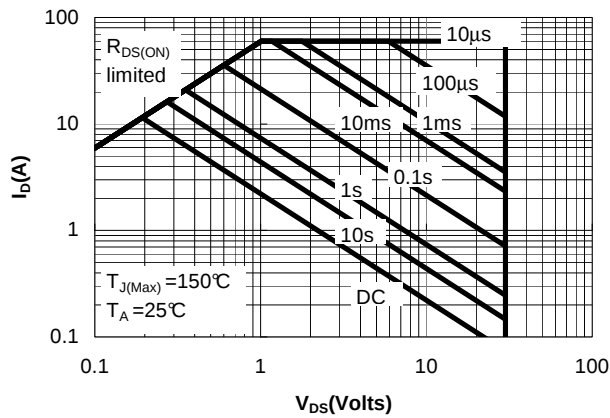


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

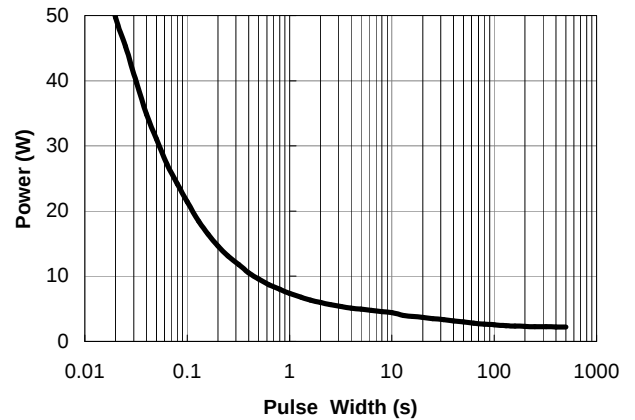


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

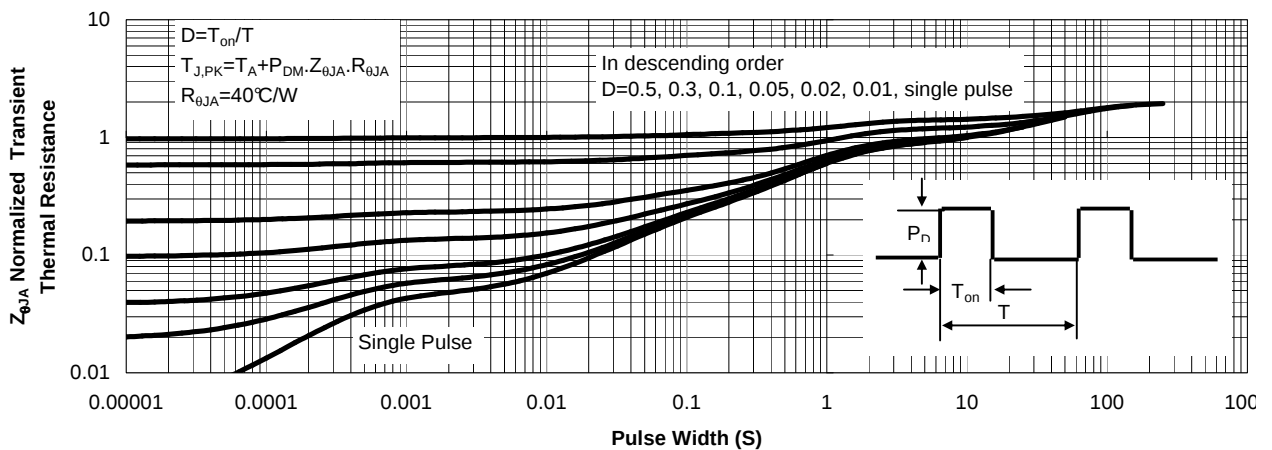


Figure 11: Normalized Maximum Transient Thermal Impedance