

Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

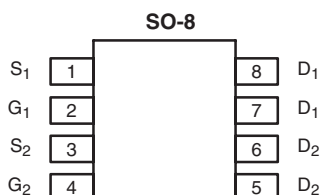
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ.)
30	0.016 at $V_{GS} = 10$ V	8	19
	0.018 at $V_{GS} = 4.5$ V	8	
	0.024 at $V_{GS} = 2.5$ V	8	

FEATURES

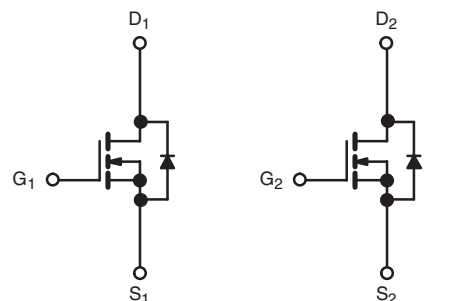
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Top View



N-Channel MOSFET

N-Channel MOSFET

Ordering Information: Si4922BDY-T1-E3 (Lead (Pb)-free)
Si4922BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current (10 μ s Pulse Width)	I_{DM}	35	A
Source-Drain Current Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	
Pulsed Source-Drain Current	I_{SM}	35	
Single Pulse Avalanche Current	I_{AS}	15	mJ
Single-Pulse Avalanche Energy	E_{AS}	11.2	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 50 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit		Unit
		Typical	Maximum	
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	50	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	30	40	

Notes:

- Based on $T_C = 25$ °C.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under Steady State conditions is 110 °C/W.
- Package Limited.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		35		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 4.6		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.8	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		0.0135	0.016	Ω
		V _{GS} = 4.5 V, I _D = 5 A		0.0145	0.018	
		V _{GS} = 2.5 V, I _D = 5 A		0.018	0.024	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 5 A		30		S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		2070		pF
Output Capacitance	C _{oss}			255		
Reverse Transfer Capacitance	C _{rss}			135		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 5 A		41	62	nC
Gate-Source Charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 5 A		19	29	
Gate-Drain Charge	Q _{gd}			3.5		
Gate Resistance	R _g			3.7		
Turn-On Delay Time	t _{d(on)}	f = 1 MHz		1.8	3	Ω
Rise Time	t _r	V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω		7	14	ns
Turn-Off Delay Time	t _{d(off)}			27	41	
Fall Time	t _f			31	47	
Turn-On Delay Time	t _{d(on)}			8	15	
Rise Time	t _r	V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω		13	25	
Turn-Off Delay Time	t _{d(off)}			53	80	
Fall Time	t _f			68	102	
				54	81	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			2.5	A
Pulse Diode Forward Current ^a	I _{SM}				35	
Body Diode Voltage	V _{SD}	I _S = 1.7 A		0.77	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1.7 A, dI/dt = 100 A/μs, T _J = 25 °C		32	48	ns
Body Diode Reverse Recovery Charge	Q _{rr}			21	32	nC
Reverse Recovery Fall Time	t _a			13		ns
Reverse Recovery Rise Time	t _b			19		

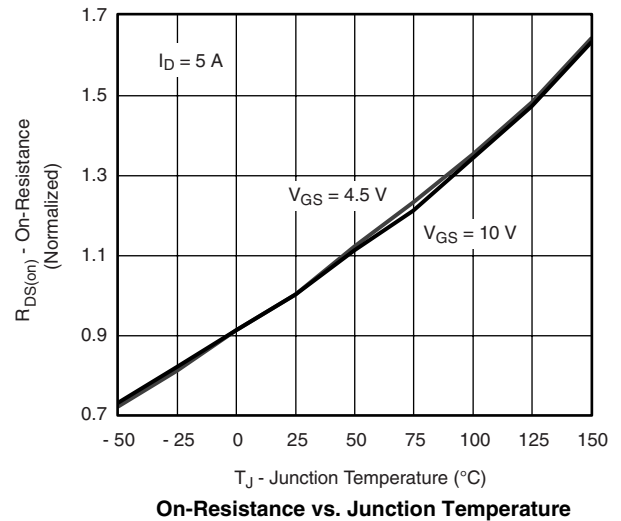
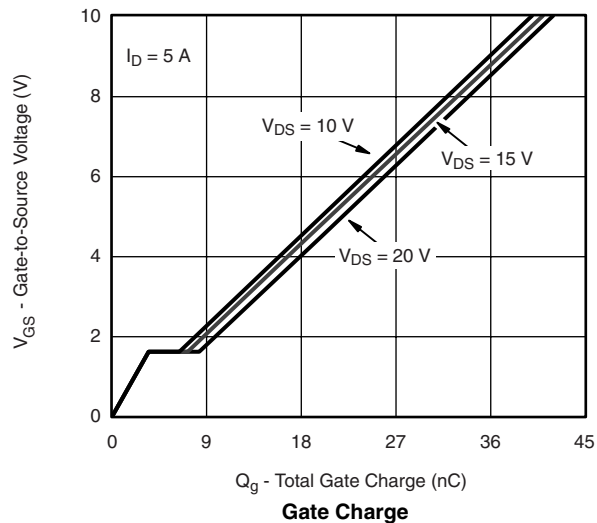
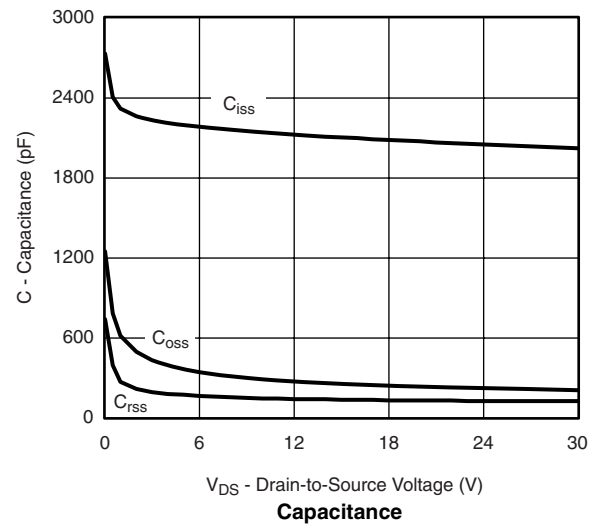
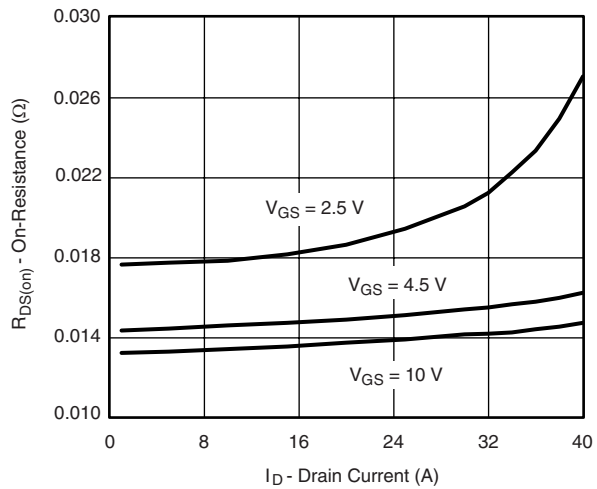
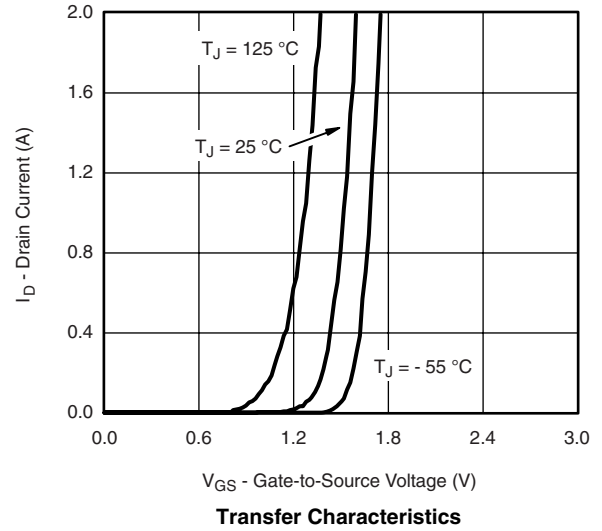
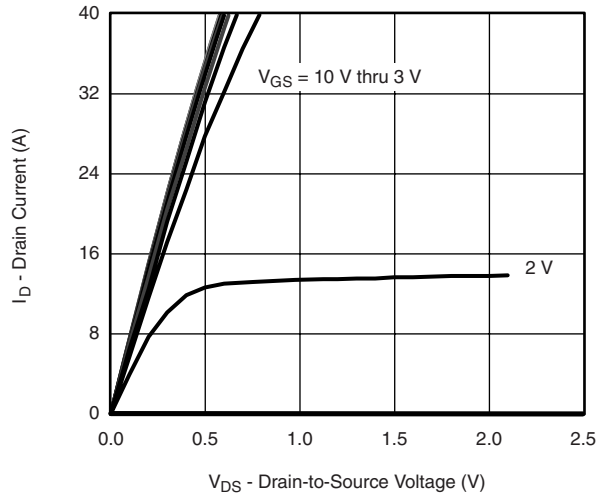
Notes:

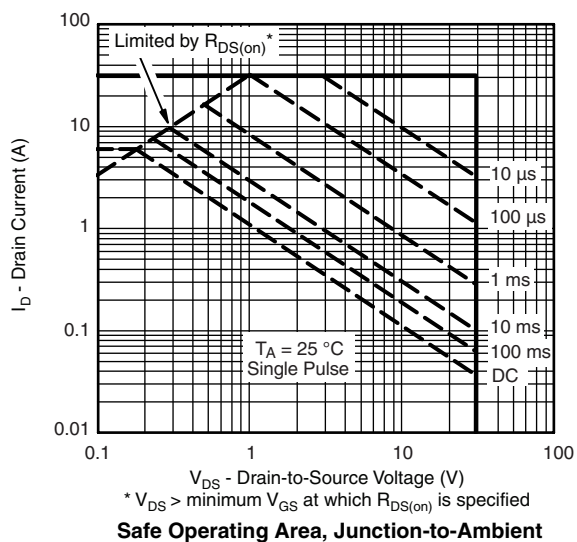
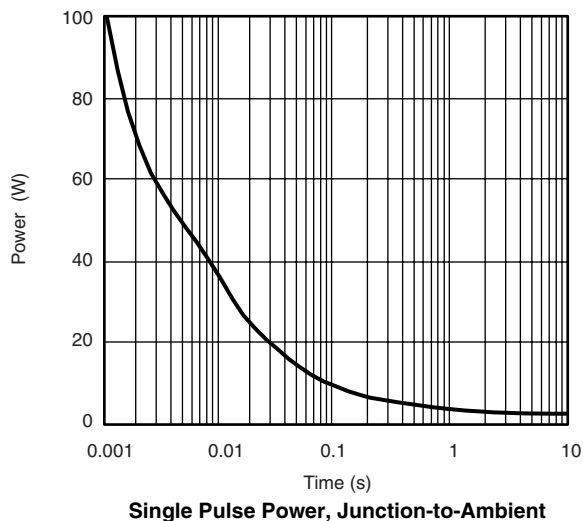
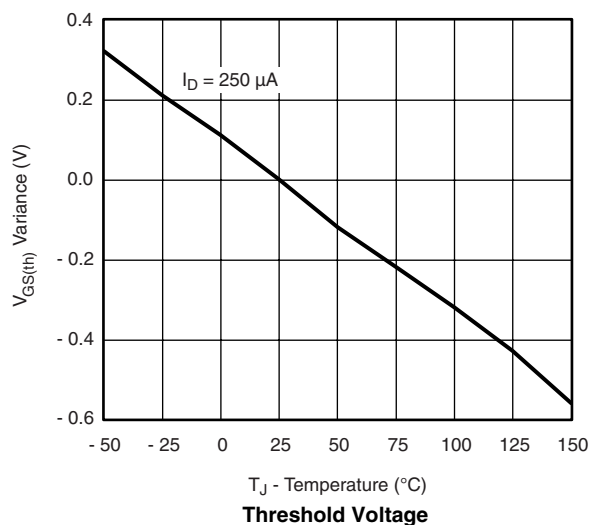
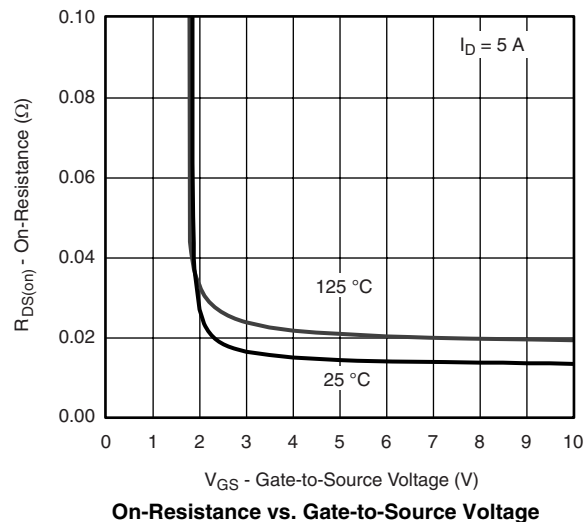
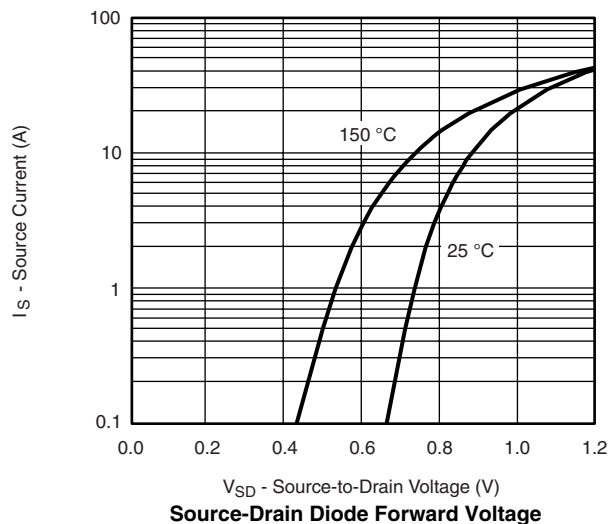
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

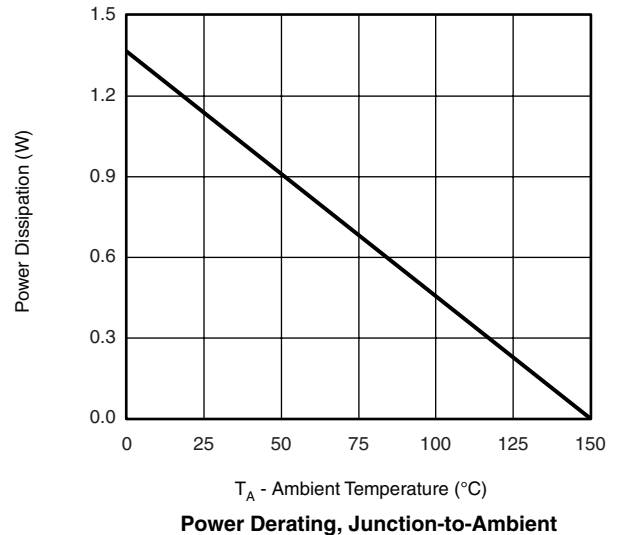
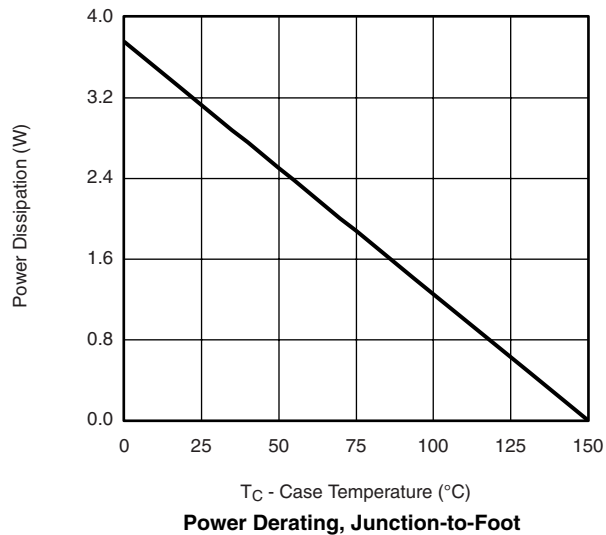
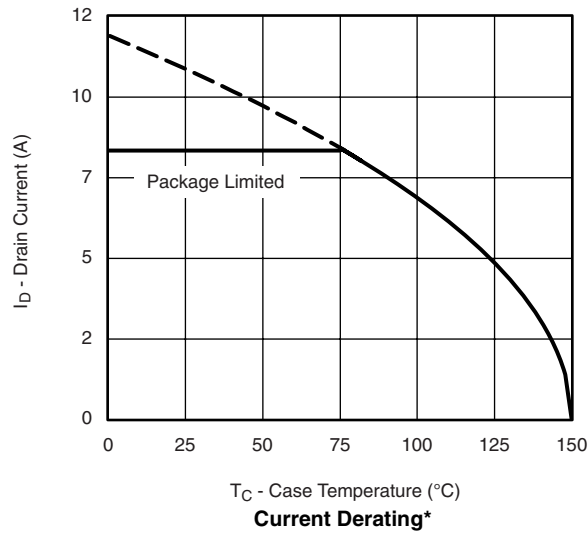
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

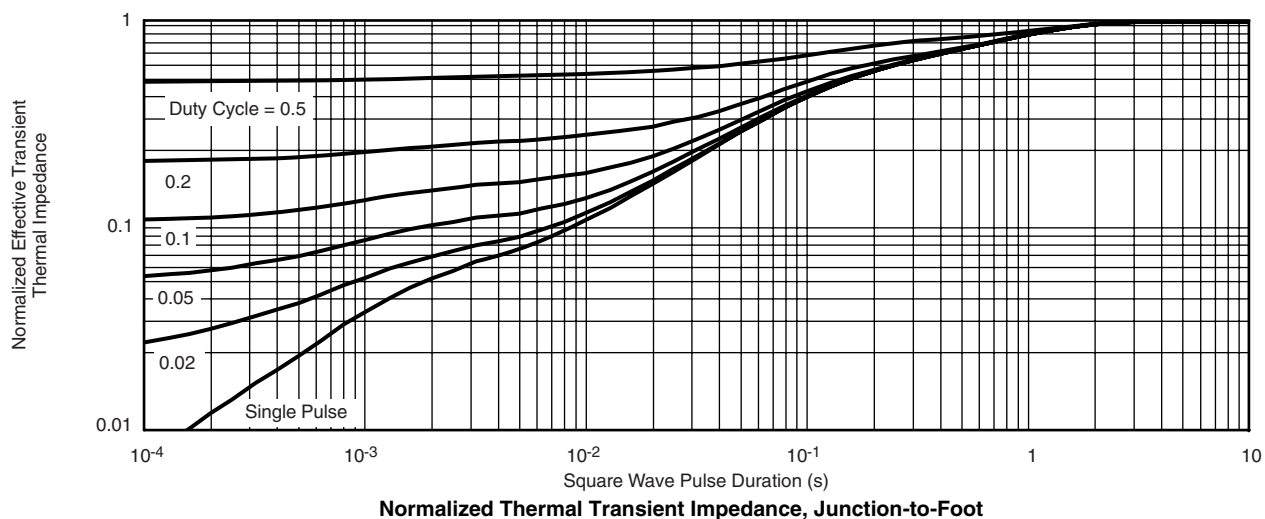
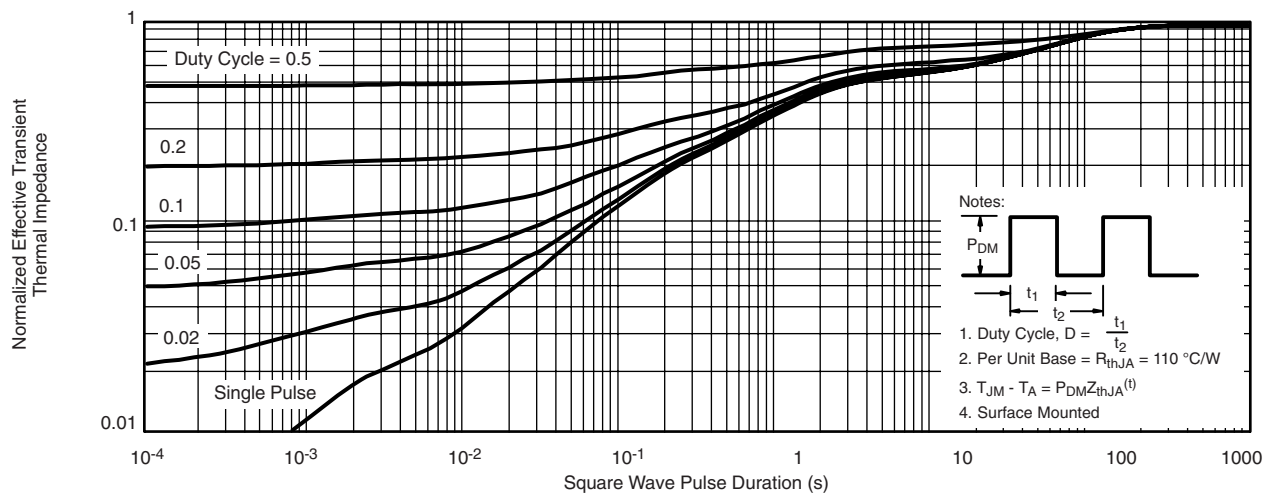


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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