PMIC for LCD TV / Monitor

General Description

The RT9955 generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and monitors. It includes boost and buck regulators, VGH and VGL charge pump regulators, gate pulse modulator (GPM) , HV LDO, voltage detector (XAO) and VCOM OP. The RT9955 supports input voltage from 8V to 14V and is optimized for LCD TV panel and LCD monitor applications running directly from 12V supply.

The boost and buck regulators feature internal power MOSFETs and high frequency operation, allowing the use of small inductors and capacitors, for in a compact solution. Both switching regulators use fixed frequency, current mode control architectures, providing fast load-transient response and easy compensation.

The VGH and VGL charge pump regulators provide supply voltages for the TFT gate driver. Both output voltages can be adjusted with external resistive voltage dividers.

The GPM is controlled by frame signals from the timing controller to modulate the Gate-On voltage (VGHM), which acts as a flicker compensation to reduce the coupling effect between gate lines and pixels. It can also delay VGHM while power on to achieve a correct power on sequence for gate driver ICs. The VGHM power on delay time, the falling time and falling stop voltage can all be programmed by an external capacitor, an external resistor and an resistive voltage divider.

The voltage detector (XAO) monitors VIN voltage to issue a reset signal when the VIN voltage is too low. The detecting level is determined by an external resistive voltage divider.

The HV LDO can provide a highly accurate voltage (0.5%) for gamma reference voltage. It has fast transient response and also a wide operation input range.

The VCOM OP can drive the LCD VCOM voltage that features high short circuit current (300mA), fast slew rate (45V/μs), wide bandwidth (20MHz) and rail-to-rail inputs and outputs.

The RT9955 is available in a small WQFN-48L 7x7 package.

Features

- **8V to 14V Supply Input Voltage Range**
- **Current Mode Boost Regulator**
  - **20V 3A 0.1Ω Internal N-MOSFET**
  - **Programmable Over Current Protection**
  - **Programmable Soft-Start**
- **Current Mode Buck Regulator**
  - **16.5V 3.2A 0.15Ω Internal N-MOSFET**
  - **Over Current Protection**
  - **Adjustable Output Voltage from 1.8V to 3.3V**
- **Adjustable VGH Charge Pump**
  - **Continuous Output Current 50mA**
- **Adjustable VGL Charge Pump**
  - **Continuous Output Current 50mA**
- **Gate Pulse Modulator**
  - **18V to 35V Positive Supply Input**
  - **Power On/Off Sequence Control**
  - **On-Chip GPM Controller with Adjustable Falling Time and Falling Stop Voltage**
- **Voltage Detector (XAO)**
  - **Adjustable Detecting Voltage (±1%)**
  - **N-CH Open-Drain Output**
- **VCOM OP**
  - **5V to 20V Input Supply Voltage**
  - **±300mA Output Short-Circuit Current for 1ms**
  - **45V/μs Slew Rate**
  - **20MHz, –3dB Bandwidth**
- **HV LDO**
  - **5V to 20V Input Supply Voltage**
  - **Adjustable Output Voltage (±0.5%)**
  - **Over Current Protection (60mA)**
  - **Low Dropout Voltage 0.5V (60mA)**
- **Selectable Frequency (500kHz/750KHz)**
- **External PMOS Isolation Switch Controlled by Gate Drive Signal**
- **Under Voltage Protection**
- **Short Circuit Protection**
- **Over Temperature Protection**
- **Power On Sequence Control**
- **Thin 48-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- LCD TV / Monitor

Ordering Information

RT9955 □□

Package Type
QW : WQFN-48L 7x7 (W-Type)
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

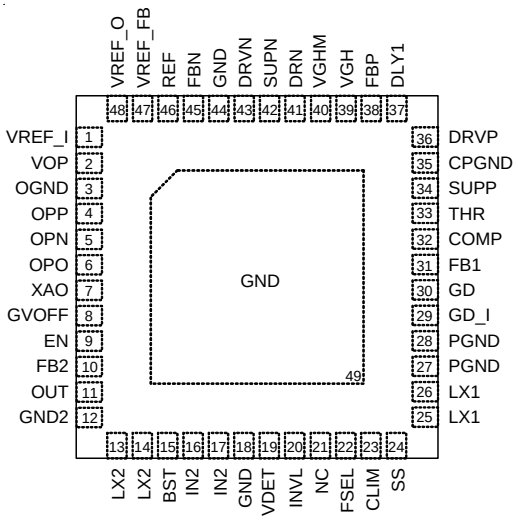
Marking Information

RT9955GQW : Product Number

YMDNN : Date Code

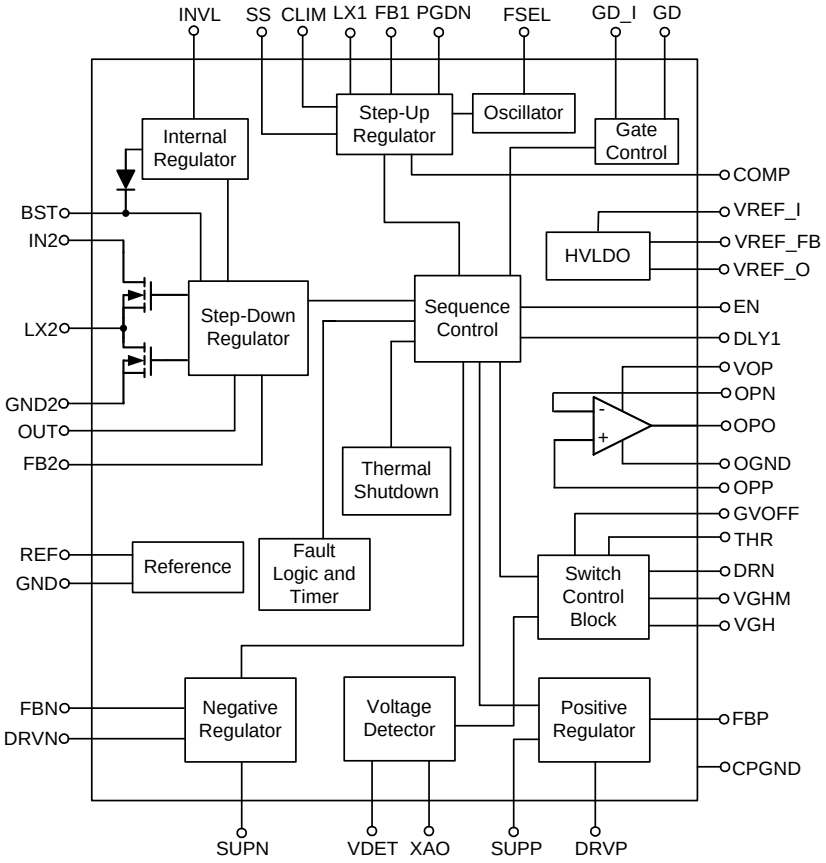
Pin Configuration

(TOP VIEW)

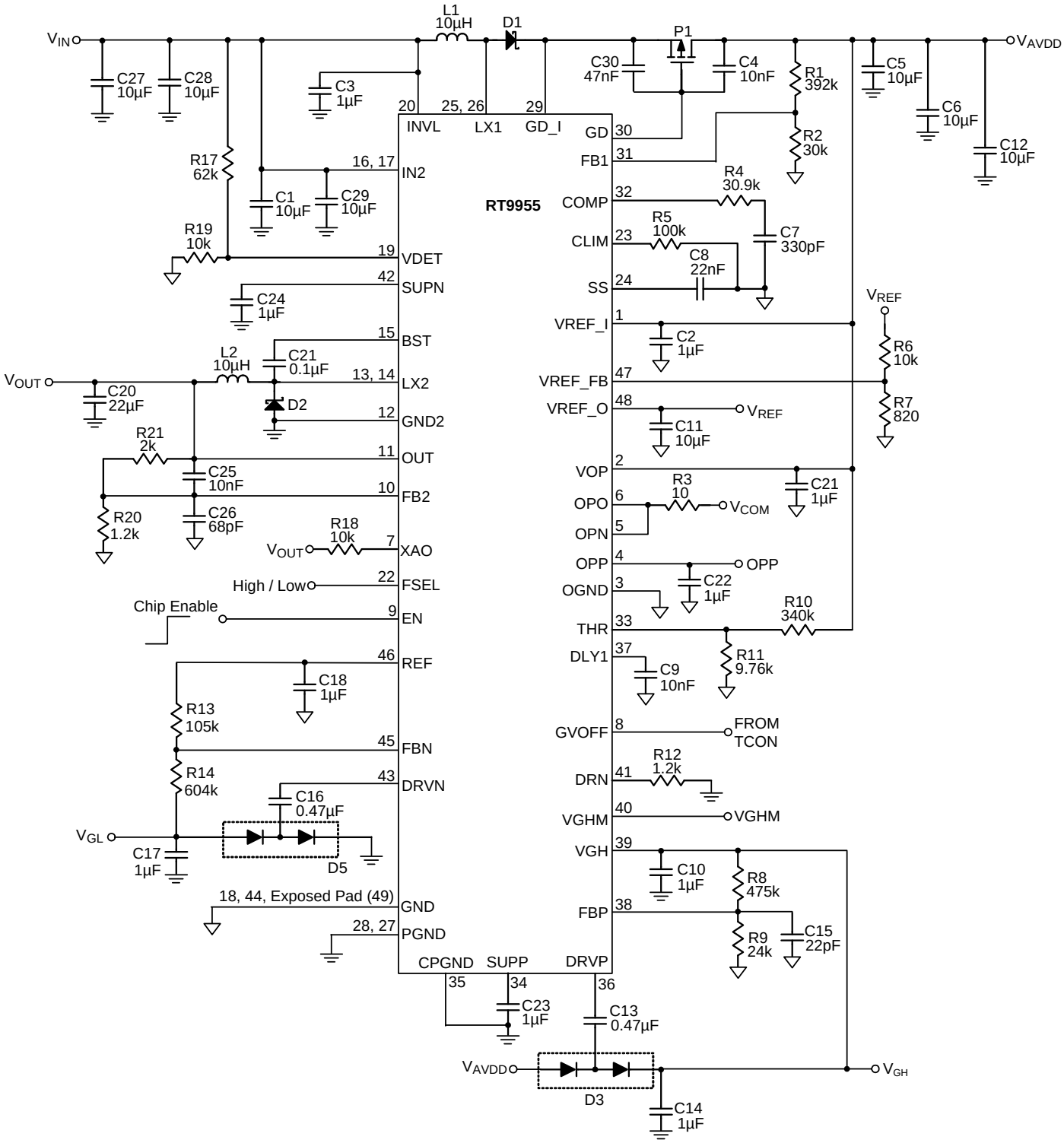


WQFN-48L 7x7

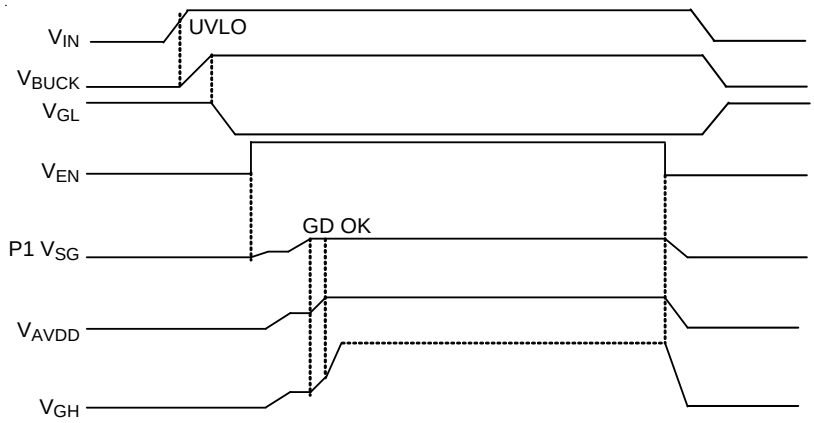
Functional Block Diagram



Typical Application Circuit



Timing Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VREF_I	Linear regulator input. Bypass VREF_I to GND with a 1μF capacitor close to the pin.
2	VOP	Operational amplifier supply input. Connect this pin to the output of boost regulator and bypass to OGND with a 1μF capacitor.
3	OGND	Ground for operational amplifiers. Connect this pin to power ground underneath the IC.
4	OPP	Operational amplifier non-inverting input.
5	OPN	Operational amplifier inverting input.
6	OPO	Operational amplifier output.
7	XAO	Reset function output.
8	GVOFF	High voltage switch control input. When GVOFF is high, the high voltage switch between VGH and VGHM is on and the high voltage switch between VGHM and DRN is off. When GVOFF is low, the switch between VGH and VGHM is off and the switch between VGHM and DRN is on. GVOFF is inhibited by the VIN under voltage lock out when the voltage on DLY1 is less than 1.25V.
9	EN	Enable input. Pulling EN high enables boost regulator and VGH charge pump.
10	FB2	Buck regulator feedback input. Connect FB2 to the center of a resistive voltage divider between buck regulator output and GND to set buck regulator output voltage.
11	OUT	Buck regulator output sense input. OUT is the inverting input to the internal current sense amplifier. Connect OUT directly to the step-down regulator output.
12	GND2	Buck regulator power ground.
13, 14	LX2	Buck regulator switching node. LX2 is the source of the internal high side MOSFET. Connect the inductor and Schottky diode to LX2 and minimum the trace area for low EMI performance.
15	BST	Buck regulator bootstrap pin. BST is the supply for the high side MOSFET gate driver. Connect a 0.1μF ceramic capacitor from BST to LX2.
16, 17	IN2	Buck regulator supply input.
19	VDET	Voltage detection input. Connect VDET to the center of a resistive voltage divider between VIN and AGND.
20	INVL	4V internal linear regulator and startup circuitry supply input. The input voltage range of INVL is between 8V and 14V. Connect a 1μF ceramic capacitor between INVL and GND. Place the capacitor close to the IC.
21	NC	No internal connection.
22	FSEL	Frequency select pin. Connect FSEL to VIN or leaving FSEL unconnected for 750kHz operation. Connect this pin to GND for 500kHz operation.
23	CLIM	Boost regulator OCP level setting by an external resistor to GND.
24	SS	Soft-start control pin. Connect a soft-start capacitor (C8) to this pin. Soft-start capacitor is charged with 5μA. The soft start capacitor is discharged to ground when EN is low. If C8 is less than 220pF, soft-start is controlled internally and soft-start time is 10ms. Otherwise, the soft-start time is controlled by C8 and 5μA charging current.
25, 26	LX1	Boost regulator switching node. Connect the inductor and the Schottky diode to LX1 and minimum the trace area for low EMI.
27, 28	PGND	Boost regulator power ground.

Pin No.	Pin Name	Pin Function
29	GD_I	Output sense pin. The GD_I pin is connected to the internal tracking circuit and over voltage protection comparator. This pin needs to be connected to the output of the boost converter.
30	GD	Gate drive pin. Used to control an external PMOSFET switch to provide input to output isolation of AVDD. GD pin will be pulled low when EN pulls high. The GD pin pulls high when UVP/SCP occurs.
31	FB1	Boost regulator feedback input. Connect FB1 to the center of a resistive voltage divider between boost regulator output and GND to set boost regulator output voltage. Place the resistive voltage divider close to FB1.
32	COMP	Boost regulator error amplifier compensation pin.
33	THR	VGHM falling regulation adjustment input. Connect THR to the center of a resistive voltage divider between a reference supply and GND to adjust the VGHM falling regulation set point. GVOFF low allow VGHM to disconnect from VGH and be discharged through RE; discharge stops when VGHM reaches 10 x VTHR.
34	SUPP	VGH charge-pump regulator supply input. Bypass SUPP to CPGND with a minimum 1μF ceramic capacitor.
35	CPGND	Power ground for charge pump.
36	DRVP	VGH charge pump regulator driver output.
37	DLY1	VGH charge pump regulator and GPM delay input. Connect a capacitor, C9, between DLY1 and GND to set the delay time. A 5μA current source charges C9.
38	FBP	VGH charge pump regulator feedback input. Connect FBP to the center of a resistive voltage divider between the positive output and GND to set the positive charge pump regulator output voltage. Place the resistive voltage divider close to FBP.
39	VGH	GPM input.
40	VGHM	GPM output.
41	DRN	GPM discharge pin.
42	SUPN	VGL charge pump regulator supply input. Bypass SUPN to GND with a minimum 1μF ceramic capacitor.
43	DRVN	VGL charge pump regulator driver output.
18, 44	GND	VGL charge pump power ground and analog ground.
45	FBN	VGL charge pump regulator feedback input. Connect FBN to the center of a resistive voltage divider between the negative output and REF to set the negative charge pump regulator output voltage. Place the resistive voltage divider close to FBN.
46	REF	Reference output. Connect a 1μF ceramic capacitor between REF and GND.
47	VREF_FB	Linear regulator feedback input. Connect VREF_FB to the center of a resistive voltage divider between to VREF_O and GND to set the needed regulator output voltage.
48	VREF_O	Linear regulator output. Bypass VREF_O to GND with a minimum 1μF capacitor close to the pin.
49 (Exposed Pad)	GND	Ground pin. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Absolute Maximum Ratings (Note 1)

- IN2, INVL, SUPN, FSEL to GND ---------- –0.3V to 16.5V
- SUPP, GD_I, VOP, VREF_I to GND ---------- –0.3V to 20V
- DRVP to CPGND ---------- –0.3V to (V_{SUPP} + 0.3V)
- DRVN to GND ---------- –0.3V to (V_{SUPN} + 0.3V)
- OPO, OPP, OPN to OGND ---------- –0.3V to (V_{VOP} + 0.3V)
- VREF_O to GND ---------- –0.3V to (V_{VREF_I} + 0.3V)
- FB1, FB2, FBP, FBN, GVOFF, DLY1, VREF_FB, THR, EN to GND ---------- –0.3V to 6.5V
- OUT, REF, COMP, SS, XAO, VDET, CLIM to GND ---------- –0.3V to 6.5V
- GND2, OGND, CPGND to GND ---------- ±0.3V
- BST to GND2 ---------- –0.3V to 20V
- LX1 to PGND ---------- –0.3V to 20V
- LX2 to GND2 ---------- –0.3V to (IN2+0.3V)
- VGHM, VGH, DRN to GND ---------- –0.3V to 40V
- VGH to VGHM ---------- –0.3V to 40V
- VGH, VGHM to DRN ---------- –0.3V to 40V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-48L 7x7 ---------- 3.226W
- Package Thermal Resistance (Note 2)
  WQFN-48L 7x7, θ_{JA} ---------- 31°C/W
  WQFN-48L 7x7, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

Recommended Operating Conditions (Note 3)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
IN2, INVL Input Voltage Range			8	12	14	V
Quiescent Current into INVL	I_{QIN}	LX not switching	--	0.02	2	mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	5.4	6	6.6	V
		Rising hystersis	0.1	--	0.5	
Switching Frequency		FSEL = GND	--	500	--	kHz
		FSEL = VIN	--	750	--	
Maximum Duty-Cycle			--	80	--	%
Boost Regulator						
Output Voltage Range	V_{AVDD}		VIN	--	18	V
FB1 Reference Voltage	V_{FB1}		1.2375	1.25	1.2625	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB Line Regulation		V_{IN} = 10.8V to 13.2V	--	0.15	0.2	%/V
Transconductance	G_m	ΔI = ±2.5μA at COMP = 1V	--	100	--	μA/V
Voltage Gain	A_V	FB to COMP	--	700	--	V/V
Current Limit	I_{LIM1}		3	4	--	A
On-Resistance	$R_{DS(ON)}$		--	100	250	mΩ
Current-Sense Transresistance	R_{CS}		--	0.25	--	V/A
Soft-start Charge Current	I_{SS}		--	5	--	μA
Internal Soft-Start		C8 < 220pF	--	10	--	ms
Reference						
REF Output Voltage		No external load,	--	1.25	--	V
REF Load Regulation		0 < I_{REF} < 50μA	--	10	--	mV
REF Sink Current		REF in regulation	--	10	--	μA
Buck Regulator						
FB2 Reference Voltage	V_{FB2}		1.2375	1.25	1.2625	V
DC Line Regulation		10.8V < V_{IN} < 13.2V	--	0.1	--	%/V
LX2-to-IN2 Switch On-Resistance			--	150	300	mΩ
LX2-to-GND2 Switch On-Resistance			--	20	--	Ω
Current Limit			2.5	3.2	--	A
Error Amplifier Transconductance	G_{m2}		--	100	--	μA/V
Error Amplifier Voltage Gain	A_V		--	700	--	V/V
Current-Sense Transresistance	R_{CS}		--	0.3	--	V/A
Soft-Start Ramp Time			--	3	--	ms
FB2 UVP Trip Level		Falling edge	--	1	--	V
Duration to Trigger UVP Condition			--	50	--	ms
FB2 SCP Trip Level		Falling edge	--	0.5	--	V
Positive Charge-Pump Regulator						
FBP Reference Voltage	V_{FBP}		1.225	1.25	1.275	V
FBP Line Regulation Error		V_{IN} = 10.8V to 13.2V	--	--	6	mV/V
DRVP P-MOSFET On-Resistance			--	2	--	Ω
DRVP N-MOSFET On-Resistance			--	1	--	Ω
Soft-Start Ramp Time			--	3	--	ms
FBP UVP Trip Level		Falling edge	--	1	--	V
Duration to Trigger Fault Condition			--	50	--	ms
FBP Short Circuit Level		Falling edge	--	0.5	--	V
Negative Charge-Pump Regulator						
FBN Regulation Voltage			0.21	0.25	0.29	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Final FBN Regulation Voltage		$V_{REF} - V_{FBN}$	0.98	1	1.02	V
FBN Line Regulation Error		V_{IN} = 10.8V to 13.2V	--	--	6	mV/V
DRVN P-MOSFET On-Resistance			--	6	--	Ω
DRVN N-MOSFET On-Resistance			--	2	--	Ω
Soft-Start Ramp Time			--	3	--	ms
FBN UVP Trip Level		$V_{REF} - V_{FBN}$	--	0.8	--	V
Duration to Trigger Fault Condition			--	50	--	ms
FBN Short Circuit Protection Level		$V_{REF} - V_{FBN}$	--	0.4	--	V
Sequence Control						
EN Input Low Voltage			--	--	0.6	V
EN Input High Voltage			1.5	--	5.5	V
DLY1 Capacitor Charge Current			--	5	--	μA
VDLY1 Turn-On Threshold			--	1.25	--	V
GD Output Sink Current		EN = high, $V_{GD\_I} = V_{IN}$	--	10	--	μA
GD On-Voltage		EN = high, $V_{GD\_I} = V_{IN}$	--	$V_{IN} - 5$	--	V
Gate Pulse Modulator (GPM)						
GVOFF Input Low Voltage			--	--	0.6	V
GVOFF Input High Voltage			1.5	--	5.5	V
GVOFF Input Leakage Current			–1	--	1	μA
GVOFF-to-VGHM Rising Propagation Delay		1kΩ from DRN to GND, 1.5nF from VGHM to GND	--	100	--	ns
GVOFF-to-VGHM Falling Propagation Delay		1kΩ from DRN to GND, 1.5nF from VGHM to GND	--	250	--	ns
VGH Input Current		V_{DLY1} = GVOFF = 3V	--	1.5	2	mA
		V_{DLY1} = 3V, GVOFF = 0	--	0.14	0.2	
DRN Input Current		DRN = 8V, V_{DLY1} = 3V, VGHM > DRN, GVOFF = 0	--	0	1	μA
VGH Switch On-Resistance		V_{DLY1} = GVOFF = 3V	--	5	10	Ω
DRN Switch On-Resistance		V_{DLY1} = 3V, GVOFF = 0, VGHM= 28V, THR = 1.4V	--	20	50	Ω
VGHM Stop Level		V_{THR} < 1.5V	--	10 x V_{THR}	--	V
Voltage Detector (XAO)						
Detecting Voltage Adjustment	V_{DET}	Falling edge	--	1.25	--	V
Detecting Voltage Accuracy			–1	--	1	%
VCOMP OP						
Supply Voltage Range	V_{OP}		4.5	--	18	V
Supply Current	I_{OP}		--	3	--	mA
Input Offset Voltage	V_{OS}	V_{COM} = AVDD/2	--	--	20	mV
Input Bias Current	I_{BIAS}		--	1	100	nA

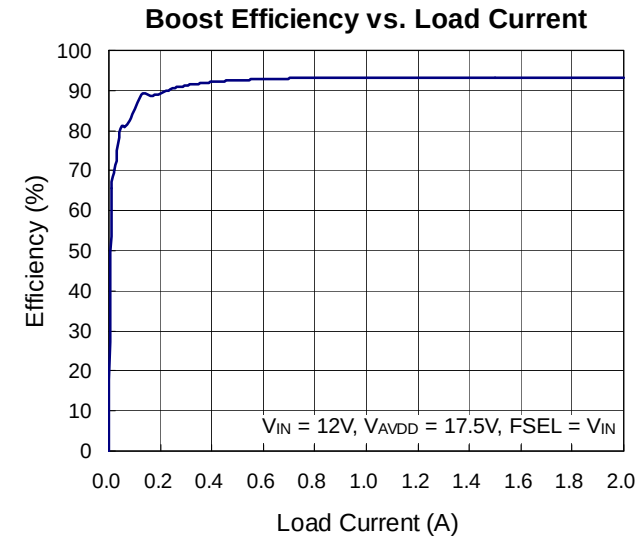
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Swing High	V_{OH}	I_{LOAD} = 10mA	--	V_{SUP} –100	--	mV
Output Voltage Swing Low	V_{OL}	I_{LOAD} = –10mA	--	100	--	mV
Short Circuit Current		To AVDD/2 source or sink for 1ms	--	300	--	mA
-3dB Bandwidth	F_{3dB}	R_L = 10kΩ, C_L = 10pF	--	20	--	MHz
Gain Bandwidth Product	G_{BW}	R_L = 10kΩ, C_L = 10pF	--	8	--	MHz
Slew Rate			--	45	--	V/μs
HVLDO						
Quiescent Current	I_Q		--	40	--	μA
LDO Feedback Reference Voltage	V_{REF_FB}		--	1.25	--	V
Feedback Voltage Tolerance			–0.5	--	0.5	%
Output Current Limit		V_{REF_I} = 15V, V_{REF_O} = 14V, R_{OUT} = 50Ω	60	--	--	mA
Dropout Voltage		I_{LOAD} = 60mA	--	0.5	--	V
Power Supply Rejection Rate		V_{REF_I} = V_{REF_O} + 1V, I_{OUT} = 10mA	--	60	--	dB
Protection						
Thermal Shutdown Threshold	T_{SD}		--	160	--	°C
Switching Frequency Selection						
FSEL Input Levels		FSEL = high	1.5	--	--	V
		FSEL = low	--	--	0.6	
FSEL Pull High Current			--	5	--	μA

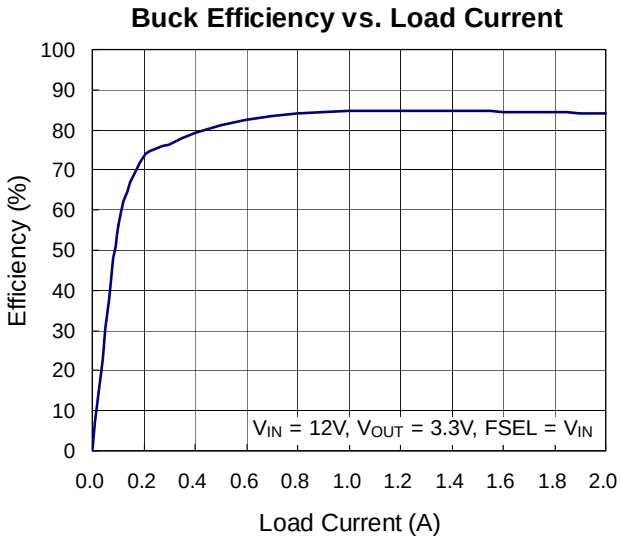
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

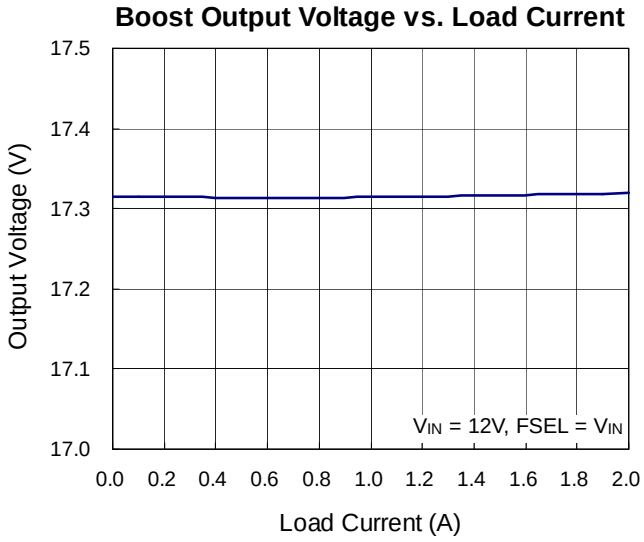
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

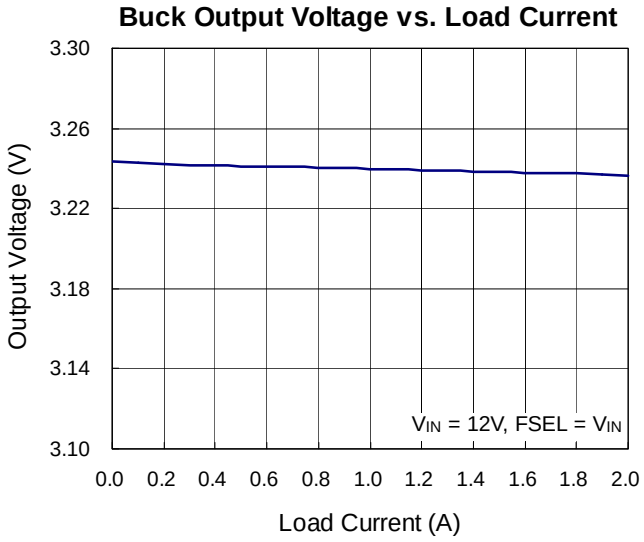
Note 3. The device is not guaranteed to function outside its operating conditions.

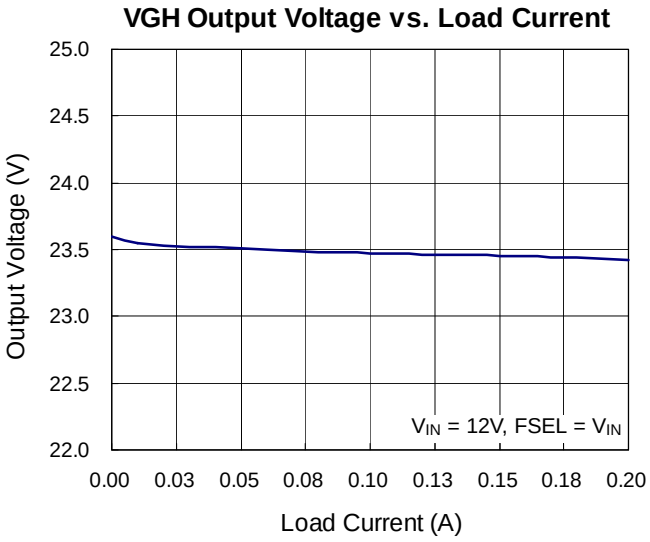
Typical Operating Characteristics

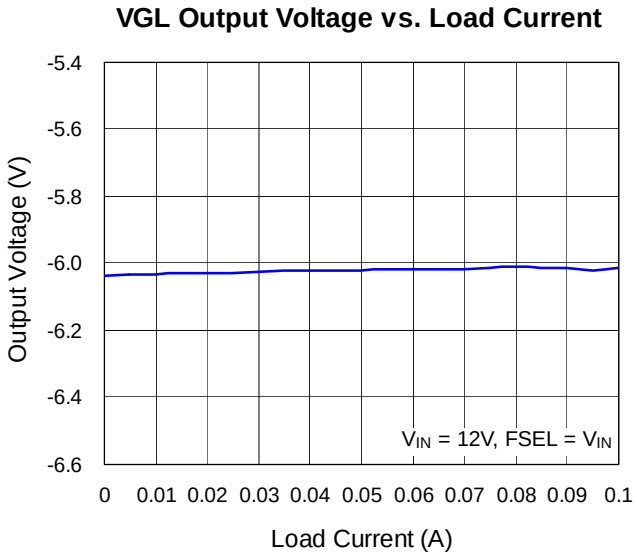




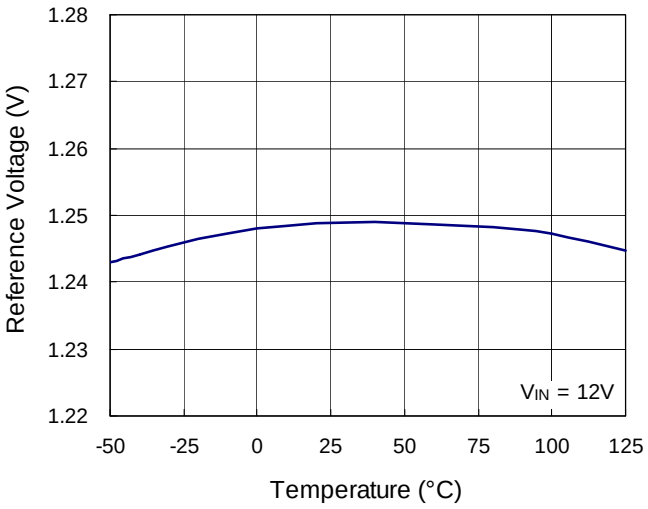




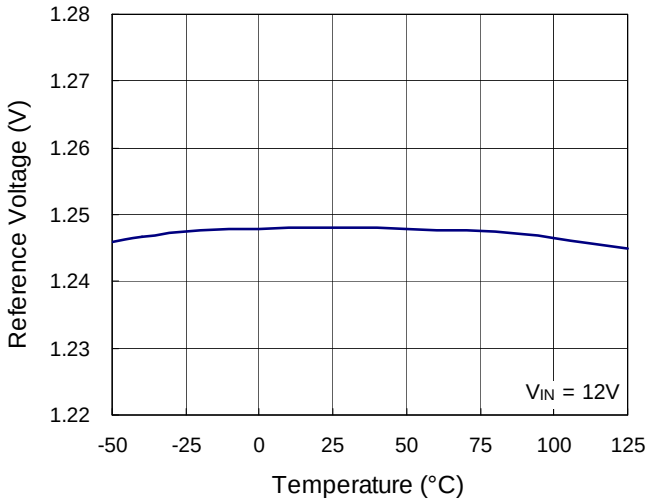




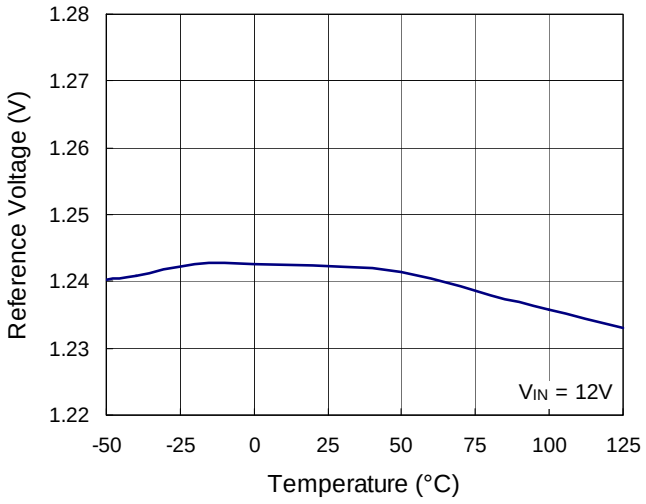
Boost Reference Voltage vs. Temperature



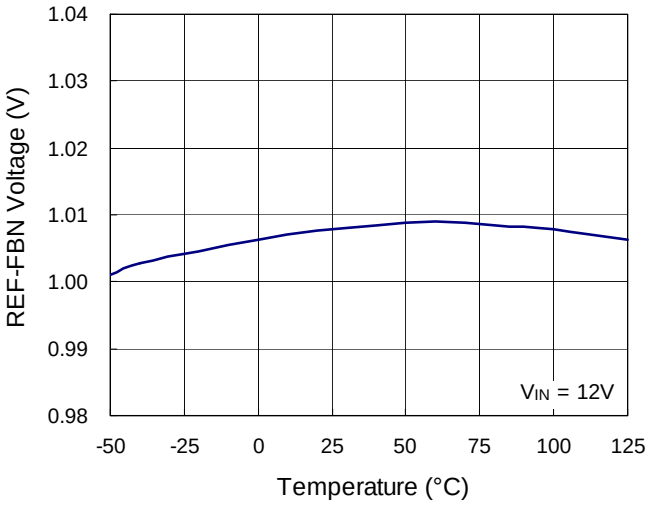
Buck Reference Voltage vs. Temperature



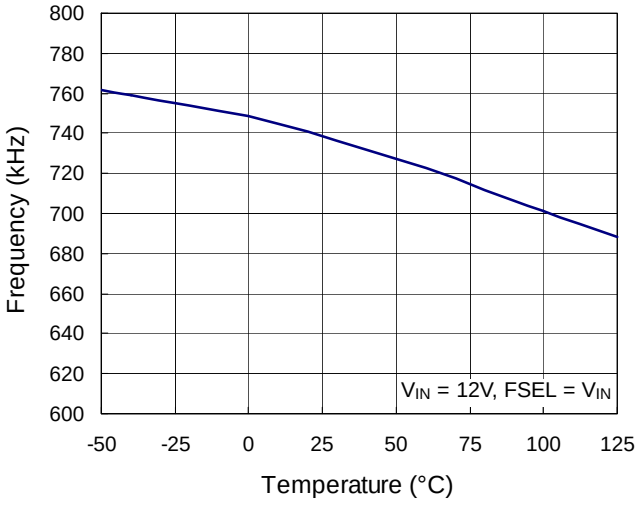
VGH Reference Voltage vs. Temperature



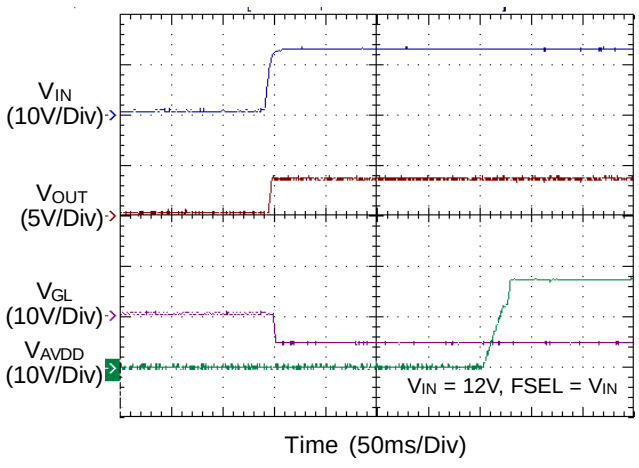
REF-FBN Voltage vs. Temperature



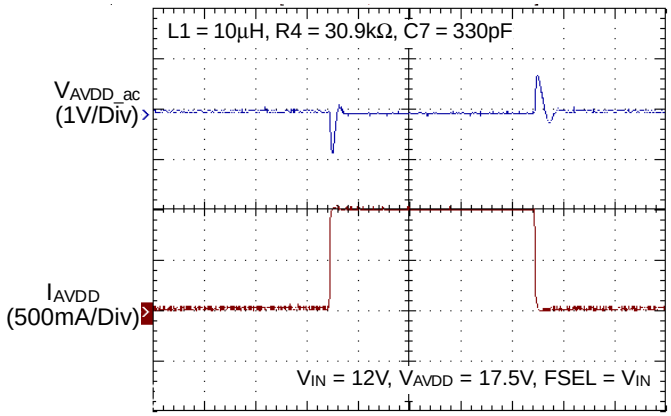
Frequency vs. Temperature



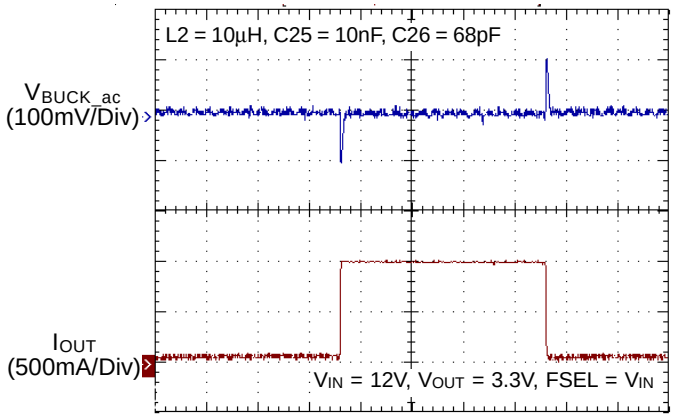
Power On



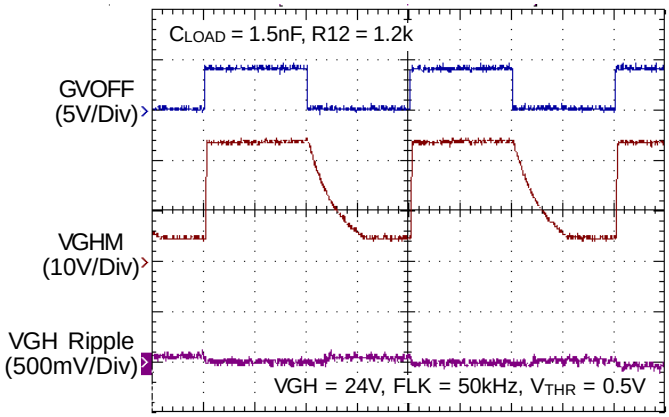
Boost Load Transient Response



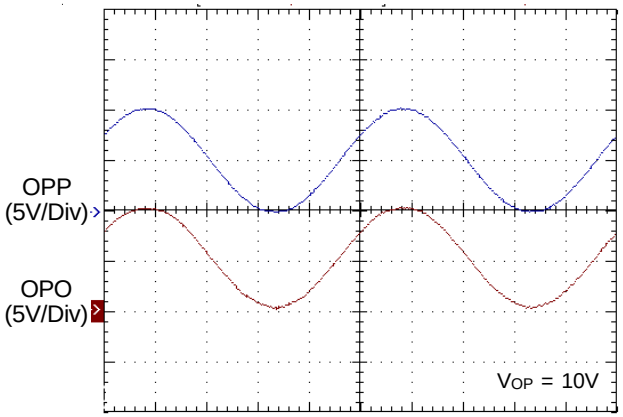
Buck Load Transient Response



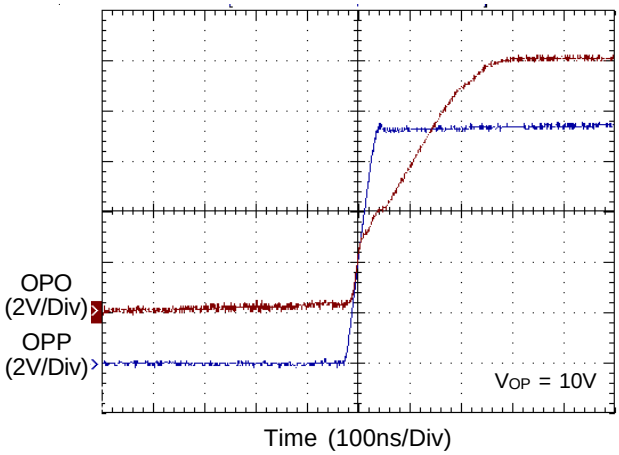
GPM with GVOFF



OPA Rail-to-Rail Input vs. Output



OPA Slew Rate



Application Information

The RT9955 contains a high performance boost regulator to generate voltage for the panel source driver ICs and a buck converter to provide the logic voltage for the timing controller. It also includes a voltage detector, a high voltage LDO regulator, and a fast response operational amplifier for common voltage. Moreover, a positive and a negative charge pump regulator are included to generate gate high and gate low voltages respectively. The following content contains detailed description of the part, as well as information for component selection.

Boost Regulator

The boost regulator is a high efficiency current-mode PWM architecture with 500kHz / 750kHz operation frequency. It provides the regulated supply voltage for the panel source driver ICs. The converter is a high switching frequency current-mode regulator with an integrated 20V N-Channel 0.1Ω MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to generate source driver supplies for TFT LCD display.

Gate Function

The gate function is used to control an external P-MOSFET to provide input to output isolation of AVDD. The GD pin is pulled low when EN pulls high. The GD pin pulls high when UVP or SCP occurs.

Boost Soft-Start

The RT9955 boost converter provides a soft-start function to minimize the inrush current. If the capacitor,C8, is less than 220pF, soft-start will be controlled internally with a default soft-start time of 10ms. Otherwise, the soft-start time is controlled by C8 with a 5μA charging current. A typical value for the soft-start capacitor is 22nF.

Boost Output Voltage Setting

The regulated output voltage is shown in the following equation :

$$AVDD = V_{FB1} \times \left(1 + \frac{R1}{R2}\right), \text{ where } V_{FB1} = 1.25V \text{ (typ.)}$$

The recommended value for R2 is up to 10kΩ without any side-effects. Moreover, place the resistor divider as close as possible to the chip to reduce noise sensitivity.

Boost Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisting of R4 and C7 . Choose R4 to set high frequency integrator gain for fast transient response and C7 to set the integrator zero to maintain loop stability.

Boost Over Current Protection

The RT9955 boost converter has over-current protection to limit the peak inductor current. It prevents large current from damaging the inductor and diode. If the inductor current exceeds the current limit, while the switch is ON the internal LX switch will turn off immediately to shorten the duty cycle. Therefore, the output voltage drops whenever the over current condition occurs. The peak inductor current is also affected by the input voltage, duty cycle, and inductor value. Therefore, the boost OCP level is setting by an external resistor to GND. The regulated OCP level is shown as following equation :

$$\text{Boost Current Limit Setting Level} = I_{LIM1} - \frac{60.5k}{R5}$$

where I_{LIM1} is the current-limit level and typical value is 4A

Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor current ripple is 20% to 40% of the maximum input current. Assuming 40% as the criterion, then

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency, $I_{IN(MAX)}$ is the maximum input current and I_{RIPPLE} is the inductor current ripple. The input peak current is then calculated to be the maximum input current plus half of the inductor current ripple.

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of the inductor must be greater than I_{PEAK}. The inductance can then be determined by the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

Where f_{OSC} is the switching frequency. To consider the system performance, a shielded inductor is preferred to avoid EMI issue.

Boost Diode Selection

Schottky diode is a good choice for any asynchronous boost converter due to its small forward voltage. However,important parameters such as power dissipation, reverse voltage rating and pulsating peak current should be considered when selecting the Schottky diode. It is recommended to choose a suitable diode with reverse voltage rating greater than the maximum output voltage.

Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of the inductor current ripple with ESR of output capacitor, while the other part is formed by charging and discharging process of the output capacitor. As shown in Figure 3, ΔV_{OUT1} can be evaluated base on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. Bring C_{OUT} to the left side to estimate the value of ΔV_{OUT1} according to the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

when D is the duty cucle and η and the boost converter efficiency.

Finally, taking ESR into account, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

The output capacitor, C_{OUT}, sholud be selected accordingly.

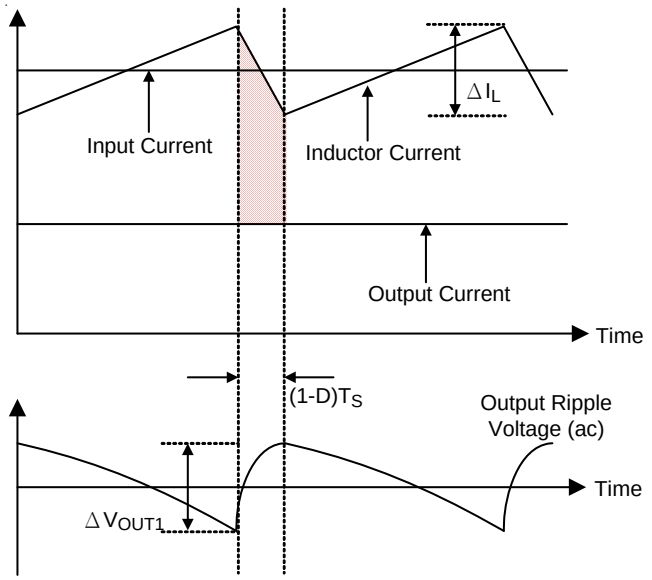


Figure 1. The Output Ripple Voltage without the Contribution of ESR

Boost Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input voltage ripple caused by the switching operation. A 20μF low ESR ceramic capacitor is sufficient for most applications. Nevertheless, this value can be decreased for applications with lower output current requirement. Another consideration is the voltage rating of the input capacitor, which must be greater than the maximum input voltage.

Buck Regulator

The buck converter is a high efficiency PWM architecture with 500kHz / 750kHz operation frequency, fast transient response and simple internal compensation. The converter drives an internal N-channel MOSFET connected between the IN2 pin and LX2 pin. Connect a 100nF low ESR ceramic capacitor between the BST pin and LX2 pin to provide gate driver voltage for the high side MOSFET.

Buck Output Voltage Setting

The regulated output voltage is shown as following the equation :

$$V_{OUT} = V_{FB2} \times \left(1 + \frac{R21}{R20} \right), \text{ where } V_{FB2} = 1.25V \text{ (typ.)}$$

Buck Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, I_L, will increase with higher V_{IN} and decrease with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{OSC} \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest operation efficiency . However, it requires a large inductor to achieve this goal. For the inductor selection, setting the value of $\Delta I_{I(MAX)}$ = 0.4 is a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left(\frac{V_{OUT}}{f_{OSC} \times \Delta I_{L(MAX)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor's current rating (causes a 40°C temperature rise from 25°C ambient) should be greater than the maximum load current, and its saturation current should be greater than the short-circuit peak current limit.

Buck Diode Selection

When the power switch turns off, the path of the current is through the diode connected between the switch output and ground. This forward biased diode must have a minimum voltage drop and quick recovery time. Schottky diodes are recommended and should be able to handle typical operation currents. Care should be given, however, to make sure that the reverse voltage rating of the diode is greater than the maximum input voltage, and the current rating is greater than the maximum load current.

Buck Input Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10µF x 2 low ESR ceramic capacitor is recommended.

Buck Output Capacitor Selection

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, V_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

The output ripple will be highest at the maximum input voltage since I_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Suitable candidates such as dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications requiring high ripple current rating and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Nevertheless higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at

the input and output. When a ceramic capacitor is used at the input and V_{IN} the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

LDO Current Limit

The HVLDO contains an independent current-limit mechanism, which monitors and controls the pass transistor's gate voltage to limit the output current. It can protect the IC even when directly shorting the output to GND.

LDO Output Voltage Setting

The regulated output voltage can be calculated as the following equation :

$$V_{REF} = V_{REF\_FB} \times \left(1 + \frac{R6}{R7}\right), \text{ where } V_{REF\_FB} = 1.25V \text{ (typ.)}$$

The recommended value for R6 is up to 10kΩ without any side-effects. Place the resistor divider as close as possible to the chip to reduce noise sensitivity.

GPM

The GPM is controlled by frame signals from the timing controller to modulate the Gate-On voltage and acts as a flicker compensation circuit to reduce the coupling effect between gate lines and pixels. It can also delay the Gate-On voltage while in power on for achieving a correct power on sequence for gate driver ICs. Both, the power on delay time and the falling time of the Gate-On voltage, are programmable by an external capacitor and resistor. The delay time is programmable by an external capacitor (C9). Moreover, when GVOFF is low, VGHM falling stop level is 10 times the voltage on the THR pin. However, this gain ratio will be increase if V_{THR} higher than 1.5V. The following figure illustrates the corresponding VGHM stop level within the THR voltage.

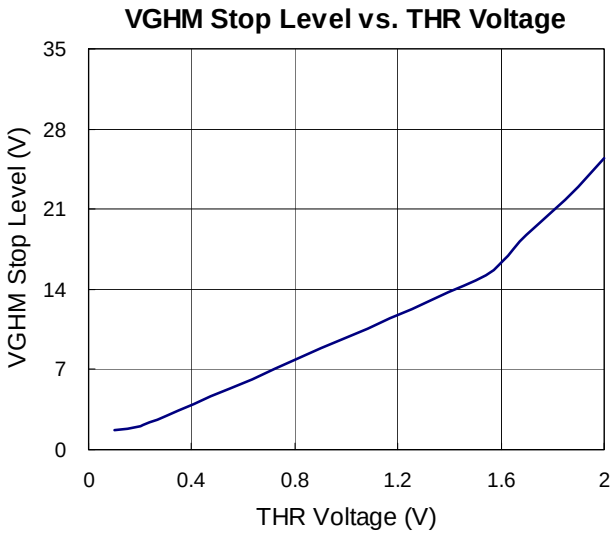


Figure 2

Operational Amplifier

The function of the operational amplifier is to supply the LCD backplane, V_{COM}. The operational amplifier features ±300mA output short-circuit current, 45V/μs slew rate, and 20MHz bandwidth. An internal short-circuit protection circuit is implemented to protect the device from output short-circuit.

Voltage Detector

The voltage detector monitors the VDET pin voltage to generate a reset signal when VDET is lower than the detecting level and the detecting level is determined by an external resistor divider.

$$\text{Reset Voltage} = V_{DET} \times \left(1 + \frac{R17}{R19}\right) = 1.25V \times \left(1 + \frac{R17}{R19}\right)$$

$$V_{HYS} = 50mV \times \left(1 + \frac{R17}{R19}\right), \text{ where } V_{HYS} \text{ is the Hysteresis}$$

Positive Charge-Pump Regulator

The positive charge pump provides high level voltage for the TFT gate driver. The charge pump can provide a programmable output voltage by setting the resistive voltage-divider sensing at the FBP pin. The error amplifier varies the differential voltage by sensing FBP pin to regulate the output voltage as the following equation :

$$V_{GH} = V_{FBP} \times \left(1 + \frac{R8}{R9}\right)$$

Where V_{FBP} is the reference voltage and the typical value is 1.25V.

Negative Charge Pump Regulator

The operation of the negative charge pump is similar to the positive charge pump. The negative charge pump provides low level voltage for the TFT gate driver. The charge pump can provide a programmable output voltage by setting the resistive voltage divider sensing at the FBN pin. The error amplifier varies the differential voltage by sensing FBN pin to regulate the output voltage as the following equation :

$$V_{GL} = V_{FBN} - (V_{REF} - V_{FBN}) \times \frac{R14}{R13}$$

Where V_{REF} is the reference voltage on pin and the typical value is 1.25V. V_{FBN} is the reference voltage and the typical value is 0.25V

Over-Temperature Protection

The RT9955 boost converter has a thermal protection function to prevent overheating from excessive power dissipation. When the junction temperature exceeds 160°C, it will shut down the all switching signals and the GD pin will pull high.

Layout Consideration

For high frequency switching power supplies, a correct PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short enough especially for the high-current loop.
- The feedback voltage-divider resistors must be near the feedback pin. The divider center trace must be short and the trace must be kept away from any switching nodes.
- The compensation circuit should be kept away from the power loops and be shielded with a ground trace to prevent any noise coupling.
- Minimize the size of the LX node and keep it wide and short. Keep the LX node away from the FB.
- The Exposed Pad of the chip should be connected to a strong ground plane for maximum thermal consideration.

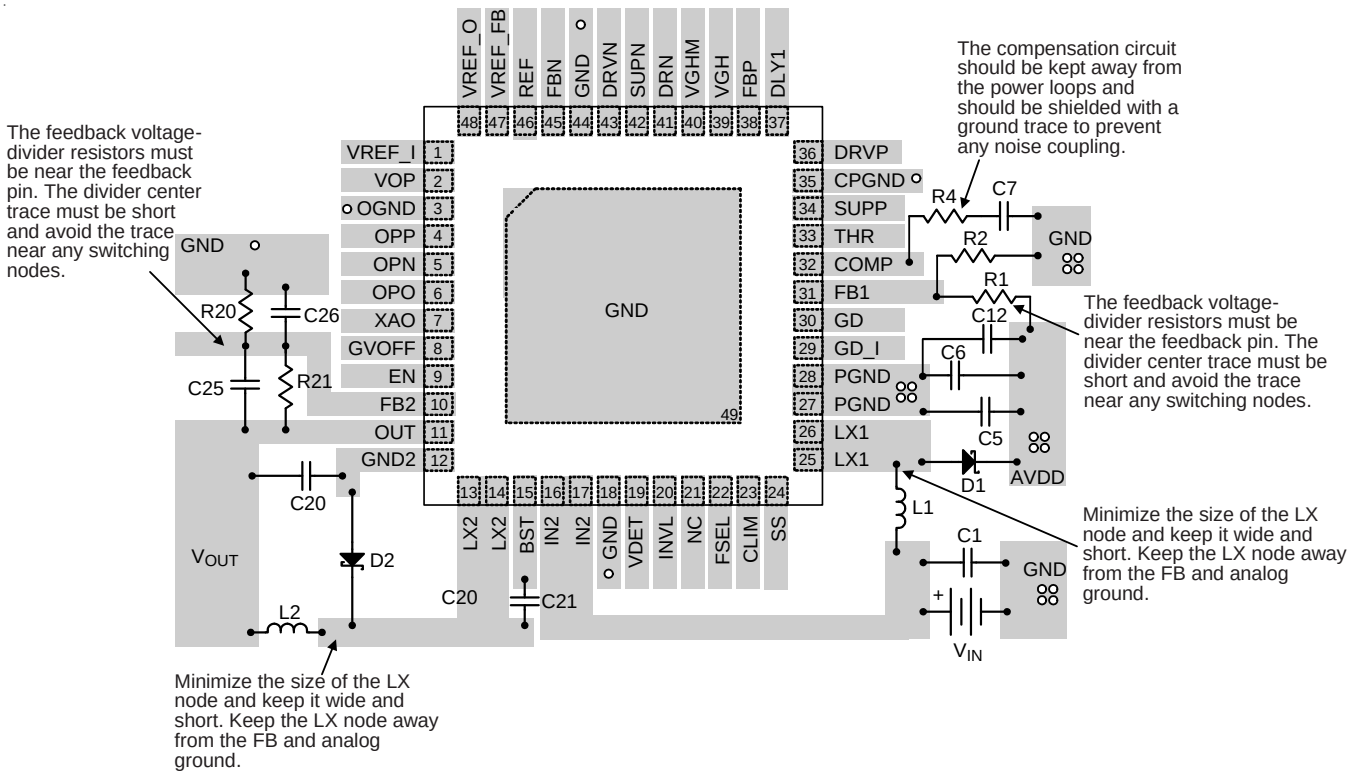
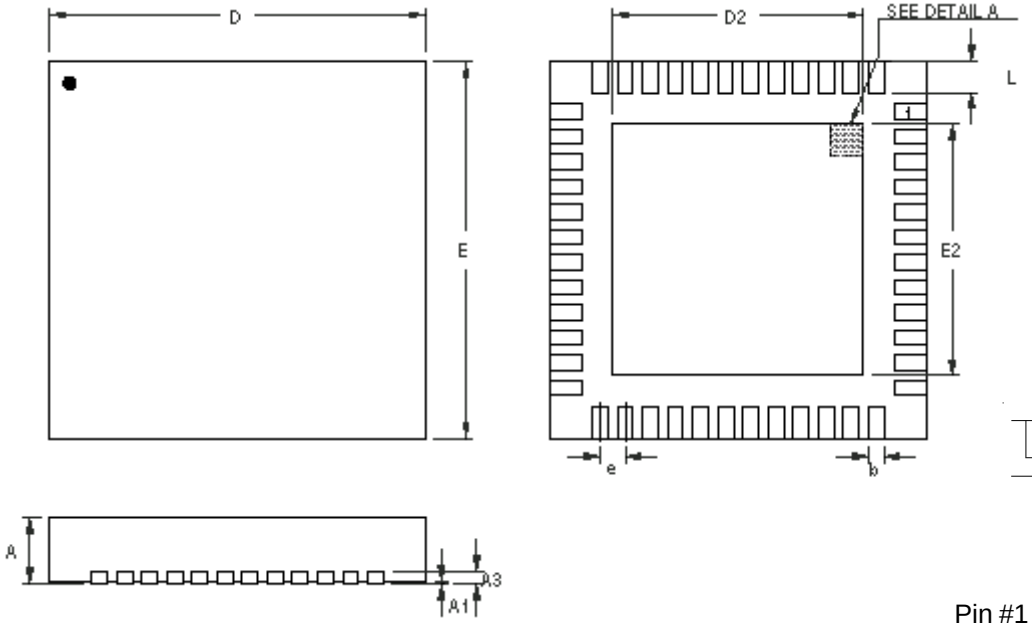


Figure 3. PCB Layout Guide

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	6.950	7.050	0.274	0.278
D2	5.050	5.250	0.199	0.207
E	6.950	7.050	0.274	0.278
E2	5.050	5.250	0.199	0.207
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 48L QFN 7x7 Package

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