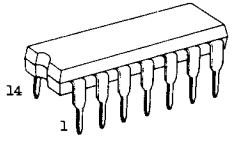
TC5026BP

TC5026BP DECADE COUNTER

TC5026BP is DECADE UP COUNTER with two reset functions, RESET (9) and RESET (0) and can be used as binary counter, quinary counter or decimal counter. When two inputs of RESET (0) are set to "H", the content of counter is reset to 0 regardless of the clock and when two inputs of RESET (9) are set to "H", it is set to 9.
RESET (9) takes precedance over RESET (0).
The outputs change their states at the falling edge of count inputs (IN_A and IN_B).

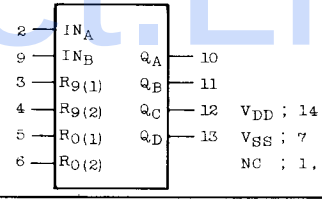


DIP 14 (3D14A-P)

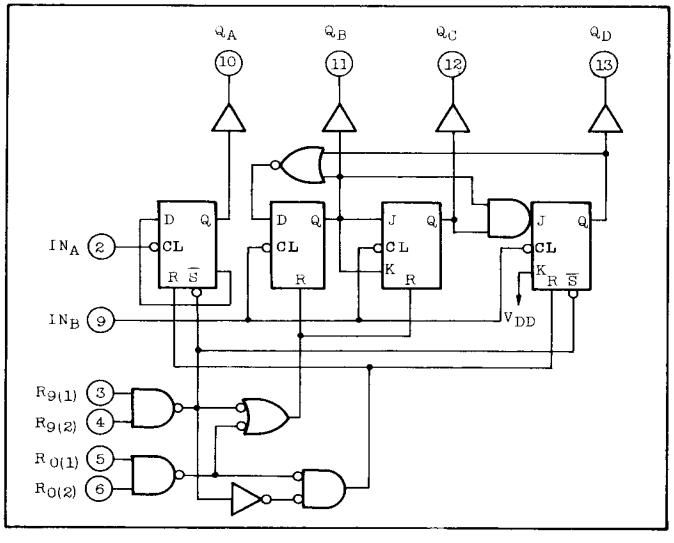
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

RESET / COUNT MODE

INPUTS					OUTPUTS			
IN_A, IN_B	$R_{O(1)}$	$R_{O(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
*	H	H	L	*	L	L	L	L
*	H	H	*	L	L	L	L	L
*	*	*	H	H	H	L	L	H
↓	*	L	*	L	COUNT			
↓	L	*	L	*	COUNT			
↓	L	*	*	L	COUNT			
↓	*	L	L	*	COUNT			

* Don't care

COUNT MODE A

COUNT NO.	OUTPUTS		
	Q_D	Q_C	Q_B
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

A ; Separate mode.
B ; IN_B should be connected to Q_A

COUNT MODE B

COUNT NO.	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN} = V_{SS}, V_{DD}$	5	-0.2	-	-0.16		-	-0.12	-	mA
			10	-0.5	-	-0.4		-	-0.3	-	
			15	-1.4	-	-1.2		-	-1.0	-	
Low Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}, V_{DD}$	5	0.52	-	0.44		-	0.36	-	
			10	1.3	-	1.1		-	0.9	-	
			15	3.6	-	3.0		-	2.4	-	
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
			15	-	80	-	0.015	80	-	600	

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

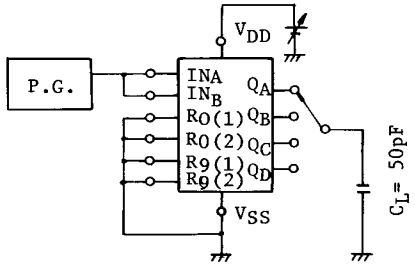
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
(LOW-HIGH) Propagation Delay Time (IN_A, IN_B - Q)	tpLH		5	-	340	750	ns
			10	-	160	350	
			15	-	130	280	
(HIGH-LOW) Propagation Delay Time (IN_A, IN_B - Q)	tpHL		5	-	310	650	
			10	-	150	330	
			15	-	120	250	
(LOW-HIGH) Propagation Delay Time ($R_{(0)}$, $R_{(9)}$ - Q)	tpLH		5	-	350	700	ns
			10	-	150	300	
			15	-	120	250	
(HIGH-LOW) Propagation Delay Time ($R_{(0)}$, $R_{(9)}$ - Q)	tpHL		5	-	350	700	
			10	-	150	300	
			15	-	120	250	
Max. Clock Rise Time Max. Clock Fall Time	t_{rCL} t_{fCL}		5	20	-		μs
			10	2.5	-		
			15	1.0	-		
Max. Clock Frequency (IN_A, IN_B)	t_{CL}		5	0.8	1.2	-	MHz
			10	1.5	2.5	-	
			15	2.0	3.2	-	
Min. Reset Pulse Width	t_w (RESET)		5	-	250	500	ns
			10	-	100	200	
			15	-	75	150	
Input Capacity	C_{IN}			-	5	7.5	pF

SWITCHING TIME TEST CIRCUIT

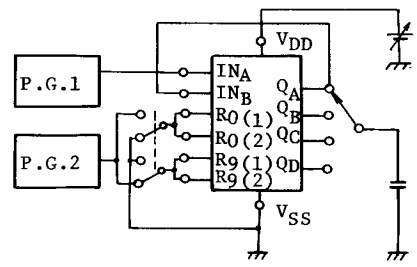
TEST CIRCUIT 1 tpLH,tpHL(IN_A,IN_B-Q)

f_{CL}



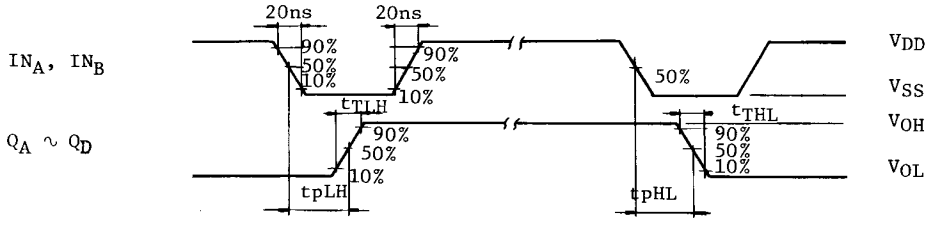
TEST CIRCUIT 2 tpLH,tpHL(R_0,R_9-Q)

t_w



SWITCHING TIME TEST WAVEFORMS

WAVEFORM 1. tpLH, tpHL (IN_A,IN_B - Q), f_{CL}



WAVEFORM 2. tpLH, tpHL [$R_{(0)}$,$R_{(9)}$ - Q], t_w