Ordering number : EN5065A

CMOS LSI

LC72358N, 72362N, 72366

Single-Chip PLL Microcontrollers

Overview

The LC72358N, LC72362N, and LC72366 are 1.33 µs instruction execution time single-chip microcontrollers for electronic tuning applications. These products incorporate a high-speed locking circuit and a high-performance direct PLL circuit that can control the local oscillator C/N characteristics. These products have 256 or 512 bytes of RAM and 16K, 24K or 32K bytes of program ROM on chip, and incorporate a three-channel serial I/O interface, a six-channel A/D converter and other interfaces.

Features

- ROM
  - — LC72358N: 8K steps (8191 × 16 bits)
  - — LC72362N: 12K steps (12287 × 16 bits)
  - — LC72366: 16K steps (16383 × 16 bits)

  The subroutine area in both products is 4K steps (4095 × 16 bits).
- RAM
  - — LC72358N, 72362N: 512 × 4 bits (banks 0 to 7)
  - — LC72366: 1K × 4 bits (banks 0 to F)
- Stack: Eight levels
- Serial I/O: Three channels (8-bit 3-wire format)

  There are three internal serial clocks: 12.5 kHz, 37.5 kHz and 187.5 kHz.
- External interrupts:

  Two channels (the INT0 and INT1 pins)

  Switching between rising and falling edge detection is supported.
- Internal interrupts:

  Three channels
  - — Two internal timer interrupt channels

    The timers provide eight interrupt periods: 100 µs, 1 ms, 2 ms, 5 ms, 10 ms, 50 ms, 125 ms and 250 ms.
  - — One serial I/O interrupt channel
- Multiple interrupt levels:

  Four levels

  Hardware priority order

  INT0 pin > INT1 pin > SI/O pin > internal timer 0 > internal timer 1
- A/D converter: Six channels (6-bit successive approximation type)
- General-purpose ports
  - — Input ports: 10
  - — Output ports: 28
  - — I/O ports: 25 (These pins can be switched between input and output in bit units.)
- PLL block
  - — Built-in sub-charge pump for high-speed locking
  - — Support for dead zone control
  - — Built-in unlock detection circuit
  - — Twelve reference frequencies: 1, 3, 3.125, 5, 6.25, 9, 10, 12.5, 25, 30, 50 and 100 kHz
- Universal counter: 20 bits

  Supports frequency and period measurement with counting periods of 1, 4, 8 and 32 ms.
- Timers: Timer interrupt periods

  100 µs, 1 ms, 2 ms, 5 ms, 10 ms, 50 ms, 125 ms and 250 ms
- Beep: Six frequencies: 2.08 kHz, 2.25 kHz, 2.5 kHz, 3.0 kHz, 3.75 kHz, 4.17 kHz.
- Reset: Built-in voltage detection type reset circuit
- Cycle time: 1.33 µs (all instructions execute in one cycle)
- Halt mode: The microcontroller operating clock is stopped in halt mode.

  There are four types of event that clear halt mode: interrupt requests, timer FF overflows, key inputs, and hold pin inputs.
- Operating supply voltage: 4.5 to 5.5 V (3.5 to 5.5 V when only the controller block operates)
- Package: QFP80E (QIP80E)
- OTP version: LC72P366
- Development tools: Emulator RE32N

  Evaluation chip.....LC72EV350

  Evaluation chip board EB-72EV350

This LSI can easily use CCB that is SANYO's original bus format.

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

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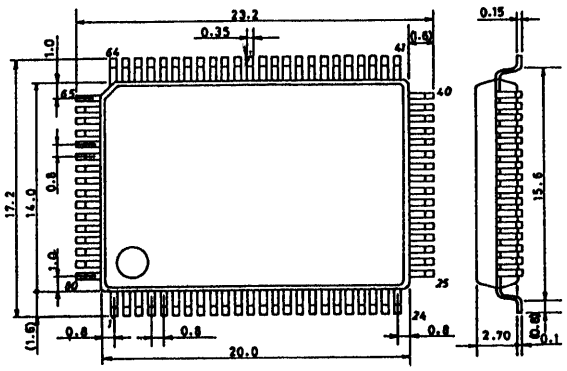
Package Dimensions

unit: mm

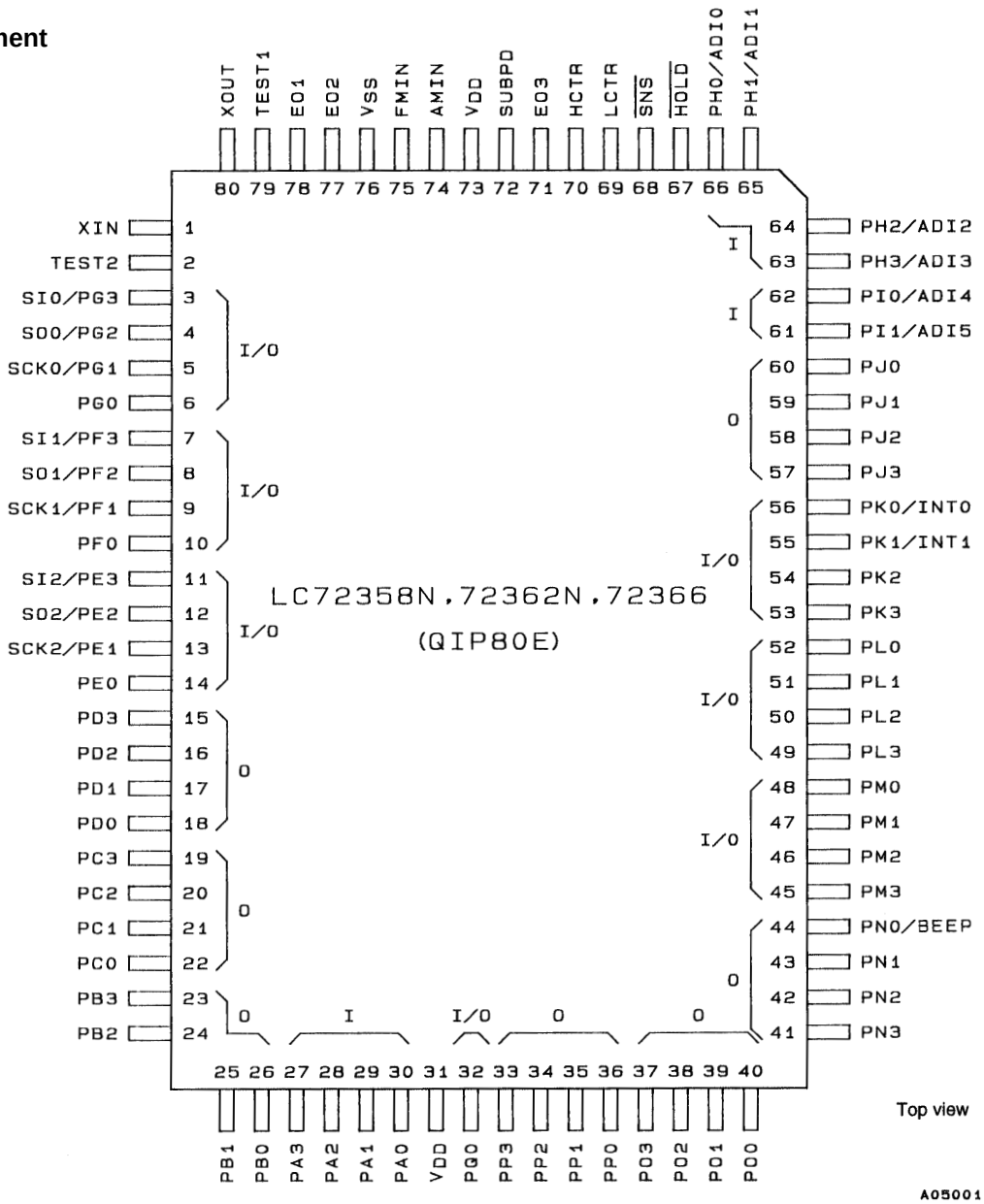
3174-QFP80E

[LC72358N, 72362N, 72366]

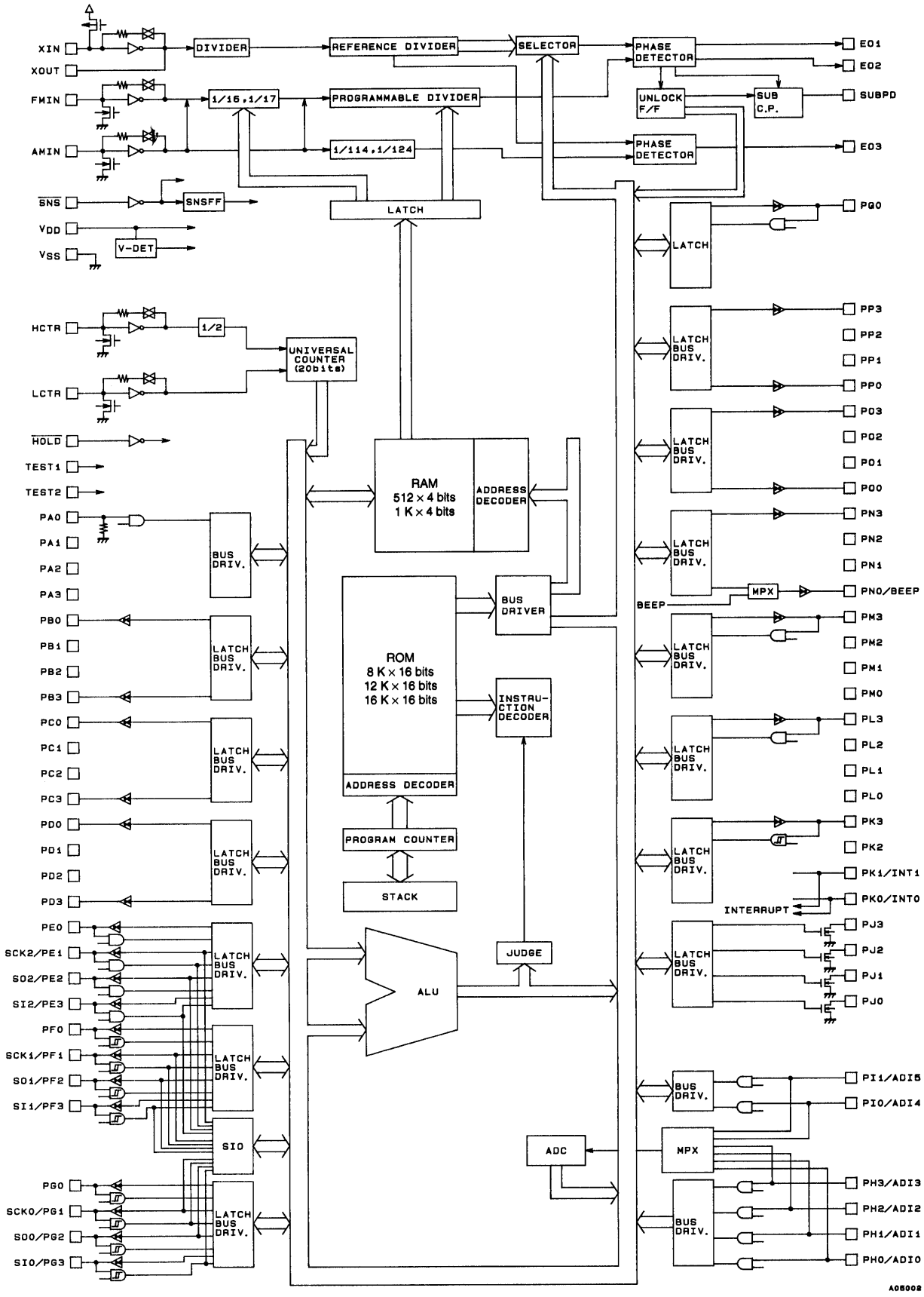


SANYO: QIP80E

Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.5	V
Input voltage	V_{IN}	All input pins	–0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT} (1)	J port	–0.3 to +15	V
	V_{OUT} (2)	All output ports other than V_{OUT} (1)	–0.3 to V_{DD} + 0.3	V
Output current	I_{OUT} (1)	J port	0 to 5	mA
	I_{OUT} (2)	D, E, F, G, K, L, M, N, O, P and Q ports, EO1, EO2, EO3, SUBPD	0 to 3	mA
	I_{OUT} (3)	B and C ports	0 to 1	mA
Allowable power dissipation	Pd max	Ta = –40 to +85°C	400	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–45 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 3.5 to 5.5 V

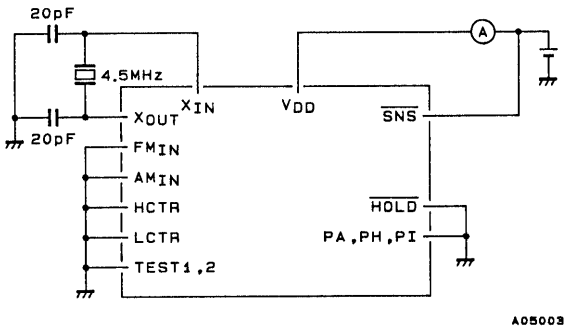
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD} (1)	CPU and PLL operating	4.5	5.0	5.5	V
	V_{DD} (2)	CPU operating	3.5		5.5	V
	V_{DD} (3)	Memory retention	1.3		5.5	V
Input high level voltage	V_{IH} (1)	E, H, I, L, M and Q ports, HCTR and LCTR (when selected for input)	0.7 V_{DD}		V_{DD}	V
	V_{IH} (2)	F, G and K ports, LCTR (period measurement mode), $\overline{HOLD}$	0.8 V_{DD}		V_{DD}	V
	V_{IH} (3)	$\overline{SNS}$	2.5		V_{DD}	V
	V_{IH} (4)	A port	0.6 V_{DD}		V_{DD}	V
Input low level voltage	V_{IL} (1)	E, H, I, L, M and Q ports, HCTR and LCTR (when selected for input)	0		0.3 V_{DD}	V
	V_{IL} (2)	A, F, G and K ports, LCTR (period measurement mode)	0		0.2 V_{DD}	V
	V_{IL} (3)	$\overline{SNS}$	0		1.3	V
	V_{IL} (4)	$\overline{HOLD}$	0		0.4 V_{DD}	V
Input frequency	f_{IN} (1)	XIN	4.0	4.5	5.0	MHz
	f_{IN} (2)	FMIN: V_{IN} (2), V_{DD} (1)	10		150	MHz
	f_{IN} (3)	FMIN: V_{IN} (3), V_{DD} (1)	10		130	MHz
	f_{IN} (4)	AMIN (H): V_{IN} (3), V_{DD} (1)	2.0		40	MHz
	f_{IN} (5)	AMIN (L): V_{IN} (3), V_{DD} (1)	0.5		10	MHz
	f_{IN} (6)	HCTR: V_{IN} (3), V_{DD} (1)	0.4		12	MHz
	f_{IN} (7)	LCTR: V_{IN} (3), V_{DD} (1)	100		500	kHz
	f_{IN} (8)	LCTR (period measurement): V_{IH} (2), V_{IL} (2), V_{DD} (1)	1		20×10^3	Hz
Input amplitude	V_{IN} (1)	XIN	0.5		1.5	Vrms
	V_{IN} (2)	FMIN	0.10		1.5	Vrms
	V_{IN} (3)	FMIN, AMIN, HCTR, LCTR	0.07		1.5	Vrms
Input voltage range	V_{IN} (4)	ADI0 to ADI5	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level current	I_{IH} (1)	XIN: $V_I = V_{DD} = 5.0$ V	2.0	5.0	15	µA
	I_{IH} (2)	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD} = 5.0$ V	4.0	10	30	µA
	I_{IH} (3)	A, E, F, G, H, I, K, L, M and Q ports, $\overline{SNS}$, $\overline{HOLD}$, HCTR, LCTR, with no pull-down resistor on A port. $V_I = V_{DD} = 5.0$ V, with the E, F, G, K, L, M and Q ports selected for input.			3.0	µA
	I_{IH} (4)	A port: pull-down resistor present, $V_I = V_{DD} = 5.0$ V		50		µA
Input low level current	I_{IL} (1)	XIN: $V_I = V_{SS}$	2.0	5.0	15	µA
	I_{IL} (2)	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	µA
	I_{IL} (3)	A, E, F, G, H, I, K, L, M and Q ports, $\overline{SNS}$, $\overline{HOLD}$, HCTR, LCTR, with no pull-down resistor on A port. $V_I = V_{SS}$, with the E, F, G, K, L, M and Q ports selected for input.			3.0	µA
Input floating voltage	V_{IF}	A port: pull-down resistor present			0.05 V_{DD}	V
Pull-down resistance	R_{PD} (1)	A port: pull-down resistor present, $V_{DD} = 5$ V	75	100	200	kΩ
Hysteresis	V_H	F, G and K ports, LCTR (period measurement mode)	0.1 V_{DD}	0.2 V_{DD}		V
Output high level voltage	V_{OH} (1)	B and C ports: $I_O = -1$ mA	V_{DD} – 2.0	V_{DD} – 1.0		V
	V_{OH} (2)	D, E, F, G, K, L, M, N, O, P and Q ports: $I_O = -1$ mA	V_{DD} – 1.0			V
	V_{OH} (3)	EO1, EO2, EO3, SUBPD: $I_O = -500$ µA	V_{DD} – 1.0			V
	V_{OH} (4)	XOUT: $I_O = -200$ µA	V_{DD} – 1.0			V
Output low level voltage	V_{OL} (1)	B and C ports: $I_O = 50$ µA		1.0	2.0	V
	V_{OL} (2)	D, E, F, G, K, L, M, N, O, P and Q ports: $I_O = 1$ mA			1.0	V
	V_{OL} (3)	EO1, EO2, EO3, SUBPD: $I_O = 500$ µA			1.0	V
	V_{OL} (4)	XOUT: $I_O = 200$ µA			1.5	V
	V_{OL} (5)	J port: $I_O = 5$ mA			2.0	V
Output off leakage current	I_{OFF} (1)	B, C, D, E, F, G, K, L, M, N, O, P and Q ports	–3.0		+3.0	µA
	I_{OFF} (2)	EO1, EO2, EO3, SUBPD	–100		+100	nA
	I_{OFF} (3)	J port	–5.0		+5.0	µA
A/D conversion error		ADI0 to ADI5: V_{DD} (1)	–1/2		+1/2	LSB
Reject pulse width	P_{REJ}	$\overline{SNS}$			50	µs
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Pull-down resistance	R_{PD} (2)	TEST1, TEST2		10		kΩ
Current drain	I_{DD} (1)	V_{DD} (1): f_{IN} (2) = 130 MHz, Ta = 25°C		12	24	mA
	I_{DD} (2)	V_{DD} (2): Halt mode*, Ta = 25°C (Figure 1)		0.45	(0.9)	mA
	I_{DD} (3)	V_{DD} = 5.5 V, oscillator stopped, Ta = 25°C (Figure 2)			5	µA
	I_{DD} (4)	V_{DD} = 2.5 V, oscillator stopped, Ta = 25°C (Figure 2)			1	µA

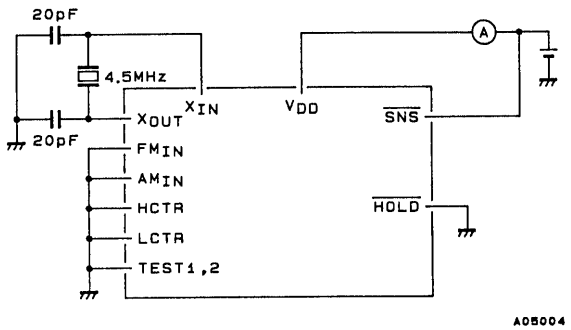
Note: Execute 20 STEP instructions every 1 ms. With the PLL, counters and other functions all stopped.
( ) Value: LC72366

Test Circuit



Note: All of the pins PB to PG and PJ to PQ must be left open.
Here, the pins PE to PG, PK to PM, and PQ are selected for output.

Figure 1: I_{DD}(2) in Halt Mode



Note: All of the pins PA to PQ must be left open.

Figure 2. I_{DD}(3) and I_{DD}(4) in Backup Mode

Pin Functions

Pin No.	Symbol	I/O	I/O type	Function
30 29 28 27	PA0 PA1 PA2 PA3	I	Pull-down resistor included Input	Key return signal input-only ports. The threshold voltage is set to a relatively low value. When a key matrix is formed in combination with the PB and PC ports, up to three simultaneous key presses can be detected. The pull-down resistors are set by the IOS instruction with PWn = 2 for all four pins at the same time and cannot be set on an individual pin basis. Input is disabled in clock stop mode.
26 25 24 23 22 21 20 19	PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	O	Unbalanced CMOS push-pull	Key source signal output-only ports. Since the output transistor circuit is an unbalanced CMOS structure, diodes to prevent shorting due to multiple key presses are not required. In clock stop mode, these pins go to the output high-impedance state. During the power-on reset, these pins go to the output high-impedance state and hold that state until an output instruction is executed.
18 17 16 15	PD0 PD1 PD2 PD3	O	CMOS push-pull	Output-only ports. In clock stop mode, these pins go to the output high-impedance state. During the power-on reset, these pins go to the output high-impedance state and hold that state until an output instruction is executed.
14 13 12 11 10 9 8 7 6 5 4 3	PE0 PE1/SCK2 PE2/SO2 PE3/SI2 PF0 PF1/SCK1 PF2/SO1 PF3/SI1 PG0 PG1/SCK0 PG2/SO0 PG3/SI0	I/O	CMOS push-pull	General-purpose I/O port/serial I/O pin shared-function ports. The F and G port inputs are Schmitt inputs. The E ports is a normal input. The IOS instruction switches these ports between general-purpose I/O ports and serial I/O ports, and between input and output for general-purpose I/O ports. • When used as general-purpose I/O ports these pins: Can be set for input or output in bit units (bit I/O), and are set for use as general-purpose I/O ports by the IOS instruction with PWn = 0. b0 = SI/O 0 0 .....general-purpose port b1 = SI/O 1 1 .....SI/O port b2 = SI/O 2 are set for input or output by the IOS instruction in bit units. PE.....PWn = 4 0 .....Input PF.....PWn = 5 1 .....Output PG .....PWn = 6 • When used as serial I/O ports these pins: Are set for serial I/O port use by the IOS instruction with PWn = 0, and are accessed by reading and writing the serial I/O data buffer with the INR and OUTR instructions. Note: Pin setup states when used as serial I/O ports: PE0, PF0, PG0 .....General-purpose I/O PE1, PF1, PG1 .....SCK output in internal clock mode SCK input in external clock mode PE2, PF2, PG2.....SO output PE3, PF3, PG3.....SI input In clock stop mode, input is disabled and these pins go to the high-impedance state. During the power-on reset, these pins become general-purpose input ports.
1 80	XIN XOUT	I O	—	Connections for a 4.5 MHz crystal oscillator
78 77	EO1 EO2	O	CMOS tristate	Main charge pump outputs These pins output a high level when the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, and a low level when that frequency is lower. These pins go to the high-impedance state when the frequencies match. These pins go to the high-impedance state when the $\overline{\text{HOLD}}$ pin is set low in the hold enable state. In clock stop mode, during the power-on reset and in the PLL stop state, these pins go to the high-impedance state.

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<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>I/O type</th><th>Function</th></tr>
<tr><td>76
73
31</td><td>V_{SS}
V_{DD}
V_{DD}</td><td>—</td><td>—</td><td>Power supply connections</td></tr>
<tr><td>75</td><td>FMIN</td><td>I</td><td>Input</td><td>FM VCO (local oscillator) input
This pin is selected by the PLL instruction CW1 (b1, b0 are ignored).
Capacitor coupling must be used for signal input.
Input is disabled when the $\overline{\text{HOLD}}$ pin is set low in the hold enable state.
Input is disabled in clock stop mode, during the power-on reset, and in the PLL stop state.</td></tr>
<tr><td>74</td><td>AMIN</td><td>I</td><td>Input</td><td>AM VCO (local oscillator) input
This pin is selected and the band set by the PLL instruction CW1 (b1, b0).
<table><tr><th>b1</th><th>b0</th><th>Band</th></tr><tr><td>1</td><td>0</td><td>2 to 40 MHz (SW)</td></tr><tr><td>1</td><td>1</td><td>0.5 to 10 MHz (MW, LW)</td></tr></table>
Capacitor coupling must be used for signal input.
Input is disabled when the $\overline{\text{HOLD}}$ pin is set low in the hold enable state.
Input is disabled in clock stop mode, during the power-on reset, and in the PLL stop state.</td></tr>
<tr><td>72</td><td>SUBPD</td><td>O</td><td>CMOS tristate</td><td>Sub-charge pump output
This pin, in combination with the main charge pump, allows the construction of a high-speed locking circuit.
The DZC instruction controls the sub-charge pump.
<table><tr><th>b3</th><th>b2</th><th>Operation</th></tr><tr><td>0</td><td>0</td><td>High impedance</td></tr><tr><td>0</td><td>1</td><td>Only operates in the unlocked state (450 kHz)</td></tr><tr><td>1</td><td>0</td><td>Only operates in the unlocked state (900 kHz)</td></tr><tr><td>1</td><td>1</td><td>Normal operation</td></tr></table>
This pin goes to the high-impedance state when the $\overline{\text{HOLD}}$ pin is set low in the hold enable state.
This pin goes to the high-impedance state in clock stop mode, during the power-on reset, and in the PLL stop state.</td></tr>
<tr><td>71</td><td>EO3</td><td>O</td><td>CMOS tristate</td><td>Second PLL charge pump output
This pin outputs a low level when the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, and a high level when that frequency is lower.
This pin goes to the high-impedance state when the frequencies match. (Note that this pin's output logic is the opposite of that of the EO1 and EO2 pins.)
This pin goes to the high-impedance state when the $\overline{\text{HOLD}}$ pin is set low in the hold enable state.
This pin goes to the high-impedance state in clock stop mode, during the power-on reset, and in the PLL stop state.</td></tr>
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Pin No.	Symbol	I/O	I/O type	Function
70	HCTR	I	Input	Universal counter/general-purpose input shared-function input port The IOS instruction b3 with PWn = 3 switches the pin function between universal counter input and general-purpose input. • Frequency measurement The universal counter function is selected by an IOS instruction with PWn = 3 and b3 = 0. HCTR frequency measurement mode is set up by a UCS instruction with b3 = 0 and b2 = 0, and counting is started with a UCC instruction after the count time is selected. The CNTEND flag is set when the count completes. To operate this circuit as an AC amplifier in this mode, the input must be capacitor coupled. • General-purpose input pin use The general-purpose input port function is selected by an IOS instruction with PWn = 3 and b3 = 1. An internal register (address: 0EH) input instruction INR (b0) is used to acquire data from this pin. Input is disabled in clock stop mode. (The input pin will be pulled down.) During the power-on reset, the universal counter function is selected.
69	LCTR	I	Input	Universal counter (frequency and period measurement)/general-purpose input shared-function input port The IOS instruction b2 with PWn = 3 switches the pin function between universal counter input and general-purpose input. • Frequency measurement The universal counter function is selected by an IOS instruction with PWn = 3 and b2 = 0. LCTR frequency measurement mode is set up by a UCS instruction with b3 = 0 b2 = 1, and counting is started with a UCC instruction after the count time is selected. The CNTEND flag is set when the count completes. To operate this circuit as an AC amplifier in this mode, the input must be capacitor coupled. • Period measurement With the universal counter function selected, set up period measurement mode with a UCS instruction with b3 = 1 and b2 = 0, and start the count with a UCC instruction after selecting the count time. The CNTEND flag will be set when the count completes. In this mode, the signal must be input with DC coupling to turn off the bias feedback resistor. • General-purpose input pin use The general-purpose input port function is selected by an IOS instruction with PWn = 3, b2 = 1. An internal register (address: 0EH) input instruction INR (b1) is used to acquire data from this pin. Input is disabled in clock stop mode. (The input pin will be pulled down.) During the power-on reset, the universal counter function (in HCTR frequency measurement mode) is selected.
68	$\overline{\text{SNS}}$	I	Input	Voltage sense/general-purpose input pin shared-function port This circuit is designed for a relatively low input threshold voltage. • Voltage sense pin usage This input pin is used to determine whether or not a power failure occurred after recovery from backup (clock stop) mode. An internal sense F/F is used for this determination. The sense F/F is tested with a TUL instruction (b2). • General-purpose input port usage When used as a general-purpose input port, the state is sensed by using a TUL instruction (b3). Since, unlike other input ports, input is not disabled in clock stop mode and during the power-on reset, special care is required with respect to through currents.

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Pin No.	Symbol	I/O	I/O type	Function
67	$\overline{\text{HOLD}}$	I	Input	PLL control and clock stop mode control Setting this pin low in the hold enabled state disables input to the FMIN and AMIN pins and sets the EO pin to the high-impedance state. To enter clock stop mode, set the HOLDEN flag, set this pin low, and execute a CKSTP instruction. To clear clock stop mode, set this pin high.
66 65 64 63 62 61	PH0/ADI0 PH1/ADI1 PH2/ADI2 PH3/ADI3 PI0/ADI4 PI1/ADI5	I	Input	General-purpose input port/A/D converter shared-function pins The IOS instruction with PWn = 7 or 8 switches the pin function between general-purpose input ports and A/D converter inputs. • General-purpose input port usage Specify general-purpose input port usage with the IOS instruction with PWn = 7 or 8 in bit units. • A/D converter usage Specify A/D converter usage with the IOS instruction with PWn = 7 or 8 in bit units. Specify the pin to convert with the IOS instruction with PWn = 1. Start a conversion with the UCC instruction (b2). The ADCE flag will be set when the conversion competes. Note: Executing an input instruction for a port specified for ADI usage will always return low since input is disabled. These pins must be set up for general-purpose input port usage before an input instruction is executed. Input is disabled in clock stop mode. During the power-on reset, these pins go to the general-purpose input port function.
60 59 58 57	PJ0 PJ1 PJ2 PJ3	O	N-channel open drain	General-purpose output ports An external pull-up resistor is required since these pins are open-drain circuits. In clock stop mode, these pins go to the transistor off state (high level output). During the power-on reset, these pins are set up as general-purpose output ports and go to the transistor off state (high level output).
56 55 54 53	PK0/INT0 PK1/INT1 PK2 PK3	I/O	CMOS push-pull	General-purpose I/O/external interrupt shared-function ports There is no instruction that switches the function of these ports between general-purpose ports and external interrupt ports. These pins function as external interrupt pins at the point that the external interrupt enable flag is set. • General-purpose I/O port usage These pins can be set for input or output in bit units (bit I/O). The IOS instruction is used to specify input or output in bit units. • External interrupt pin usage This function can be used by setting the external interrupt enable flags (INT0EN and INT1EN) in status register 2. The corresponding pin must be set up for input. To enable interrupt operation, the interrupt enable flag (INTEN) in status register 1 also must be set. The IOS instruction with PWn = 3, b1 = INT1, and b0 = INT0 is used to select rising or falling edge detection. In clock stop mode, input is disabled and these pins go to the high impedance state. During the power-on reset, these pins function as general-purpose input ports.
52 to 45	PL0 to PL3 PM0 to PM3	I/O	CMOS push-pull	General-purpose I/O ports The IOS instruction is used to specify input or output. In clock stop mode input is disabled and these pins go to the high impedance state. During the power-on reset, these pins function as general-purpose input ports.

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Pin No.	Symbol	I/O	I/O type	Function
44 43 42 41	PN0/BEEP PN1 PN2 PN3	O	CMOS push-pull	General-purpose output port/BEEP tone shared-function output pins The BEEP instruction switches between the general-purpose output port and BEEP tone functions. • General-purpose output port usage The BEEP instruction with b3 = 0 sets up the general-purpose output port function. Pins PN1 to PN3 are general-purpose output-only pins. • BEEP output usage The BEEP instruction with b3 = 1 sets up BEEP output. The BEEP instruction bits b0, b1 and b2 sets the frequency. When set up as the BEEP port, executing an output instruction will set the internal latch data but has no influence on the output. These pins go to the output high-impedance state in clock stop mode. These pins go to the output high-impedance state during the power-on reset and hold that state until an output instruction is executed.
40 to 33	PO0 to PO3 PP0 to PP3	O	CMOS push-pull	Output-only ports These pins go to the output high-impedance state in clock stop mode. These pins go to the output high-impedance state during the power-on reset and hold that state until an output instruction is executed.
32	PQ0	I/O	CMOS push-pull	General-purpose I/O ports The IOS instruction is used to specify input or output. The OUTR and INR instructions are used for output and input. The bit set, reset and test instruction cannot be used. In clock stop mode input is disabled and these pins go to the high impedance state. During the power-on reset, these pins function as general-purpose input ports.
79 2	TEST1 TEST2			LSI test pins These pins must be either left open or connected to ground.

LC72358N, LC72362N and LC72366 Instruction Table

Abbreviations:

ADDR: Program memory address
b: Borrow
C: Carry
D_H: Data memory address high (row address): 2 bits
D_L: Data memory address low (column address):4 bits
I: Immediate data:4 bits
M: Data memory address
N: Bit position
Pn: Port number:4 bits
PWn: Port control word number: 4 bits
r: General register (one of banks 00 to 0FH)
Rn: Register number:4 bits
( ): Contents of register or memory
( )N: Contents of bit N of register or memory

Instruction Group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	D_H		D_L				r			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M) skip if carry	0	1	0	0	0	1	D_H		D_L				r			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	D_H		D_L				r			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	D_H		D_L				r			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	D_H		D_L				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I skip if carry	0	1	0	1	0	1	D_H		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	D_H		D_L				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C skip if carry	0	1	0	1	1	1	D_H		D_L				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) – (M)	0	1	1	0	0	0	D_H		D_L				r			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) – (M) skip if borrow	0	1	1	0	0	1	D_H		D_L				r			
	SB	r	M	Subtract M from r with borrow	r ← (r) – (M) – b	0	1	1	0	1	0	D_H		D_L				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) – (M) – b skip if borrow	0	1	1	0	1	1	D_H		D_L				r			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	D_H		D_L				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) – I skip if borrow	0	1	1	1	0	1	D_H		D_L				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	D_H		D_L				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b skip if borrow	0	1	1	1	1	1	D_H		D_L				I			
Comparison instructions	SEQ	r	M	Skip if r equal to M	(r) – M skip if zero	0	0	0	1	0	0	D_H		D_L				r			
	SEQI	M	I	Skip if M equal to I	(M) – I skip if zero	0	0	0	1	0	1	D_H		D_L				I			
	SNEI	M	I	Skip if M not equal to I	(M) – I skip if not zero	0	0	0	0	0	1	D_H		D_L				I			
	SGE	r	M	Skip if r is greater than or equal to M	(r) – M skip if not borrow	0	0	0	0	1	1	D_H		D_L				r			
	SGEI	M	I	Skip if M is greater than or equal to I	(M) – I skip if not borrow	0	0	0	1	1	1	D_H		D_L				I			
	SLEI	M	I	Skip if M is less than I	(M) – I skip if zero	0	0	0	0	1	1	D_H		D_L				I			

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
Logical operation instructions	AND	r	M	AND M with r	r ← (r) AND (M)	0 0 1 0	0 0	D_H	D_L r
	ANDI	M	I	AND I with M	M ← (M) AND I	0 0 1 0	0 1	D_H	D_L I
	OR	r	M	OR M with r	r ← (r) OR (M)	0 0 1 0	1 0	D_H	D_L r
	ORI	M	I	OR I with M	M ← (M) ORI	0 0 1 0	1 1	D_H	D_L I
	EXL	r	M	Exclusive OR M with r	r ← (r) XOR (M)	0 0 1 1	0 0	D_H	D_L r
	EXLI	M	I	Exclusive OR I with M	M ← (M) XOR I	0 0 1 1	0 1	D_H	D_L I
	SHR	r		Shift r right with carry	Carry → (r)	0 0 0 0	0 0	0 0	1 1 1 0 r
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 1 0 1	0 0	D_H	D_L r
	ST	M	r	Store r to M	M ← (r)	1 1 0 1	0 1	D_H	D_L r
	MVRD	r	M	Move M to destination M referring to r in the same row	$[D_H, rn]$ ← (M)	1 1 0 1	1 0	D_H	D_L r
	MVRS	M	r	Move source M referring to r to M in the same row	M ← $[D_H, rn]$	1 1 0 1	1 1	D_H	D_L r
	MVSR	M1	M2	Move M to M in the same row	$[D_H, D_L1]$ ← $[D_H, D_L2]$	1 1 1 0	0 0	D_H	D_L1 D_L2
	MVI	M	I	Move I to M	M ← I	1 1 1 0	0 1	D_H	D_L I
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1, then skip	1 1 1 1	0 0	D_H	D_L N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0, then skip	1 1 1 1	0 1	D_H	D_L N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0	ADDR (14 bits)		
	CAL	ADDR		Call subroutine	Stack ← (PC) + 1	1 1 0 0	ADDR (12 bits)		
	RT			Return from subroutine	PC ← Stack	0 0 0 0	0 0 0 0	1 0 0 0	
	RTS			Return from subroutine and skip	PC ← Stack + 1	0 0 0 0	0 0 0 0	1 0 1 0	
	RTB			Return from subroutine with bank data	PC ← Stack BANK ← Stack	1 1 1 1	1 1 1 1	1 1 0 0	
	RTBS			Return from subroutine with bank data and skip	PC ← Stack + 1 BANK ← Stack	1 1 1 1	1 1 1 1	1 1 0 1	
	RTI			Return from interrupt	PC ← Stack BANK ← Stack Carry ← Stack	0 0 0 0	0 0 0 0	1 0 0 1	
Status register instructions	SS	I	N	Set status register	(Status reg I) N ← 1	1 1 1 1	1 1 1 1	0 0 0	I N
	RS	I	N	Reset status register	(Status reg I) N ← 0	1 1 1 1	1 1 1 1	0 0 1	I N
	TST	I	N	Test status register true	if (Status reg I) N = all 1, then skip	1 1 1 1	1 1 1 1	0 1	I N
	TSF	I	N	Test status register false	if (Status reg I) N = all 0, then skip	1 1 1 1	1 1 1 1	1 0	I N

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
F/F test instructions	TUL	N		Test unlock F/F then skip if it has not been set	if unlock FF (N) = 0, then skip	0 0 0 0	0 0 0 0	1 1 0 1	N
Internal register transfer instructions	PLL	M	r	Load M to PLL registers	PLL reg ← PLL data	1 1 1 1	1 0 D_H	D_L	r
	INR	M	Rn	Input register/port data to M	M ← (Rn reg)	0 0 1 1	1 0 D_H	D_L	Rn
	OUTR	M	Rn	Output contents of M to register/port	Rn reg ← (M)	0 0 1 1	1 1 D_H	D_L	Rn
Hardware control instructions	SIO	I1	I2	Serial I/o control	SIO reg ← I1, I2	0 0 0 0	0 0 0 1	I1	I2
	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0	0 0 0 0	0 0 0 1	I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0	0 0 0 0	0 0 1 0	I
	BEEP	I		Beep control	Beep reg ← I	0 0 0 0	0 0 0 0	0 1 1 0	I
	DZC	I		Data zone control	DZC reg ← I	0 0 0 0	0 0 0 0	1 0 1 1	I
	TMS	N		Set timer register	Timer reg ← I	0 0 0 0	0 0 0 0	1 1 0 0	N
	IOS	PWn	N	Set port control word	IOS reg PWn ← N	1 1 1 1	1 1 1 0	PWn	N
I/O instructions	IN	M	Pn	Input port data to M	M ← (Pn)	1 1 1 0	1 0 D_H	D_L	Pn
	OUT	M	Pn	Output contents of M to port	Pn ← M	1 1 1 0	1 1 D_H	D_L	Pn
	SPB	Pn	N	Set port bits	(Pn) N ← 1	0 0 0 0	0 0 1 0	Pn	N
	RPB	Pn	N	Reset port bits	(Pn) N ← 0	0 0 0 0	0 0 1 1	Pn	N
	TPT	Pn	N	Test port bits, then skip if all bits specified are true	if (Pn) N = all 1, then skip	1 1 1 1	1 1 0 0	Pn	N
	TPF	Pn	N	Test port bits, then skip if all bits specified are false	if (Pn)) N = all 0, then skip	1 1 1 1	1 1 0 1	Pn	N
Bank switching instructions	BANK	I		Select bank	BANK ← I	0 0 0 0	0 0 0 0	0 1 1 1	I
Other instruc-tions	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0 0 0 0	0 0 0 0	0 1 0 0	I
	CKSTP			Clock stop	Stop Xtal OSC if HOLD = 0	0 0 0 0	0 0 0 0	0 1 0 1	
	NOP			No operation	No operation	0 0 0 0	0 0 0 0	0 0 0 0	