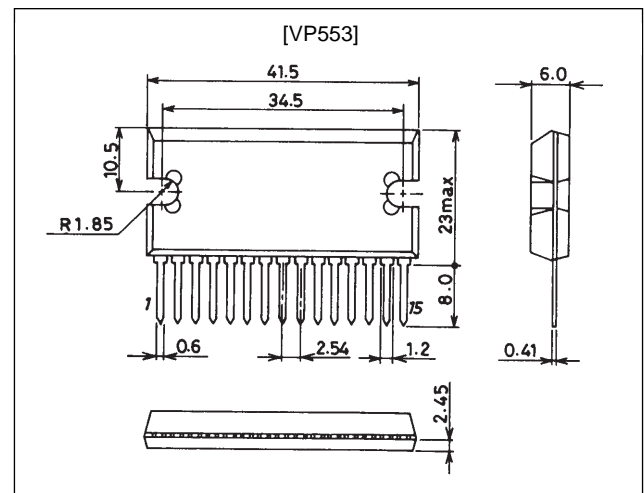


**VP553****CRT Display Video Output Amplifier****Features**

- Active load circuits
- Wide bandwidth and high output voltage. Optimal for use in f_H (horizontal deflection frequency) = 90 kHz class ultrahigh precision monitors.
- Single 15-pin SIP molded package houses three channels.

Package Dimensionsunit: mm
2127A**Specifications****Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		90	V
Allowable power dissipation	P_d max	With an ideal heat sink at $T_a = 25^\circ\text{C}$	25	W
Maximum junction temperature	T_j max		150	$^\circ\text{C}$
Maximum case temperature	T_c max		100	$^\circ\text{C}$
Storage temperature	T_{stg}		-20 to +110	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		80	V

Electrical Characteristics at $T_a = 25^\circ\text{C}$ (For a single channel, with $R_{in} = 680\ \Omega$, $R_{ip} = 22\ \Omega$, $C_{ip} = 56\ \text{pF}$)

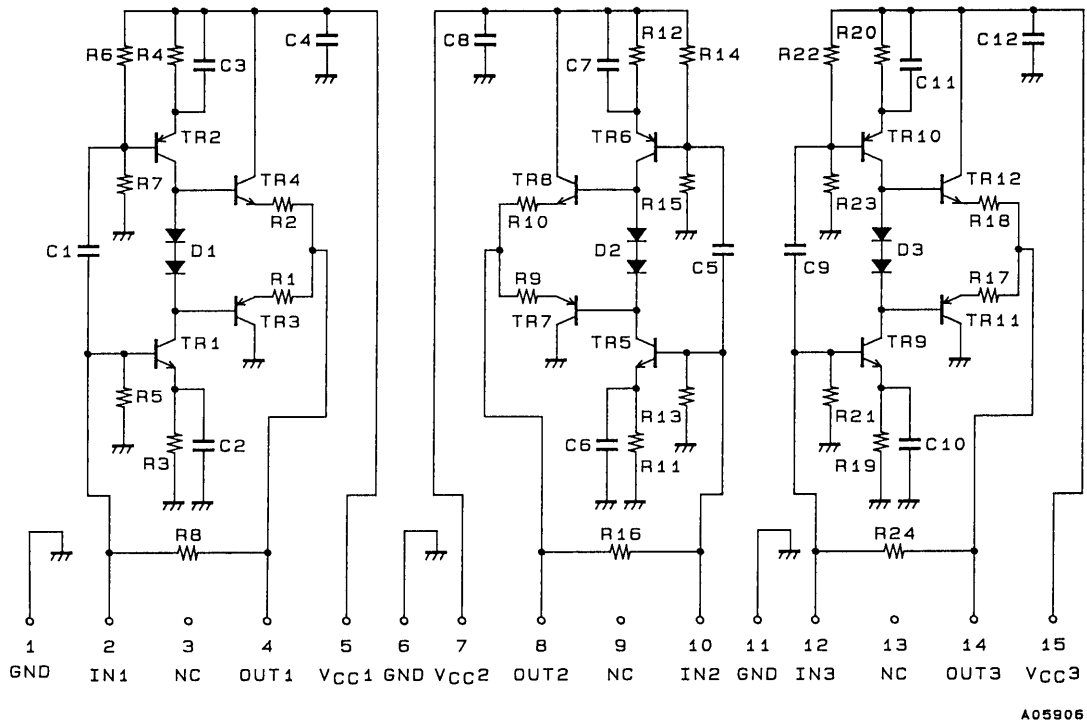
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock frequency bandwidth (-3 dB)	f (clock)	$V_{CC} = 80\ \text{V}$, $C_L = 10\ \text{pF}$		160		MHz
Frequency bandwidth (-3 dB)	f_c	V_{IN} (DC) = 2.0 V, V_{OUT} (p-p) = 40 V		80		MHz
Pulse response	t_r	$V_{CC} = 80\ \text{V}$, $C_L = 10\ \text{pF}$		4.8		ns
	t_f	V_{IN} (DC) = 2.0 V, V_{OUT} (p-p) = 40 V		4.5		ns
Voltage gain	VG (DC)		13	15	17	Double
Current drain	$I_{CC}(1)$	$V_{CC} = 80\ \text{V}$, V_{IN} (DC) = 2.0 V, $f = 10\ \text{MHz}$ clock, $C_L = 10\ \text{pF}$, V_{OUT} (p-p) = 40 V		32		mA
	$I_{CC}(2)$	$V_{CC} = 80\ \text{V}$, V_{IN} (DC) = 2.0 V, $f = 100\ \text{MHz}$ clock, $C_L = 10\ \text{pF}$, V_{OUT} (p-p) = 40 V		75		mA

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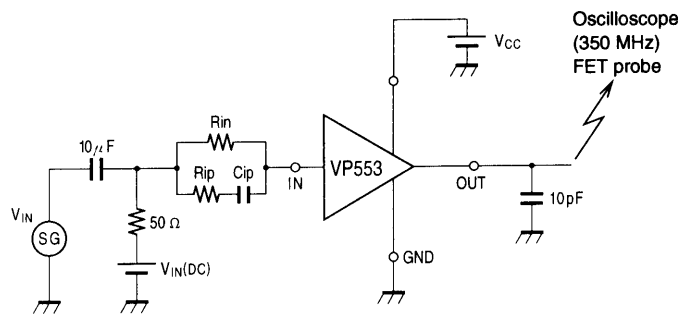
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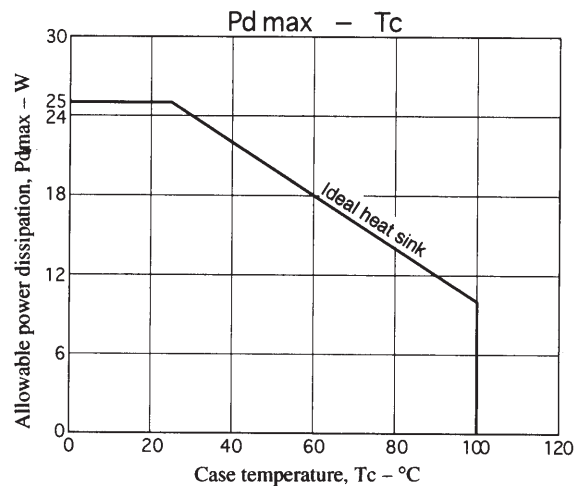
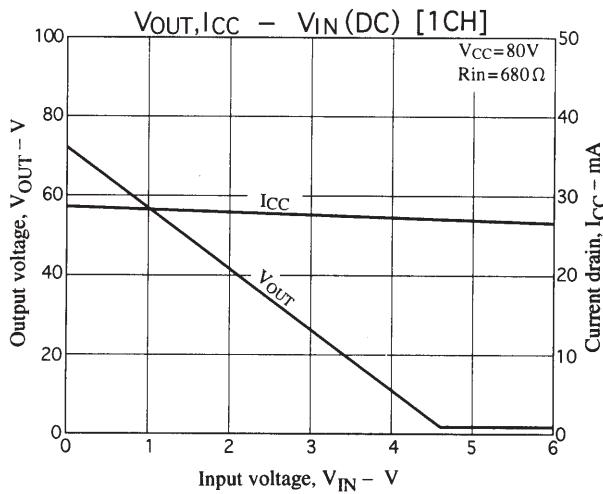
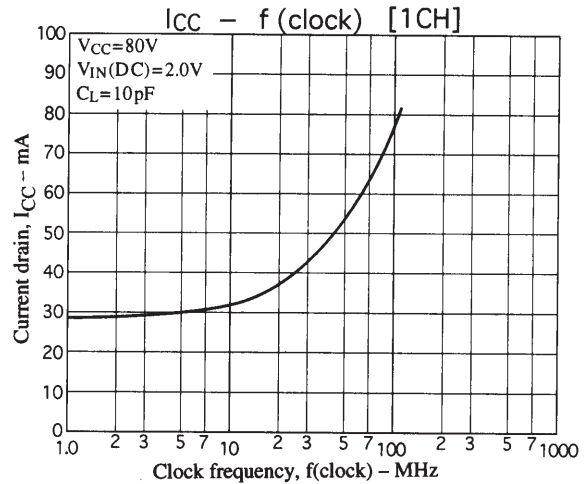
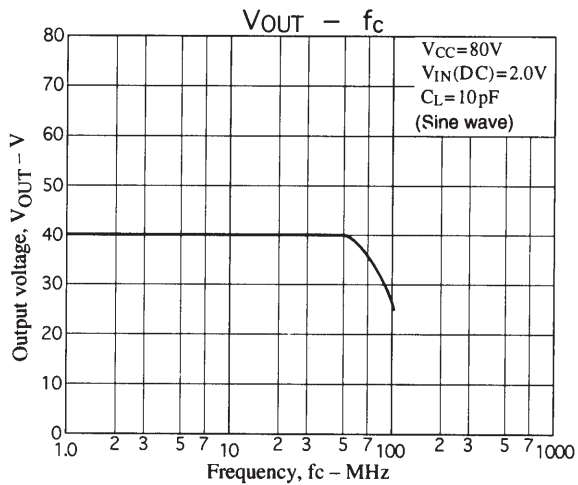
VP553

Internal Equivalent Circuit



Test Circuit (for a single channel)





Thermal Design

Thermal design requires that the two conditions $T_j(\text{max}) \leq 150^\circ\text{C}$ and $T_c \leq 100^\circ\text{C}$ be met.

(a) Concerning $T_j(\text{max})$, the chip temperature T_j for each transistor is given by equation (1).

$$T_j = (T_{ri}) = \theta_{j-c} (T_{ri}) \times P_C (T_{ri}) + \Delta T_c + T_a \text{ (}^\circ\text{C)} \dots\dots\dots(1)$$

$\theta_{j-c} (T_{ri})$: The thermal resistance of each transistor chip itself

$P_C (T_{ri})$: The collector loss for each transistor

ΔT_c : Increase in the case temperature

T_a : Ambient temperature

$\theta_{j-c} (T_{ri})$ for each chip will be:

$$\theta_{j-c} (T_{r1}) \text{ to } (T_{r4}) = 35^\circ\text{C/W} \dots\dots\dots(2)$$

The loss in transistors in a video pack varies with frequency. The loss increases with the frequency.

For example, if the maximum frequency will be 100 MHz (clock), then the transistors with the largest losses will be transistors 3 and 4 in the emitter-follower (EF) stage. From the $P_d - f(\text{clock})$ figure, we see that that loss will be 25% of the total for a single channel. That is:

$$P_C (\text{EF stage})_{f=100 \text{ MHz}} = P_d (1\text{ch})_{f=100 \text{ MHz}} \times 0.25 \text{ [W]} \dots\dots\dots(3)$$

The thermal design must assure that T_j does not exceed 150°C at this time.

(b) Concerning $T_c(\text{max})$, the relationship between θ_h and ΔT_c is:

$$\Delta T_c = P_d (\text{total}) \times \theta_h \dots\dots\dots(4)$$

Taking the increase due to T_a into account, the condition the thermal design must meet becomes $T_c = \Delta T_c + T_a \leq 100^\circ\text{C}$.

Next we design thermal conditions for the VP553 that meet the conditions in sections (a) and (b) above.

Sample Thermal Design for the VP553

Conditions: For an $f_H = 90$ kHz class monitor, $f_V = 100$ MHz (clock).

$V_{CC} = 80$ V, $V_{OUT} = 40$ Vp-p ($C_L = 10$ pF)

Here we consider the case where such a monitor is to be operated at ambient temperatures up to $T_a = 60^\circ\text{C}$ and at a maximum frequency of $f = 100$ MHz (clock).

As mentioned previously, the chips with the maximum loss will be transistors 3 and 4 in the emitter-follower stage. Equation (5) follows from deriving that value from the figure below and equation (3).

$$P_C(\text{Tr}3, 4)_{f=100\text{ MHz}} = 6.2 \times 0.25 \approx 1.55 \text{ [W]} \dots\dots\dots(5)$$

However, the actual usage conditions include a blanking period. If we calculate the power during this period approximately at a 1-MHz power ratio, from $P_d - f$ (clock) and $P_C(\text{Tri})\text{Ratio} - f$ (clock) figures, we see that $P_C(\text{BLK})$ for transistors 3 and 4 will be:

$$P_C \text{ BLK}(\text{Tr}3, 4) = 2.2 \times 0.08 = 0.18 \text{ [W]} \dots\dots\dots(6)$$

If the blanking period is 20% of the total, from the data of equation (5) and formula (6) we see that the loss in transistors 3 and 4 will be:

$$P_C(\text{Tr}3, 4) = P_C(\text{Tr}3, 4)_{f=100\text{ MHz}} \times 0.8 + P_C \text{ BLK}(\text{Tr}3, 4) \times 0.2 \approx 1.28 \text{ [W]} \dots(7)$$

Next, applying the value of θ_{j-c} to equation (7), shows ΔT_j to be:

$$\Delta T_j = 1.28 \times 35 \approx 45 \text{ [}^\circ\text{C]}$$

Since $\Delta T_j \leq 50^\circ\text{C}$, it suffices to only consider the $T_c \leq 100^\circ\text{C}$ condition in the thermal design. That is, in the thermal design we design θ_h so that T_c will be under 100°C when $P_d(\text{total}) = P_d(1\text{ch}) \times 3$ for the time when all three channels are operating at their maximum levels.

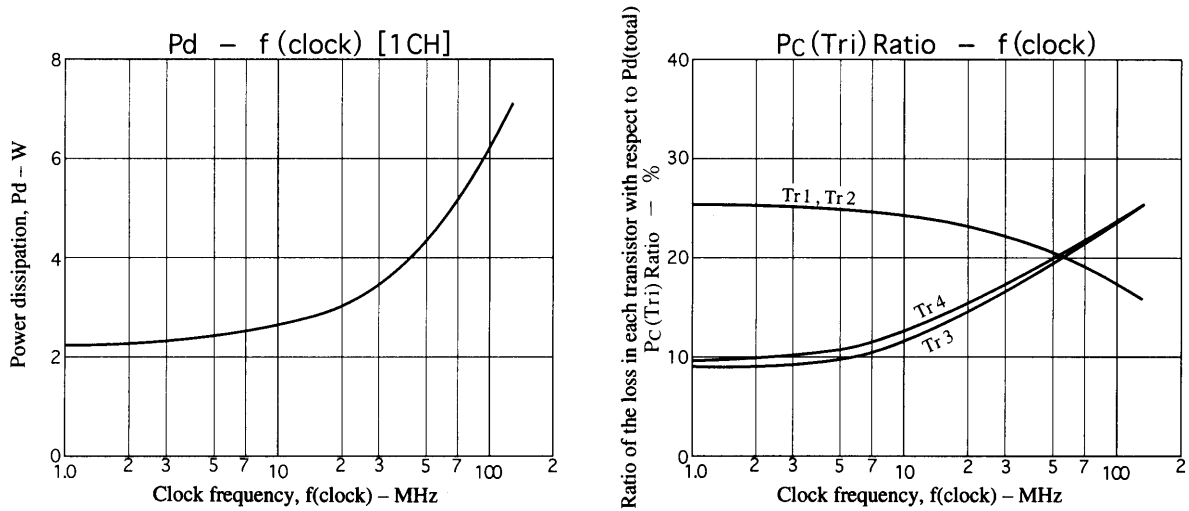
$$\Delta T_c \text{ will be: } \Delta T_c = 100 - 60 = 40^\circ\text{C}$$

$$\theta_h = \Delta T_c \div P_d(\text{total}) = 40 \div \{(6.2 \times 0.8 + 2.2 \times 0.2) \times 3\} = 2.5$$

Thus:

$$\theta_h = 2.5^\circ\text{C/W}$$

In actual use, due to the actual ambient temperature, the operating conditions, and other factors, it will be possible to use a heat sink smaller than the one required by the above design. Users should design an optimal heat sink using the data presented above and their actual conditions.



V_{CC} (V)	V_{OUT} (V)	V_O (center)
80	40	40

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