

# High Efficiency PMIC with Dynamic Voltage Management

## General Description

The uP6636Q includes 4 synchronous-rectified buck converters and 9 linear regulators. With internal low RDS(ON) switches, the buck converter is capable of delivering 1.5A or 2.8A output current over a wide input voltage range from 2.7V to 5.3V. Fixed 2.25MHz PWM operation allows possible smallest output ripple and external component size. Dynamic Voltage Scaling (DVS) is supported either by dedicated control pins, or through I2C interface to optimize the system performance for the processor. Other features include internal soft-start, over-temperature, and over-current protections.

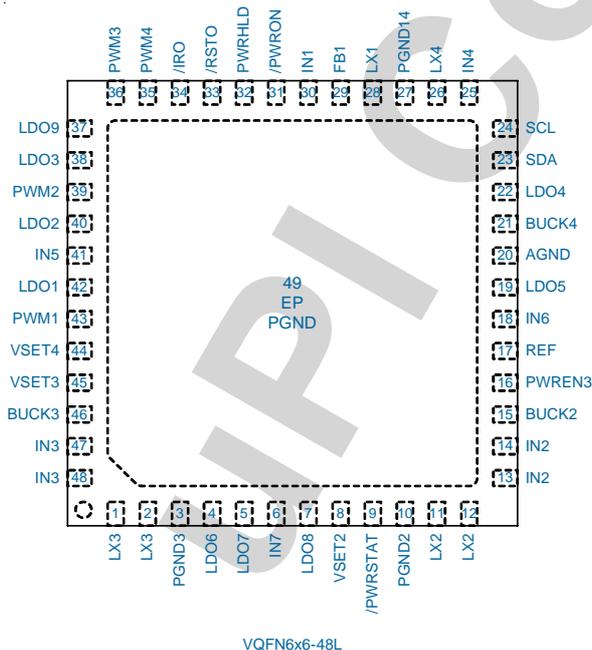
The power sequence and reset controller provides power-on reset, software initiated reset, and power cycle reset for the processor. It also features the watchdog supervisory function. Multiple sleep modes with autonomous sleep and wake-up sequence control are supported.

The uP6636Q is available in a space-saving, VQFN6x6-48L package.

## Applications

- Tablet
- Phone
- MID
- PND

## Pin Configuration



## Features

- 4 Synchronous Step-Down Converters
  - Buck\_1 for VDD\_DDR: 1.2V/1.5A
  - Buck\_2 for VDD\_LOG: 1.0V/2.8A
  - Buck\_3 for VDD\_ARM: 1.0V/2.8A
  - Buck\_4 for VCC\_IO: 3.3V/1.5A
- 5 Low-Noise Linear Regulators
  - LDO1 for VDD\_10: 1.0V/150mA
  - LDO2 for VDD\_12: 1.2V/150mA
  - LDO3 for VCC18\_CIF: 1.8V/350mA
  - LDO4 for VCCA\_33: 3.3V/350mA
  - LDO5 for VCC\_TP: 3.3V/350mA
- 3 Low Input Linear Regulators
  - LDO6 for VCCIO\_WL: 3.3V/150mA
  - LDO7 for VCC\_18: 1.8V/350mA
  - LDO8 for VCC28\_CIF: 2.8V/350mA
- 1 Low Quiescent Linear Regulator
  - LDO9 for RTC: 1.8V/50mA
- 2.7V to 5.3V Input Range
- I<sup>2</sup>C Interface
- BUCK2, BUCK3, and BUCK4 Default Voltage with I/O Select
- Build-In Fault Interrupt Controller
- Power Sequencing and Reset Controller
  - Power ON/OFF
  - Power ON Reset
  - Soft/Hard Ware Reset
  - Watchdog Supervision
  - Multiple Sleep Modes
- Space-Saving VQFN6x6-48L Package
- RoHS Compliant and Halogen Free

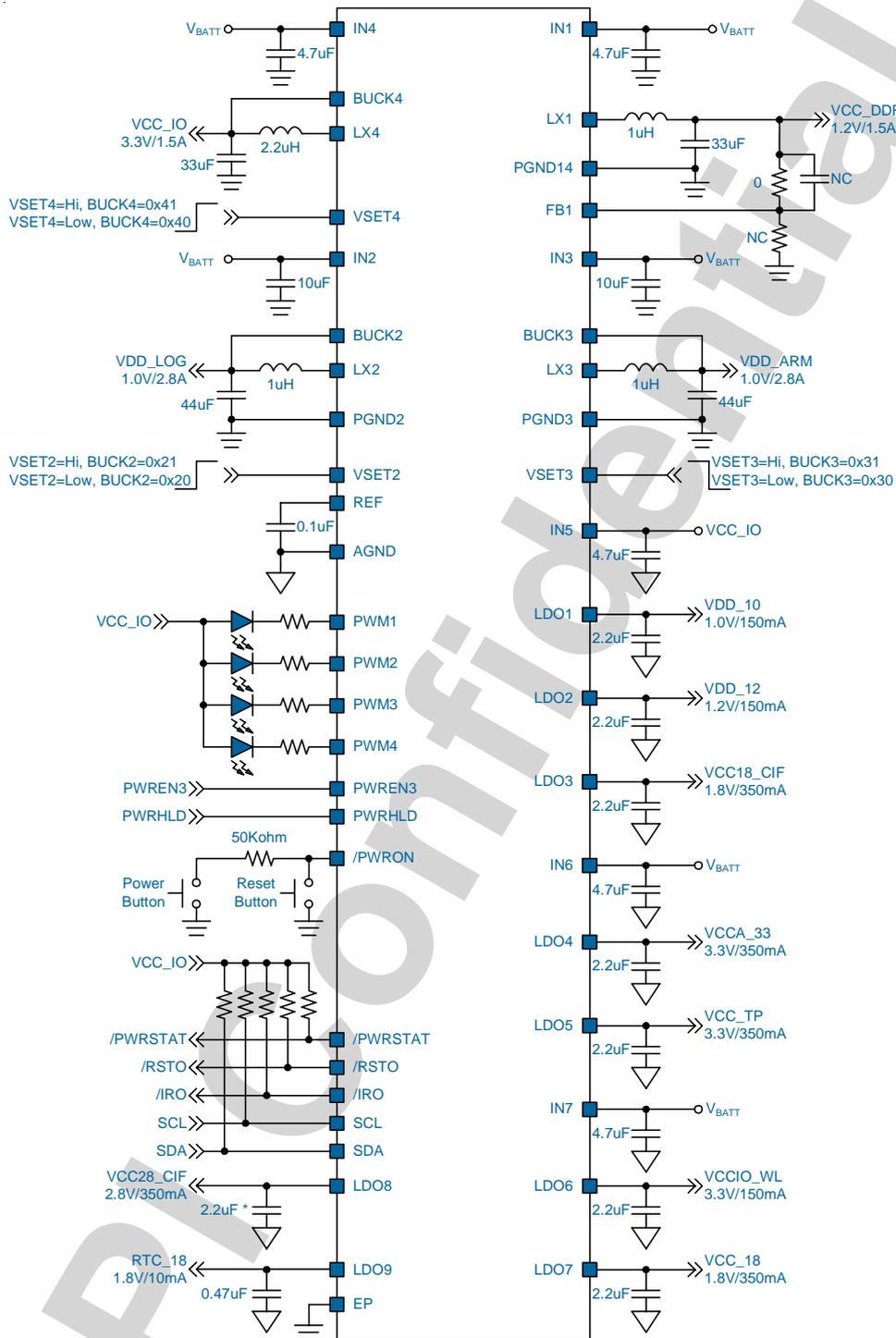
## Ordering Information

Order Number	Package Type	Top Marking
uP6636QQGK	VQFN6x6-48L	uP6636Q

Note:

- (1) Please check the sample/production availability with uPI representatives.
- (2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit



\* When power is used in sensor such as camera, in order to obtain a better PSRR and output noise, it is recommended output capacitor 22uF.

**Functional Pin Description**

No.	Pin Name	Pin Function
1, 2	LX3	Switches Output for BUCK3. Connect this pin to the output inductor.
3	PGND3	<b>Power Ground for BUCK3.</b> Connect the input and output capacitor GND for BUCK3 to this pin directly.
4	LDO6	<b>LDO6 Output Voltage.</b> This pin is LDO6 power output of the device. A minimum 2.2uF output capacitor is required.
5	LDO7	<b>LDO7 Output Voltage.</b> This pin is LDO7 power output of the device. A minimum 2.2uF output capacitor is required.
6	IN7	<b>Supply Input for LDO6, LDO7, and LDO8.</b> A minimum 4.7uF ceramic capacitor is required for locally bypassing the supply voltage.
7	LDO8	<b>LDO8 Output Voltage.</b> This pin is LDO8 power output of the device. A minimum 2.2uF output capacitor is required.
8	VSET2	<b>Output Voltage Selection for BUCK2.</b> This pin can select the BUCK2 default output voltage (0x20 or 0x21).
9	/PWRSTAT	<b>Active-Low Open-Drain Power-Button Status Output.</b> /PWRSTAT is active low whenever the /PWRON is pushed, and is high-Z otherwise.
10	PGND2	<b>Power Ground for BUCK2.</b> Connect the input and output capacitor GND for BUCK2 to this pin directly.
11, 12	LX2	<b>Switches Output for BUCK2.</b> Connect this pin to the output inductor.
13, 14	IN2	<b>Supply Input for BUCK2 Converter.</b> A minimum 10uF ceramic capacitor is required for locally bypassing the supply voltage. Place the bypassing capacitor physically near this pin and connect it to the PGND2 pin with wide and short trace.
15	BUCK2	<b>BUCK2 Output Feedback Voltage.</b> A minimum 44uF output capacitor is required.
16	PWREN3	<b>Power Enable Input for BUCK3.</b> PWREN3 is functional only when PWRHLD is driven high. Drive PWREN to a logic high to turn on the BUCK3. Drive PWREN to a logic low to turn off the BUCK3.
17	REF	<b>Reference Voltage.</b> Connect a 0.1uF capacitor from this pin to AGND for bypassing the internal reference voltage.
18	IN6	<b>Supply Input for LDO4 and LDO5.</b> A minimum 4.7uF ceramic capacitor is required for locally bypassing the supply voltage.
19	LDO5	<b>LDO5 Output Voltage.</b> This pin is LDO5 power output of the device. A minimum 2.2uF output capacitor is required.
20	AGND	<b>Analog Ground.</b> Connect the REF bypass capacitor to this pin directly.
21	BUCK4	<b>BUCK4 Output Feedback Voltage.</b> A minimum 33uF output capacitor is required.
22	LDO4	<b>LDO4 Output Voltage.</b> This pin is LDO4 power output of the device. A minimum 2.2uF output capacitor is required.
23	SDA	<b>Data Input/Output for Serial Interface.</b> An external pull-up resistor is needed.
24	SCL	<b>Clock Input for Serial Interface.</b> An external pull-up resistor is needed.

**Functional Pin Description**

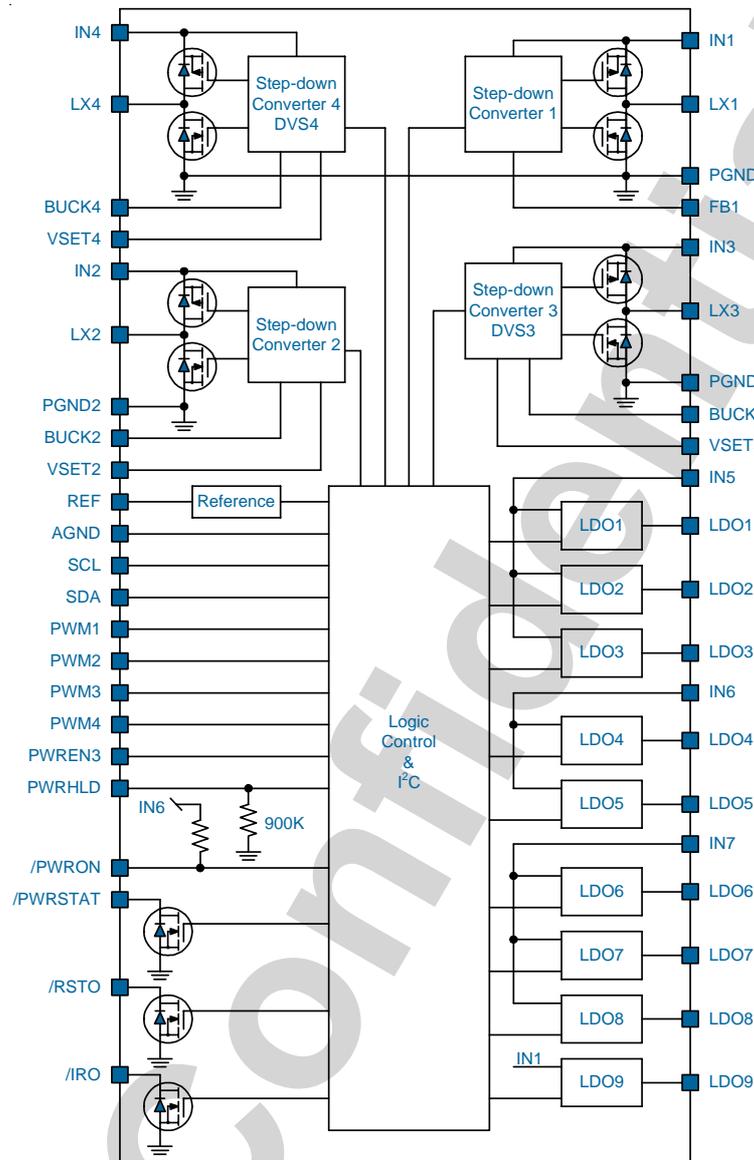
No.	Pin Name	Pin Function
25	IN4	<b>Supply Input for BUCK4 Converter.</b> A minimum 4.7uF ceramic capacitor is required for locally bypassing the supply voltage. Place the bypassing capacitor physically near this pin and connect it to the PGND14 pin with wide and short trace.
26	LX4	<b>Switches Output for BUCK4.</b> Connect this pin to the output inductor.
27	PGND14	<b>Power Ground for BUCK1 and BUCK4.</b> Connect the input and output capacitor GND for BUCK1 and BUCK4 to this pin directly.
28	LX1	<b>Switches Output for BUCK1.</b> Connect this pin to the output inductor.
29	FB1	<b>BUCK1 Output Feedback Voltage.</b> For the adjustable output voltage options, connect this pin to the output feedback resistor divider for voltage setting. For the fixed output voltage options, connect this pin to the output directly to regulate the output voltage. A minimum 33uF output capacitor is required.
30	IN1	<b>Supply Input for BUCK1 Converter.</b> A minimum 4.7uF ceramic capacitor is required for locally bypassing the supply voltage. Place the bypassing capacitor physically near this pin and connect it to the PGND14 pin with wide and short trace.
31	/PWRON	<b>Power ON/OFF Controller Input.</b> /PWRON is a unique, multi-function input. Drive /PWRON to GND through a 50kΩ resistor to enable the IC, drive /PWRON directly to GND to assert a Manual-Reset condition.
32	PWRHLD	<b>Power Hold Input.</b> Power Enable input for BUCK1, BUCK2, BUCK3, BUCK4, LDO1, and LDO7. PWRHLD is internally pulled down to GND through a 900kΩ resistor.
33	/RSTO	<b>Open-Drain Reset Output.</b> /RSTO is active low upon startup or when manual reset is to occur via the /PWRON input. When active on startup, /RSTO remains low until reset time-out period expires. When manual-reset is active, /RSTO immediately active low, then remains active low until the /PWRON input is non-active and the reset time-out period expires.
34	/IRO	<b>Open-Drain Interrupt Output.</b> /IRO is an active low when interrupt is generated.
35	PWM4	<b>General Purpose PWM I/O.</b> Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Drive section for more information.
36	PWM3	<b>General Purpose PWM I/O.</b> Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Drive section for more information.
37	LDO9	<b>LDO9 Output Voltage.</b> This pin is LDO9 power output of the device. A minimum 0.47uF output capacitor is required.
38	LDO3	<b>LDO3 Output Voltage.</b> This pin is LDO3 power output of the device. A minimum 2.2uF output capacitor is required.
39	PWM2	<b>General Purpose PWM I/O.</b> Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Drive section for more information.
40	LDO2	<b>LDO2 Output Voltage.</b> This pin is LDO2 power output of the device. A minimum 2.2uF output capacitor is required.
41	IN5	<b>Supply Input for LDO1, LDO2, and LDO3.</b> A minimum 4.7uF ceramic capacitor is required for locally bypassing the supply voltage.
42	LDO1	<b>LDO1 Output Voltage.</b> This pin is LDO1 power output of the device. A minimum 2.2uF output capacitor is required.

*Functional Pin Description*

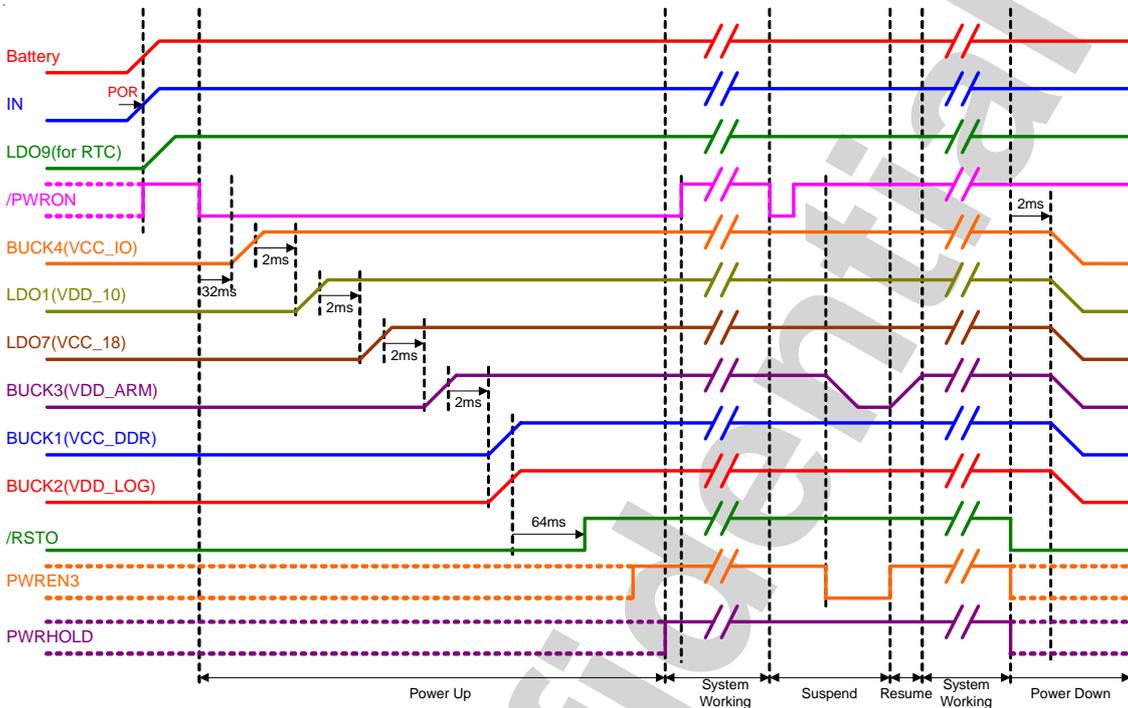
No.	Pin Name	Pin Function
43	PWM1	<b>General Purpose PWM I/O.</b> Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Drive section for more information.
44	VSET4	<b>Output Voltage Selection for BUCK4.</b> This pin can select the BUCK4 default output voltage (0x40 or 0x41).
45	VSET3	<b>Output Voltage Selection for BUCK3.</b> This pin can select the BUCK3 default output voltage (0x30 or 0x31).
46	BUCK3	<b>BUCK3 Output Feedback Voltage.</b> A minimum 44uF output capacitor is required.
47, 48	IN3	<b>Supply Input for BUCK3 Converter.</b> A minimum 10uF ceramic capacitor is required for locally bypassing the supply voltage. Place the bypassing capacitor physically near this pin and connect it to the PGND3 pin with wide and short trace.
49	Exposed Pad (PGND)	<b>Power Ground for All Regulators.</b> Connect the input and output capacitor for all regulators to this pin directly. The exposed pad should be well soldered to PCB with multiple via to ground plane for optimal thermal performance.

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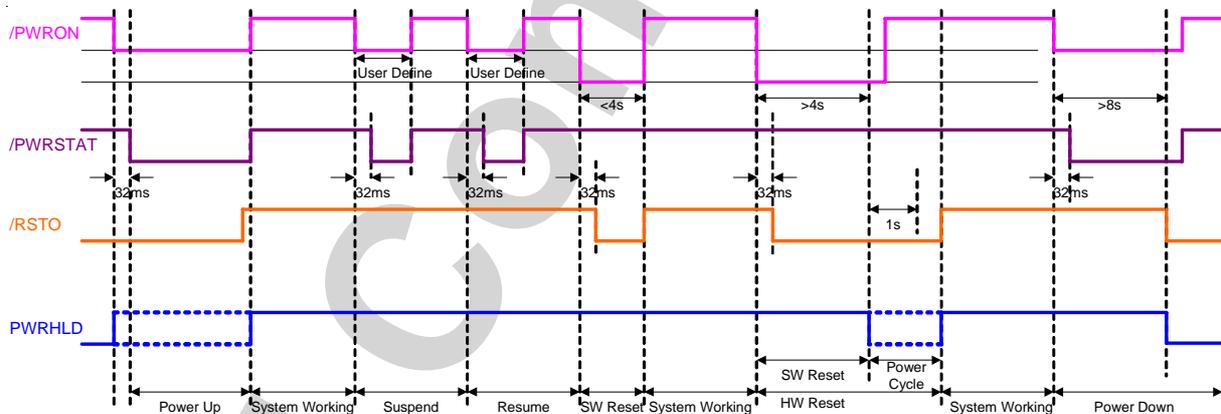
**Functional Block Diagram**



**Power ON/OFF Control Sequence**



**/PWRON, /PWRSTAT, /RSTO and PWRHLD**



**Triggering uP6636Q Power on Sequence**

Any term of the following descriptions will trigger the uP6636Q to transition from off condition to power on sequence condition:

- /PWRON goes to middle level.
- PWRHLD goes to high level.
- When /PWRON is middle level or PWRHLD is high level, and then OFFSYS is set to 0.

**Triggering uP6636Q Power off Sequence**

Any term of the following descriptions will trigger the uP6636Q to transition from working condition to power off sequence condition:

- /PWRON goes to high level and PWRHLD goes to low level.
- When /PWRON is middle level or PWRHLD is high level, and then OFFSYS is set to 1.
- When PWRHLD is high level and /PWRON is pulled down to middle level for over 8s.

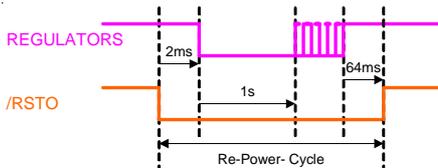
**Normal Mode Operation**

- When /PWRON is middle level or PWRHLD is high level.

**Triggering uP6636Q Rebooting Power cycle sequence (Hardware Reset)**

Any term of the following descriptions will trigger the uP6636Q to transition from working condition to reboot power cycle sequence condition and any term of them will cause PCSTAT[] from 0 to 1 (read clear):

- SIPC is set to 1.
- When PWRHLD is high level and /PWRON is pulled down to low level for over 4s.
- When PWRHLD is high level and PWREN3 is high level and WDPCEN[] is set to 1.



**Triggering uP6636Q Software Reset**

Any term of the following descriptions will trigger the uP6636Q to transition from working condition to software reset condition:

- PWRHLD is high level and /PWRON is pulled down to low level for less than 4s.
- When PWRHLD is high level and PWREN3 is high level and WDSREN[] is set to 1.

**Buck3 Control**

Any term of the following descriptions will trigger the uP6636P to transition from working condition to ON/OFF Buck3 condition:

- Regardless of throw-in sequence, as long as PWRHLD is high level and /PWRON is middle level, Buck3 can only be controlled by PWREN3.
- When /PWRON is middle level, Buck3 can only be controlled by EN[7](32h) control.
- When PWRHLD is high level, Buck3 can only be controlled by PWREN3 control.

**The transition of /RSTO**

Any term of the following descriptions will trigger the transition of /RSTO.

- When Buck4 is falling and lower than VBUCKPG, then /RSTO goes to low after 1ms (Typ.) /RSTO fault delay time.
- Power on.
- Power off.
- Hardware Reset.
- Software Reset.

**Registers Reset**

- When power on reset of IN6 is detected, to reset all registers.
- When power on sequence, power off sequence, software reset, hardware reset, to reset regulators registers.

**/PWRON Delay Time**

- /PWRON delay time is 500ms (Typ.) only when power on reset of IN6 is detected, otherwise, /PWRON delay time is 32ms (Typ.).

**Interrupt Address Indicator Operation**

- If two interrupt events occur, then interrupt address indicator points to the register address which occurs firstly, and when one is read, then interrupt address indicator points to another.
- If all interrupt register addresses are read, interrupt address indicator is set to 0xFF, and /IRO goes to high level.

**All Registers Software Control Condition**

- Regardless of throw-in sequence, as long as PWRHLD is high level and /PWRON is middle level, all the registers can be controlled by software except EN[7](32h).
- When /PWRON is middle level, all registers can be controlled by software without exception.
- When PWRHLD is high level, all the registers can be controlled by software except EN[7](32h).

**Functional Description**
**uP6636Q With Rockchip RK31x8 Power Domains**

uP6636Q	RK31x8	Default Voltage	Max. Current	Power ON Sequence	Sleep Mode State
BUCK1	VCC_DDR	Adjustable	1.5A	5	ON
BUCK2	VDD_LOG	1.0V	2.8A	5	ON
BUCK3	VDD_ARM	1.0V	2.8A	4	OFF
BUCK4	VCC_IO	3.3V	1.5A	1	ON
LDO1	VDD_10	1.0V	150mA	2	ON
LDO2	VDD_12	1.2V	150mA	--	OFF
LDO3	VCC18_CIF	1.8V	350mA	--	OFF
LDO4	VCCA_33	3.3V	350mA	--	OFF
LDO5	VCC_TP	3.3V	350mA	--	OFF
LDO6	VCCIO_WL	3.3V	150mA	--	OFF
LDO7	VCC_18	1.8V	350mA	3	ON
LDO8	VCC28_CIF	2.8V	350mA	--	OFF
LDO9	RTC_18	1.8V	50mA	0	Always ON

**I2C Read and Write Protocol**

Write to a Single Register

S	Slave_addr+W [A7 : A0]	AS	Reg_addr(index) [I7 : I0]	AS	Reg_data [D7 : D0]	AS	P
---	---------------------------	----	------------------------------	----	-----------------------	----	---

Read from a Single Register

S	Slave_addr+W [A7 : A0]	AS	Reg_addr(index) [I7 : I0]	AS	RS	Slave_addr + R [A7 : A0]	AS	Reg_data [D7 : D0]	NA	P
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S = Start

P = Stop

AS = ACK from slave

AM = ACK from master

NA = No ACK

RS = Repeat Start

**Functional Description**

The uP6636Q PMU acts a Slave Transmitter/Receiver.

The Address of the uP6636Q PMU for WRITE is B4H.

The Address of the uP6636Q PMU for READ is B5H.

PMU I<sup>2</sup>C Register Map

**(Note: Please do not write “Reserve” Register.)**

--	Index	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYS	00h	BATLEVMSK	BATSTAT	VBATDAT		BATLEV			
	01h	TMSK	TSTAT	--	--	--	--	--	--
	02h	Reserve							
	03h	Reserve							
	04h	Reserve							
BUCK1	10h	--	--	VSET					
	11h	Reserve							
	12h	EN	--	--	--	--	--	FLTMSK	PG
BUCK2	20h	--	--	VSETL					
	21h	--	--	VSETH					
	22h	EN	--	--	--	--	--	FLTMSK	PG
	23h	Reserve							
BUCK3	30h	--	--	VSETL					
	31h	--	--	VSETH					
	32h	EN	--	--	--	--	--	FLTMSK	PG
	33h	Reserve							
BUCK4	40h	--	--	VSETL					
	41h	--	--	VSETH					
	42h	EN	--	--	--	--	--	FLTMSK	PG
	43h	Reserve							
LDO1	50h	--	--	VSET					
	51h	EN	--	--	--	--	DIS	FLTMSK	PG
LDO2	58h	--	--	VSET					
	59h	EN	--	--	--	--	DIS	FLTMSK	PG
LDO3	60h	--	--	VSET					
	61h	EN	--	--	--	--	DIS	FLTMSK	PG
LDO4	68h	--	--	VSET					
	69h	EN	--	--	--	--	DIS	FLTMSK	PG
LDO5	70h	--	--	VSET					
	71h	EN	--	--	--	--	DIS	FLTMSK	PG
LDO6	80h	--	--	VSET					
	81h	EN	--	--	--	--	DIS	FLTMSK	PG

**Functional Description**

 PMU I<sup>2</sup>C Register Map (cont.)

--	Index	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDO7	90h	--	--	VSET					
	91h	EN	--	--	--	--	DIS	FLTMSK	PG
LDO8	A0h	--	--	VSET					
	A1h	EN	--	--	--	--	DIS	FLTMSK	PG
LDO9	B1h	EN	--	--	--	--	--	--	--
PB	C0h	PBAMSK	PBDMSK	--	--	--	--	WDSREN	WDPCEN
	C1h	INTADR							
	C2h	PBASTAT	PBDSTAT	PBDAT	--	--	--	--	--
	C3h	--	--	--	OFFSYS	OFFSYSCLR	--	--	SIPC
	C5h	--	--	--	--	--	--	PCSTAT	SRSTAT
PWM4	E3h	EN	FREQ			DUTY			
PWM3	E4h	EN	FREQ			DUTY			
PWM1	F4h	EN	FREQ			DUTY			
PWM2	F5h	EN	FREQ			DUTY			

**Serial Codes for Battery Voltage Monitor Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	04	BATLEVMSK	BATSTAT	VBATDAT	--	BATLEV			
		R/W	R	R	--	R/W			
Name	Default	Description							
BATLEVMSK	0	Battery Voltage Level Interrupt ON/OFF. 0= Disable the Battery Voltage Level interrupt. (Default) 1= Enable the Battery Voltage Level Interrupt.							
BATSTAT	R	Battery Voltage Interrupt Status. This bit is automatically cleared to 0 after read. 0= BATLEV interrupt is normal. 1=BATLEV interrupt is generated.							
VBATDAT	R	Battery Voltage Monitor real time status. Value is 1 when VBAT < BATLEV, value is 0 otherwise. 0= IN6 voltage is normal. 1=IN6 voltage is below BATLEV threshold.							
BATLEV	2.9V	Battery Voltage Detect Threshold. 0000=2.5V 0001=2.6V 0010=2.7V 0011=2.8V 0100=2.9V (Default) 0101=3.0V 0110=3.1V 0111=3.2V				1000=3.3V 1001=3.4V 1010=3.5V 1011=3.6V 1100=3.7V 1101=3.8V 1110=3.9V 1111=4.0V			

**Serial Codes for Thermal Monitor Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01	00	TMSK	TSTAT	--	--	--	--	--	--
		R/W	R	--	--	--	--	--	--
Name	Default	Description							
TMSK	0	Thermal Interrupt ON/OFF. 0= Disable the interrupt. (Default) 1= Enable the Thermal Monitor.							
TSTAT	R	Thermal Interrupt Status. This bit is automatically cleared to 0 after read. 0= Thermal interrupt is normal. 1=Thermal interrupt is generated.							

**Serial Codes for BUCK1 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10	18	--	--	VSET					
		--	--	R/W					
Name	Default	Description							
VSET	1.2V	BUCK1 Output Voltage Selection			010110=0.600V		101011=1.200V		
		000000=0.600V			010111=0.600V		101100=1.200V		
		000001=0.600V			011000=1.200V (Default)		101101=1.200V		
		000010=0.600V			011001=1.200V		101110=1.200V		
		000011=0.600V			011010=1.200V		101111=1.200V		
		000100=0.600V			011011=1.200V		110000=1.200V		
		000101=0.600V			011100=1.200V		110001=1.200V		
		000110=0.600V			011101=1.200V		110010=1.200V		
		000111=0.600V			011110=1.200V		110011=1.200V		
		001000=0.600V			011111=1.200V		110100=1.200V		
		001001=0.600V			100000=1.200V		110101=1.200V		
		001010=0.600V			100001=1.200V		110110=1.200V		
		001011=0.600V			100010=1.200V		110111=1.200V		
		001100=0.600V			100011=1.200V		111000=1.200V		
		001101=0.600V			100100=1.200V		111001=1.200V		
		001110=0.600V			100101=1.200V		111010=1.200V		
		001111=0.600V			100110=1.200V		111011=1.200V		
		010000=0.600V			100111=1.200V		111100=1.200V		
		010001=0.600V			101000=1.200V		111101=1.200V		
		010010=0.600V			101001=1.200V		111110=1.200V		
		010011=0.600V			101010=1.200V		111111=1.200V		
		010100=0.600V							
		010101=0.600V							

**Serial Codes for BUCK1 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12	8x	EN	--	--	--	--	--	FLTMSK	PG
		R/W	--	--	--	--	--	R/W	R
Name	Default	Description							
EN	1	BUCK1 ON/OFF Bit. 0=Disable. 1=Enable. (Default)							
FLTMSK	0	BUCK1 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	BUCK1 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Serial Codes for BUCK2 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20/21	10	--	--	VSETL/VSETH					
		--	--	R/W					
Name	Default	Description							
VSETL VSETH	1.0V	BUCK2 Output Voltage Selection. 000000=0.600V 000001=0.625V 000010=0.650V 000011=0.675V 000100=0.700V 000101=0.725V 000110=0.750V 000111=0.775V 001000=0.800V 001001=0.825V 001010=0.850V 001011=0.875V 001100=0.900V 001101=0.925V 001110=0.950V 001111=0.975V 010000=1.000V (Default) 010001=1.025V 010010=1.050V 010011=1.075V 010100=1.100V 010101=1.125V 010110=1.150V 010111=1.175V 011000=1.200V 011001=1.250V 011010=1.300V 011011=1.350V 011100=1.400V 011101=1.450V 011110=1.500V 011111=1.550V 100000=1.600V 100001=1.650V 100010=1.700V 100011=1.750V 100100=1.800V 100101=1.850V 100110=1.900V 100111=1.950V 101000=2.000V 101001=2.050V 101010=2.100V 101011=2.150V 101100=2.200V 101101=2.250V 101110=2.300V 101111=2.350V 110000=2.400V 110001=2.500V 110010=2.600V 110011=2.700V 110100=2.800V 110101=2.900V 110110=3.000V 110111=3.100V 111000=3.200V 111001=3.300V 111010=3.400V 111011=3.500V 111100=3.600V 111101=3.700V 111110=3.800V 111111=3.900V							

**Serial Codes for BUCK2 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
22	8x	EN	--	--	--	--	--	FLTMSK	PG
		R/W	--	--	--	--	--	R/W	R
Name	Default	Description							
EN	1	BUCK2 ON/OFF Bit. 0=Disable. 1=Enable. (Default)							
FLTMSK	0	BUCK2 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	BUCK2 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							



**Serial Codes for BUCK4 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40/41	39	--	--	VSETL/VSETH					
		--	--	R/W					
Name	Default	Description							
VSETL VSETH	3.3V	BUCK4 Output Voltage Selection. 000000=0.600V 000001=0.625V 000010=0.650V 000011=0.675V 000100=0.700V 000101=0.725V 000110=0.750V 000111=0.775V 001000=0.800V 001001=0.825V 001010=0.850V 001011=0.875V 001100=0.900V 001101=0.925V 001110=0.950V 001111=0.975V 010000=1.000V 010001=1.025V 010010=1.050V 010011=1.075V 010100=1.100V 010101=1.125V 010110=1.150V 010111=1.175V 011000=1.200V 011001=1.250V 011010=1.300V 011011=1.350V 011100=1.400V 011101=1.450V 011110=1.500V 011111=1.550V 100000=1.600V 100001=1.650V 100010=1.700V 100011=1.750V 100100=1.800V 100101=1.850V 100110=1.900V 100111=1.950V 101000=2.000V 101001=2.050V 101010=2.100V 101011=2.150V 101100=2.200V 101101=2.250V 101110=2.300V 101111=2.350V 110000=2.400V 110001=2.500V 110010=2.600V 110011=2.700V 110100=2.800V 110101=2.900V 110110=3.000V 110111=3.100V 111000=3.200V 111001=3.300V (Default) 111010=3.400V 111011=3.500V 111100=3.600V 111101=3.700V 111110=3.800V 111111=3.900V							

**Serial Codes for BUCK4 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42	8x	EN	--	--	--	--	--	FLTMSK	PG
		R/W	--	--	--	--	--	R/W	R
Name	Default	Description							
EN	1	BUCK4 ON/OFF Bit. 0=Disable. 1=Enable. (Default)							
FLTMSK	0	BUCK4 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	BUCK4 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							



**Serial Codes for LDO2 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
58	18	--	--	VSET					
		--	--	R/W					
Name	Default	Description							
VSET	1.2V	LDO2 Output Voltage Selection.			010110=1.150V			101011=2.150V	
		000000=0.600V			010111=1.175V			101100=2.200V	
		000001=0.625V			011000=1.200V (Default)			101101=2.250V	
		000010=0.650V			011001=1.250V			101110=2.300V	
		000011=0.675V			011010=1.300V			101111=2.350V	
		000100=0.700V			011011=1.350V			110000=2.400V	
		000101=0.725V			011100=1.400V			110001=2.500V	
		000110=0.750V			011101=1.450V			110010=2.600V	
		000111=0.775V			011110=1.500V			110011=2.700V	
		001000=0.800V			011111=1.550V			110100=2.800V	
		001001=0.825V			100000=1.600V			110101=2.900V	
		001010=0.850V			100001=1.650V			110110=3.000V	
		001011=0.875V			100010=1.700V			110111=3.100V	
		001100=0.900V			100011=1.750V			111000=3.200V	
		001101=0.925V			100100=1.800V			111001=3.300V	
		001110=0.950V			100101=1.850V			111010=3.400V	
		001111=0.975V			100110=1.900V			111011=3.500V	
		010000=1.000V			100111=1.950V			111100=3.600V	
		010001=1.025V			101000=2.000V			111101=3.700V	
		010010=1.050V			101001=2.050V			111110=3.800V	
		010011=1.075V			101010=2.100V			111111=3.900V	
		010100=1.100V							
		010101=1.125V							

**Serial Codes for LDO2 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
59	0x	EN	--	--	--	--	DIS	FLTMSK	PG
		R/W	--	--	--	--	R/W	R/W	R
Name	Default	Description							
EN	0	LDO2 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
DIS	1	LDO2 OFF Discharge Control. 0=Disable discharge. 1=Enable discharge. (Default)							
FLTMSK	0	LDO2 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	LDO2 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Serial Codes for LDO3 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60	24	--	--	VSET					
		--	--	R/W					
Name	Default	Description							
VSET	1.8V	LDO3 Output Voltage Selection.			010110=1.150V			101011=2.150V	
		000000=0.600V			010111=1.175V			101100=2.200V	
		000001=0.625V			011000=1.200V			101101=2.250V	
		000010=0.650V			011001=1.250V			101110=2.300V	
		000011=0.675V			011010=1.300V			101111=2.350V	
		000100=0.700V			011011=1.350V			110000=2.400V	
		000101=0.725V			011100=1.400V			110001=2.500V	
		000110=0.750V			011101=1.450V			110010=2.600V	
		000111=0.775V			011110=1.500V			110011=2.700V	
		001000=0.800V			011111=1.550V			110100=2.800V	
		001001=0.825V			100000=1.600V			110101=2.900V	
		001010=0.850V			100001=1.650V			110110=3.000V	
		001011=0.875V			100010=1.700V			110111=3.100V	
		001100=0.900V			100011=1.750V			111000=3.200V	
		001101=0.925V			100100=1.800V (Default)			111001=3.300V	
		001110=0.950V			100101=1.850V			111010=3.400V	
		001111=0.975V			100110=1.900V			111011=3.500V	
		010000=1.000V			100111=1.950V			111100=3.600V	
		010001=1.025V			101000=2.000V			111101=3.700V	
		010010=1.050V			101001=2.050V			111110=3.800V	
		010011=1.075V			101010=2.100V			111111=3.900V	
		010100=1.100V							
		010101=1.125V							

**Serial Codes for LDO3 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
61	0x	EN	--	--	--	--	DIS	FLTMSK	PG
		R/W	--	--	--	--	R/W	R/W	R
Name	Default	Description							
EN	0	LDO3 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
DIS	1	LDO3 OFF Discharge Control. 0=Disable discharge. 1=Enable discharge. (Default)							
FLTMSK	0	LDO3 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	LDO3 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Serial Codes for LDO4 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
68	39	--	--	VSET					
		--	--	R/W					
Name	Default	Description							
VSET	3.3V	LDO4 Output Voltage Selection. 000000=0.600V 000001=0.625V 000010=0.650V 000011=0.675V 000100=0.700V 000101=0.725V 000110=0.750V 000111=0.775V 001000=0.800V 001001=0.825V 001010=0.850V 001011=0.875V 001100=0.900V 001101=0.925V 001110=0.950V 001111=0.975V 010000=1.000V 010001=1.025V 010010=1.050V 010011=1.075V 010100=1.100V 010101=1.125V 010110=1.150V 010111=1.175V 011000=1.200V 011001=1.250V 011010=1.300V 011011=1.350V 011100=1.400V 011101=1.450V 011110=1.500V 011111=1.550V 100000=1.600V 100001=1.650V 100010=1.700V 100011=1.750V 100100=1.800V 100101=1.850V 100110=1.900V 100111=1.950V 101000=2.000V 101001=2.050V 101010=2.100V 101011=2.150V 101100=2.200V 101101=2.250V 101110=2.300V 101111=2.350V 110000=2.400V 110001=2.500V 110010=2.600V 110011=2.700V 110100=2.800V 110101=2.900V 110110=3.000V 110111=3.100V 111000=3.200V 111001=3.300V (Default) 111010=3.400V 111011=3.500V 111100=3.600V 111101=3.700V 111110=3.800V 111111=3.900V							

**Serial Codes for LDO4 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
69	0x	EN	--	--	--	--	DIS	FLTMSK	PG
		R/W	--	--	--	--	R/W	R/W	R
Name	Default	Description							
EN	0	LDO4 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
DIS	1	LDO4 OFF Discharge Control. 0=Disable discharge. 1=Enable discharge. (Default)							
FLTMSK	0	LDO4 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	LDO4 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Serial Codes for LDO5 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
70	39	--	--	VSET						
		--	--	R/W						
Name	Default	Description								
VSET	3.3V	LDO5 Output Voltage Selection.			010110=1.150V	101011=2.150V				
		000000=0.600V		010111=1.175V	101100=2.200V					
		000001=0.625V		011000=1.200V	101101=2.250V					
		000010=0.650V		011001=1.250V	101110=2.300V					
		000011=0.675V		011010=1.300V	101111=2.350V					
		000100=0.700V		011011=1.350V	110000=2.400V					
		000101=0.725V		011100=1.400V	110001=2.500V					
		000110=0.750V		011101=1.450V	110010=2.600V					
		000111=0.775V		011110=1.500V	110011=2.700V					
		001000=0.800V		011111=1.550V	110100=2.800V					
		001001=0.825V		100000=1.600V	110101=2.900V					
		001010=0.850V		100001=1.650V	110110=3.000V					
		001011=0.875V		100010=1.700V	110111=3.100V					
		001100=0.900V		100011=1.750V	111000=3.200V					
		001101=0.925V		100100=1.800V	111001=3.300V (Default)					
		001110=0.950V		100101=1.850V	111010=3.400V					
		001111=0.975V		100110=1.900V	111011=3.500V					
		010000=1.000V		100111=1.950V	111100=3.600V					
		010001=1.025V		101000=2.000V	111101=3.700V					
		010010=1.050V		101001=2.050V	111110=3.800V					
		010011=1.075V		101010=2.100V	111111=3.900V					
		010100=1.100V								
		010101=1.125V								

**Serial Codes for LDO5 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
71	0x	EN	--	--	--	--	DIS	FLTMSK	PG
		R/W	--	--	--	--	R/W	R/W	R
Name	Default	Description							
EN	0	LDO5 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
DIS	1	LDO5 OFF Discharge Control. 0=Disable discharge. 1=Enable discharge. (Default)							
FLTMSK	0	LDO5 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	LDO5 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Serial Codes for LDO6 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
80	39	--	--	VSET					
		--	--	R/W					
Name	Default	Description							
VSET	3.3V	LDO6 Output Voltage Selection. 000000=0.600V 000001=0.625V 000010=0.650V 000011=0.675V 000100=0.700V 000101=0.725V 000110=0.750V 000111=0.775V 001000=0.800V 001001=0.825V 001010=0.850V 001011=0.875V 001100=0.900V 001101=0.925V 001110=0.950V 001111=0.975V 010000=1.000V 010001=1.025V 010010=1.050V 010011=1.075V 010100=1.100V 010101=1.125V 010110=1.150V 010111=1.175V 011000=1.200V 011001=1.250V 011010=1.300V 011011=1.350V 011100=1.400V 011101=1.450V 011110=1.500V 011111=1.550V 100000=1.600V 100001=1.650V 100010=1.700V 100011=1.750V 100100=1.800V 100101=1.850V 100110=1.900V 100111=1.950V 101000=2.000V 101001=2.050V 101010=2.100V 101011=2.150V 101100=2.200V 101101=2.250V 101110=2.300V 101111=2.350V 110000=2.400V 110001=2.500V 110010=2.600V 110011=2.700V 110100=2.800V 110101=2.900V 110110=3.000V 110111=3.100V 111000=3.200V 111001=3.300V (Default) 111010=3.400V 111011=3.500V 111100=3.600V 111101=3.700V 111110=3.800V 111111=3.900V							

**Serial Codes for LDO6 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
81	0x	EN	--	--	--	--	DIS	FLTMSK	PG
		R/W	--	--	--	--	R/W	R/W	R
Name	Default	Description							
EN	0	LDO6 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
DIS	1	LDO5 OFF Discharge Control. 0=Disable discharge. 1=Enable discharge. (Default)							
FLTMSK	0	LDO5 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	LDO5 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Serial Codes for LDO7 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
90	24	--	--	VSET					
		--	--	R/W					
Name	Default	Description							
VSET	1.8V	LDO7 Output Voltage Selection. 000000=0.600V 000001=0.625V 000010=0.650V 000011=0.675V 000100=0.700V 000101=0.725V 000110=0.750V 000111=0.775V 001000=0.800V 001001=0.825V 001010=0.850V 001011=0.875V 001100=0.900V 001101=0.925V 001110=0.950V 001111=0.975V 010000=1.000V 010001=1.025V 010010=1.050V 010011=1.075V 010100=1.100V 010101=1.125V 010110=1.150V 010111=1.175V 011000=1.200V 011001=1.250V 011010=1.300V 011011=1.350V 011100=1.400V 011101=1.450V 011110=1.500V 011111=1.550V 100000=1.600V 100001=1.650V 100010=1.700V 100011=1.750V 100100=1.800V (Default) 100101=1.850V 100110=1.900V 100111=1.950V 101000=2.000V 101001=2.050V 101010=2.100V 101011=2.150V 101100=2.200V 101101=2.250V 101110=2.300V 101111=2.350V 110000=2.400V 110001=2.500V 110010=2.600V 110011=2.700V 110100=2.800V 110101=2.900V 110110=3.000V 110111=3.100V 111000=3.200V 111001=3.300V 111010=3.400V 111011=3.500V 111100=3.600V 111101=3.700V 111110=3.800V 111111=3.900V							

**Serial Codes for LDO7 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
91	8x	EN	--	--	--	--	DIS	FLTMSK	PG
		R/W	--	--	--	--	R/W	R/W	R
Name	Default	Description							
EN	1	LDO7 ON/OFF Bit. 0=Disable. 1=Enable. (Default)							
DIS	1	LDO7 OFF Discharge Control. 0=Disable discharge. 1=Enable discharge. (Default)							
FLTMSK	0	LDO7 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	LDO7 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Serial Codes for LDO8 Output Voltage Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
A0	34	--	--	VSET						
		--	--	R/W						
Name	Default	Description								
VSET	2.8V	LDO8 Output Voltage Selection.			010110=1.150V	101011=2.150V				
		000000=0.600V		010111=1.175V	101100=2.200V					
		000001=0.625V		011000=1.200V	101101=2.250V					
		000010=0.650V		011001=1.250V	101110=2.300V					
		000011=0.675V		011010=1.300V	101111=2.350V					
		000100=0.700V		011011=1.350V	110000=2.400V					
		000101=0.725V		011100=1.400V	110001=2.500V					
		000110=0.750V		011101=1.450V	110010=2.600V					
		000111=0.775V		011110=1.500V	110011=2.700V					
		001000=0.800V		011111=1.550V	110100=2.800V (Default)					
		001001=0.825V		100000=1.600V	110101=2.900V					
		001010=0.850V		100001=1.650V	110110=3.000V					
		001011=0.875V		100010=1.700V	110111=3.100V					
		001100=0.900V		100011=1.750V	111000=3.200V					
		001101=0.925V		100100=1.800V	111001=3.300V					
		001110=0.950V		100101=1.850V	111010=3.400V					
		001111=0.975V		100110=1.900V	111011=3.500V					
		010000=1.000V		100111=1.950V	111100=3.600V					
		010001=1.025V		101000=2.000V	111101=3.700V					
		010010=1.050V		101001=2.050V	111110=3.800V					
		010011=1.075V		101010=2.100V	111111=3.900V					
		010100=1.100V								
		010101=1.125V								

**Serial Codes for LDO8 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A1	0x	EN	--	--	--	--	DIS	FLTMSK	PG
		R/W	--	--	--	--	R/W	R/W	R
Name	Default	Description							
EN	0	LDO8 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
DIS	1	LDO8 OFF Discharge Control. 0=Disable discharge. 1=Enable discharge. (Default)							
FLTMSK	0	LDO8 Fault Interrupt ON/OFF Control. 0=Disable the interrupt. (Default) 1=Enable the interrupt.							
PG	R	LDO8 Power-Good Interrupt Status. This bit is automatically cleared to 0 after read. 0= Output Voltage is not Power-Good. 1= Output Voltage is Power-Good.							

**Functional Description**
**Serial Codes for LDO9 State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B1		EN	--	--	--	--	--	--	--
		R/W	--	--	--	--	--	--	--
Name	Default	Description							
EN	1	LDO9 ON/OFF Bit. 0=Disable. 1=Enable. (Default)							

**Serial Codes for PMU Control State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C0	00	PBAMSK	PBDMSK	--	--	--	--	WDSREN	WDPCEN
		R/W	R/W	--	--	--	--	R/W	R/W
Name	Default	Description							
PBAMSK	0	/PWRON Active Interrupt ON/OFF Control. 0=Disable. (Default) 1=Enable.							
PBDMSK	0	/PWRON Non-Active Interrupt ON/OFF Control. 0=Disable. (Default) 1=Enable.							
WDSREN	0	Watchdog Soft-Reset ON/OFF Control. When the watchdog timer expires, the PMU commences a soft-reset routine. This bit is automatically reset to 0 when entering sleep mode. 0=Disable. (Default) 1=Enable.							
WDPCEN	0	Watchdog Power Cycle ON/OFF Control. When watchdog timer expires, the PMU commence a power cycle. This bit is automatically reset to 0 when entering sleep mode. 0=Disable. (Default) 1=Enable.							

**Serial Codes for PWM4 LED Driver State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E3		EN	FREQ			DUTY			
		R/W	R/W			R/W			
Name	Default	Description							
EN	0	PWM4 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
FREQ	000	PWM4 Frequency Selection Bits. 000=0.25Hz. (Default) 001=0.5Hz. 010=1Hz. 011=2Hz. 100=128Hz. 101=256Hz.							
DUTY	0000	PWM4 Duty Cycle Selection Bits. 0000=06.25% (Default) 0001=12.50% 0010=18.75% 0011=25.00% 0100=31.25% 0101=37.50% 0110=43.75% 0111=50.00%				1000=56.25% 1001=62.50% 1010=68.75% 1011=75.00% 1100=81.25% 1101=87.50% 1110=93.75% 1111=100.0%			

**Serial Codes for PWM3 LED Driver State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E4		EN	FREQ			DUTY			
		R/W	R/W			R/W			
Name	Default	Description							
EN	0	PWM3 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
FREQ	000	PWM3 Frequency Selection Bits. 000=0.25Hz. (Default) 001=0.5Hz. 010=1Hz. 011=2Hz. 100=128Hz. 101=256Hz.							
DUTY	0000	PWM3 Duty Cycle Selection Bits. 0000=06.25% (Default) 0001=12.50% 0010=18.75% 0011=25.00% 0100=31.25% 0101=37.50% 0110=43.75% 0111=50.00%				1000=56.25% 1001=62.50% 1010=68.75% 1011=75.00% 1100=81.25% 1101=87.50% 1110=93.75% 1111=100.0%			

**Functional Description**
**Serial Codes for PWM1 LED Driver State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
F4		EN	FREQ			DUTY			
		R/W	R/W			R/W			
Name	Default	Description							
EN	1	PWM1 ON/OFF Bit. 0=Disable. 1=Enable. (Default)							
FREQ	101	PWM1 Frequency Selection Bits. 000=0.25Hz. 001=0.5Hz. 010=1Hz. 011=2Hz. 100=128Hz. 101=256Hz. (Default)							
DUTY	0111	PWM1 Duty Cycle Selection Bits. 0000=06.25% 0001=12.50% 0010=18.75% 0011=25.00% 0100=31.25% 0101=37.50% 0110=43.75% 0111=50.00% (Default)				1000=56.25% 1001=62.50% 1010=68.75% 1011=75.00% 1100=81.25% 1101=87.50% 1110=93.75% 1111=100.0%			

**Serial Codes for PWM2 LED Driver State Register**

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
F5		EN	FREQ			DUTY			
		R/W	R/W			R/W			
Name	Default	Description							
EN	0	PWM2 ON/OFF Bit. 0=Disable. (Default) 1=Enable.							
FREQ	000	PWM2 Frequency Selection Bits. 000=0.25Hz. (Default) 001=0.5Hz. 010=1Hz. 011=2Hz. 100=128Hz. 101=256Hz.							
DUTY	0000	PWM2 Duty Cycle Selection Bits. 0000=06.25% (Default) 0001=12.50% 0010=18.75% 0011=25.00% 0100=31.25% 0101=37.50% 0110=43.75% 0111=50.00%				1000=56.25% 1001=62.50% 1010=68.75% 1011=75.00% 1100=81.25% 1101=87.50% 1110=93.75% 1111=100.0%			

Functional Description

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C1	FF	INTADR							
		R							
Name	Default	Description							
INTADR	R	Interrupt Index. It holds the Index of the block that triggers the interrupt. This byte defaults to 0xFF and is automatically set to 0xFF after being read. Bit 7 is the MSB while Bit 0 is the LSB.							

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C2	xx	PBASTAT	PBDSTAT	PBDAT	--	--	--	--	--
		R	R	R	--	--	--	--	--
Name	Default	Description							
PBASTAT	R	/PWRON Active Interrupt Status. This bit is automatically cleared to 0 after read. 0= /PWRON active interrupt is normal. 1= /PWRON active interrupt is generated.							
PBDSTAT	R	/PWRON Non-Active Interrupt Status. This bit is automatically cleared to 0 after read. 0= /PWRON non-active interrupt is normal. 1= /PWRON non-active interrupt is generated.							
PBDAT	R	/PWRON Status bit. This bit contains the real-time status of the /PWRON pin. 0= /PWRON is non-active. 1= /PWRON is active.							

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C3	00	--	--	--	OFFSYS	--	--	--	SIPC
		--	--	--	R/W	--	--	--	R/W
Name	Default	Description							
OFFSYS	0	Power Off Control. Set this bit to 1 to turn off all outputs. 0=Power is normal. (Default) 1=Power is off.							
SIPC	0	Software Initiated Power Cycle ON/OFF Control. This bit is automatically cleared to 0. When this bit is set, the PMU commences a power cycle after 8ms delay. 0=Disable. (Default) 1=Enable.							

*Functional Description*

Index (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C5	xx	--	--	--	--	--	--	PCSTAT	SRSTAT
		--	--	--	--	--	--	R	R
Name	Default	Description							
PCSTAT	R	Power-cycle Indicator. The value of this bit is 1 after a power cycle. This bit is automatically cleared to 0 after read.							
SRSTAT	R	Soft-reset Indicator. The value of this bit is 1 after a soft-reset. This bit is automatically cleared to 0 after read.							

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**Absolute Maximum Rating**

(Note 1)

Supply Input Voltage, IN1, IN2, IN3, IN4, IN5, IN6, IN7 to GND	-0.3V to +5.5V
LX_Pin Voltage	-0.3V to (IN_+0.3V)
Other Pins	-0.3V to (IN_+0.3V)
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

**Thermal Information**

Package Thermal Resistance (Note 3)

VQFN6x6-48L $\theta_{JA}$	35°C/W
VQFN6x6-48L $\theta_{JC}$	3°C/W
Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$	
VQFN6x6-48L	2.86W

**Recommended Operation Conditions**

(Note 4)

Operating Junction Temperature Range	-40°C to +125°C
Operating Ambient Temperature Range	-40°C to +85°C
Supply Input Voltage	2.7V to 5.3V

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Electrical Characteristics**
 $(V_{IN}=3.7V, C_{REF}=0.1\mu F, T_A=25^\circ C \text{ unless otherwise specified})$ 

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Reference</b>						
Reference Output Voltage	VREF	$C_{REF}=0.1\mu F$	1.237	1.25	1.263	V
Power ON Sequence Delay Time	$T_{ON-DY}$	Channel to channel	--	2	--	ms
Power OFF Sequence Delay Time	$T_{OFF-DY}$	PWRHLD to channel off	--	2	--	ms
<b>BUCK Converter : BUCK1, BUCK2, BUCK3, BUCK4</b>						
Input Voltage Range	$V_{IN1-4}$	$I_{BUCK} = 0mA$	2.7	--	5.3	V
POR Threshold	$V_{INPOR}$	$V_{IN1-4}$ Rising	--	--	2.5	V
		$V_{IN1-4}$ Falling	2.2	--	--	
Supply Current	$I_Q$	Enable BUCK, No switching.	--	120	TBD	$\mu A$
Shutdown Current	$I_{SD}$	Disable BUCK	--	0	2	$\mu A$
Default Output Voltage Accuracy	$V_{DF}$	$V_{BUCK} \geq 1.0V, I_{BUCK} = 10mA$	-1.00	--	1.00	%
		$V_{BUCK} < 1.0V, I_{BUCK} = 10mA$	-10	--	10	mV
Line Regulation	$\Delta V_{LINE}$	$IN_=2.7V \text{ to } 5.5V, I_{BUCK} = 100mA$	--	0.15	--	%/V
Load Regulation	$\Delta V_{LOAD}$	$I_{BUCK1/4} = 10mA \text{ to } 1.5A$	--	1.7	--	%/A
		$I_{BUCK2/3} = 10mA \text{ to } 2.8A$	--	1.0	--	
Power Good Threshold	$V_{BUCKPG}$	$V_{BUCK}$ Rising	--	90	--	% $V_{DF}$
		$V_{BUCK}$ Falling	--	85	--	
Switching Frequency Range	$F_{OSC}$	PWM	2.0	2.25	2.5	MHz
Soft Start Time	SS		--	1	--	ms
Minimum On Time	$T_{on-min}$		--	80	--	ns
Maximum Output Current	$I_{MAX}$	BUCK1, BUCK4	1.5	--	--	A
		BUCK2, BUCK3	2.8	--	--	
Current Limit	$I_{CL}$	BUCK1, BUCK4	1.8	2.2	2.7	A
		BUCK2, BUCK3	3.5	4.2	4.9	
ON Resistance	$R_{ON}$	BUCK1, BUCK4; High-side MOS; $I_{LX1/4}=100mA.$	--	110	--	m $\Omega$
		BUCK1, BUCK4; Low-side MOS; $I_{LX1/4}=100mA.$	--	80	--	
		BUCK2, BUCK3; High-side MOS; $I_{LX2/3}=100mA.$	--	70	--	
		BUCK2, BUCK3; Low-side MOS; $I_{LX2/3}=100mA.$	--	80	--	

**Electrical Characteristics**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Shutdown Discharge Resistance	$R_{DIS}$	BUCK Disable	--	1.0	--	k $\Omega$
LX Leakage Current	$I_{LX-LK}$	Disable BUCK, IN=5.5V, LX=0V or 5.5V.	--	0	2	$\mu$ A
<b>Low Noise Linear Regulator : LDO1, LDO2, LDO3, LDO4, LDO5</b>						
Input Voltage Range	$V_{IN5-6}$	IN5, $I_{LDO1-3} = 0mA$	2.5	--	5.3	V
		IN6, $I_{LDO4-5} = 0mA$	2.7	--	5.5	
POR Threshold	$V_{IN6POR}$	$V_{IN6}$ Rising	--	--	2.2	V
		$V_{IN6}$ Falling	1.8	--	--	
Default Output Voltage Accuracy	$V_{DF}$	$V_{LDO} \geq 1.0V$ , $I_{LDO} = 10mA$	-1.00	--	1.00	%
		$V_{LDO} < 1.0V$ , $I_{LDO} = 10mA$	-10	--	10	mV
Line Regulation	$\Delta V_{LINE}$	IN5-6 = 3.0V to 5.5V, $I_{LDO} = 10mA$	--	0.5	--	mV
Load Regulation	$\Delta V_{LOAD}$	$I_{LDO1/2} = 1mA$ to 150mA	--	0.1	--	V/A
		$I_{LDO3/4/5} = 1mA$ to 350mA	--	0.1	--	
PSRR	PSRR	1kHz, $V_{LDO} = 1.2V$ , $I_{LDO} = 20mA$	--	70	--	dB
		10kHz, $V_{LDO} = 1.2V$ , $I_{LDO} = 20mA$	--	50	--	
Supply Current	$I_Q$	Enable LDO	--	60	--	$\mu$ A
Shutdown Current	$I_{SD}$	Disable LDO	--	0	2	$\mu$ A
Soft Start Time	SS	$V_{LDO} = 3.0V$	--	500	--	$\mu$ s
Power Good Threshold	$V_{LDOPG}$	$V_{LDO}$ Rising	--	90	--	% $V_{DF}$
		$V_{LDO}$ Falling	--	85	--	
Output Noise	$V_{NOISE}$	10Hz-100kHz, $V_{LDO} = 1.2V$ , $I_{LDO} = 20mA$	--	50	--	$\mu$ V <sub>RMS</sub>
Shutdown Discharge Resistance	$R_{DIS}$	LDO Disable, DIS[2]=1	--	1.5	--	k $\Omega$
Dropout Voltage	$V_{DV}$	LDO1, LDO2; $I_{LDO} = 80mA$ , $V_{LDO} > 3.1V$	--	140	280	mV
		LDO3, LDO4, LDO5; $I_{LDO} = 160mA$ , $V_{LDO} > 3.1V$	--	140	280	
Maximum Output Current	$I_{MAX}$	LDO1, LDO2	150	--	--	mA
		LDO3, LDO4, LDO5	350	--	--	
Current Limit	$I_{CL}$	LDO1, LDO2; $V_{LDO} = 0.95 \times VDF$	180	260	340	mA
		LDO3, LDO4, LDO5; $V_{LDO} = 0.95 \times VDF$	400	500	600	
Output Short Circuit Current Limit	$I_{SCL}$	LDO1, LDO2; $V_{LDO} = 0V$	45	65	85	mA
		LDO3, LDO4, LDO5; $V_{LDO} = 0V$	85	125	165	

**Electrical Characteristics**

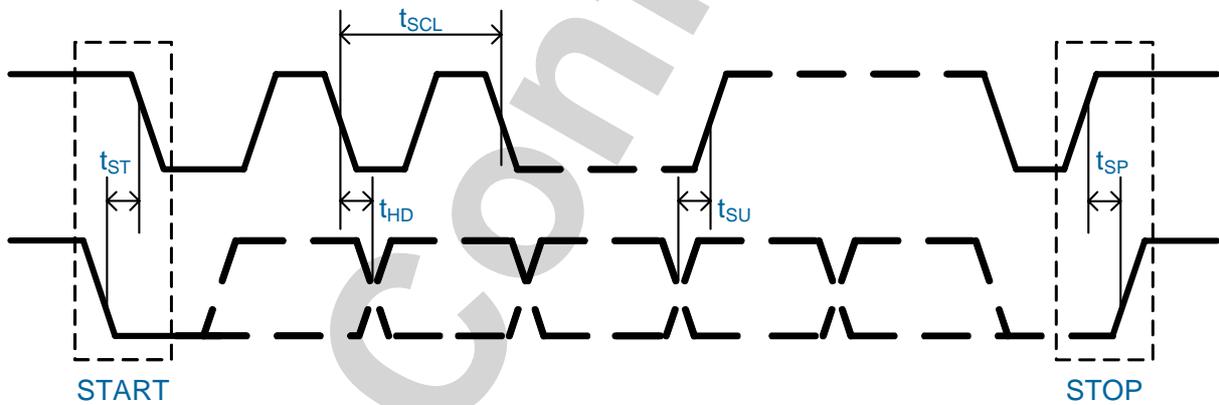
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Low Input Voltage Linear Regulator : LDO6, LDO7, LDO8</b>						
Input Voltage Range	$V_{IN7}$	IN7, $I_{LDO6-8} = 0\text{mA}$	1.7	--	5.3	V
Default Output Voltage Accuracy	$V_{DF}$	$V_{LDO} \geq 1.0\text{V}$ , $I_{LDO} = 10\text{mA}$	-1.00	--	1.00	%
		$V_{LDO} < 1.0\text{V}$ , $I_{LDO} = 10\text{mA}$	-10	--	10	mV
Line Regulation	$\Delta V_{LINE}$	IN7=3.0V to 5.5V, $I_{LDO} = 10\text{mA}$	--	0.5	--	mV
Load Regulation	$\Delta V_{LOAD}$	$I_{LDO6} = 1\text{mA}$ to 150mA	--	0.1	--	V/A
		$I_{LDO7/8} = 1\text{mA}$ to 350mA	--	0.1	--	
PSRR	PSRR	1kHz, $V_{LDO} = 1.2\text{V}$ , $I_{LDO} = 20\text{mA}$	--	50	--	dB
		10kHz, $V_{LDO} = 1.2\text{V}$ , $I_{LDO} = 20\text{mA}$	--	30	--	
Supply Current	$I_Q$	Enable LDO	--	50	--	$\mu\text{A}$
Shutdown Current	$I_{SD}$	Disable LDO	--	0	2	$\mu\text{A}$
Soft Start Time	SS	$V_{LDO} = 3.0\text{V}$	--	500	--	$\mu\text{s}$
Power Good Threshold	$V_{LDOPG}$	$V_{LDO}$ Rising	--	90	--	% $V_{DF}$
		$V_{LDO}$ Falling	--	85	--	
Output Noise	$V_{NOISE}$	10Hz-100kHz, $V_{LDO} = 1.2\text{V}$ , $I_{LDO} = 20\text{mA}$	--	50	--	$\mu\text{V}_{RMS}$
Shutdown Discharge Resistance	$R_{DIS}$	LDO Disable, DIS[2]=1	--	1.5	--	$\text{k}\Omega$
Dropout Voltage	$V_{DV}$	LDO6; $I_{LDO} = 80\text{mA}$ , $V_{LDO} > 3.1\text{V}$	--	100	200	mV
		LDO7, LDO8; $I_{LDO} = 160\text{mA}$ , $V_{LDO} > 3.1\text{V}$	--	100	200	
Maximum Output Current	IMAX	LDO6	150	--	--	mA
		LDO7, LDO8	350	--	--	
Current Limit	$I_{CL}$	LDO6; $V_{LDO} = 0.95 \times V_{DF}$	180	260	340	mA
		LDO7, LDO8; $V_{LDO} = 0.95 \times V_{DF}$	400	500	600	
Output Short Circuit Current Limit	$I_{SCL}$	LDO6; $V_{LDO} = 0\text{V}$	45	65	85	mA
		LDO7, LDO8; $V_{LDO} = 0\text{V}$	85	125	165	
<b>Low Input Power Linear Regulator : LDO9</b>						
Input Voltage Range	$V_{IN5}$	IN5, $I_{LDO9} = 0\text{mA}$	2.5	--	5.3	V
Default Output Voltage Accuracy	$V_{DF}$	$I_{LDO} = 10\text{mA}$	-3	--	3	%
Line Regulation	$\Delta V_{LINE}$	IN5 = 2.5V to 5.5V, $I_{out} = 1\text{mA}$	--	13	--	mV

**Electrical Characteristics**

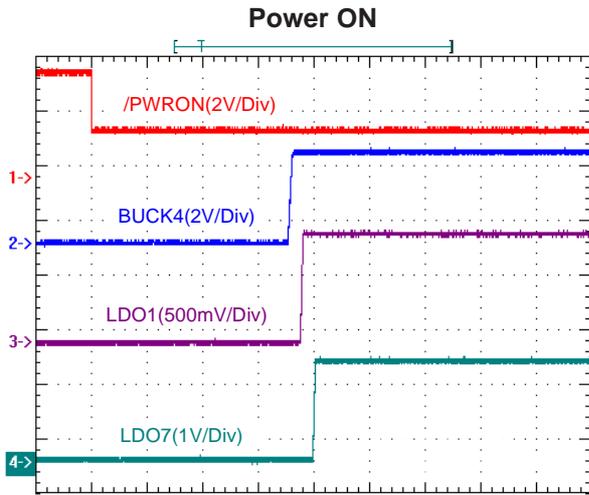
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current	$I_Q$	Enable LDO	--	5	--	uA
Maximum Output Current	$I_{MAX}$	LDO9	10	--	--	mA
Output Capacitor	$C_{OUT}$		0.47	--	--	uF
<b>PWM LED Driver</b>						
Maximum Output Current	$I_{LED-MAX}$	IN6 = 3.7V, 100% Duty Cycle	6	10	16	mA
Output Low Voltage	$V_{LED-LOW}$	PWM1-PWM4, Sink Current = 6mA	--	--	0.35	V
Output Leakage Current	$I_{LK}$	PWM1-PWM4 = 5.5V, Source Current	--	--	1	uA
PWM Frequency	FREQ	FRE[2:0] = 000	--	0.25	--	Hz
PWM Duty Range	DUTY	DUTY[3:0] = 0000 to 1111	6.26	--	100	%
<b>Low Battery Detect</b>						
Low Battery Detect Threshold	LBDT	IN6 falling, BATLEV[3:0]	2.863	2.9	2.972	V
Low Battery Hysteresis Threshold	LBHT	IN6 rising	--	0.2	--	V
<b>Logic Input and Output : /PWRON, PWRHLD, PWREN3, VSET2, VSET3, VSET4, /IRO, /RSTO, /PWRSTAT</b>						
Input High Level	$V_H$	PWRHLD, PWREN3, VSET2, VSET3, VSET4	1.4	--	--	V
Input Low Level	$V_L$	PWRHLD, PWREN3, VSET2, VSET3, VSET4	--	--	0.4	V
Leakage Current	$I_{LK}$	/IRO, /RSTO = 5.5V	--	0.1	1	uA
Output Low Voltage	$V_{LOW}$	/IRO, /RSTO, Sink Current = 5mA	--	--	0.3	V
/PWRON High Level	$V_{Standby}$	/PWRON Standby	0.9IN	--	IN	V
/PWRON Middle Level	$V_{PWR}$	PWR ON/OFF/Suspend/Resume Mode	0.4IN	--	0.6IN	V
/PWRON Low Level	$V_{RESET}$	SW/Power Cycle Reset	--	--	0.4	V
/PWRON Power Off detect Time	$T_{PWOFF-DY}$	/PWRON to Middle Level	--	8	--	s
/PWRON Reset detect Time	$T_{HWR-DY}$	/PWRON to Low Level	--	4	--	s
/PWRON Delay Time	$T_{PWR-DY}$	/PWRON to power on (after power off)	--	32	--	ms
/PWRON Delay Time	$T_{PWR-DY}$	/PWRON to power on (after IN6 power on reset)	--	500	--	ms
/PWRSTAT Falling Delay Time	$T_{STAT-FDY}$	/PWRON to /PWRSTAT falling delay time	--	32	--	ms
/RSTO Power ON Delay Time	$T_{RSTO-DY}$	BUCK1 and BUCK2 to /RSTO	--	64	--	ms
/RSTO Fault Delay Time	$T_{RSF-DY}$	BUCK4 VBUCKPG falling to /RSTO	--	1	--	ms
/RSTO Reset Delay Time	$T_{RSF-DY}$	/PWRON falling to /RSTO	--	32	--	ms
Interrupt Delay Time	$T_{INT-DY}$	Fault to /IRO	--	1	--	ms
Power Cycle Delay Time	$T_{PC-DY}$	Power OFF to Power ON(SIPC[] and WDPCEN[])	--	1	--	s

Electrical Characteristics

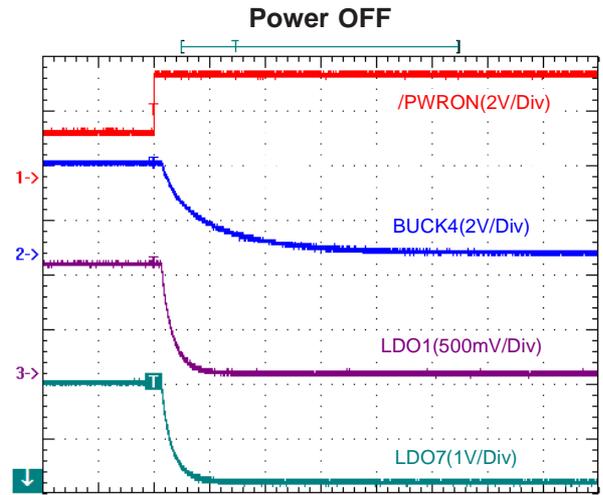
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>I2C Interface</b>						
SCL, SDA Low Level	$V_L$	IN6=3.1V to 5.5V, TA = -40°C to 85°C	--	--	0.35	V
SCL, SDA High Level	$V_H$	IN6=3.1V to 5.5V, TA = -40°C to 85°C	1.55	--	--	V
Leakage Current	$I_{LK}$	SCL, SDA = 5.5V	--	--	1	uA
SDA Output Low Voltage	$V_{OL}$	SDA, Sink Current = 5mA	--	--	0.35	V
SCL Clock Period	$t_{SCL}$		1.5	--	--	us
SDA Data Setup Time	$t_{SU}$		100	--	--	ns
SDA Data Hold Time	$t_{HD}$		300	--	--	ns
Start Setup Time	$t_{ST}$	For Start Condition	100	--	--	ns
Stop Setup Time	$t_{SP}$	For Stop Condition	100	--	--	ns
<b>Over Temperature Protection</b>						
Over Temperature Protection	OTP		--	160	--	°C
Over Temperature Hysteresis	$\Delta T$		--	20	--	°C



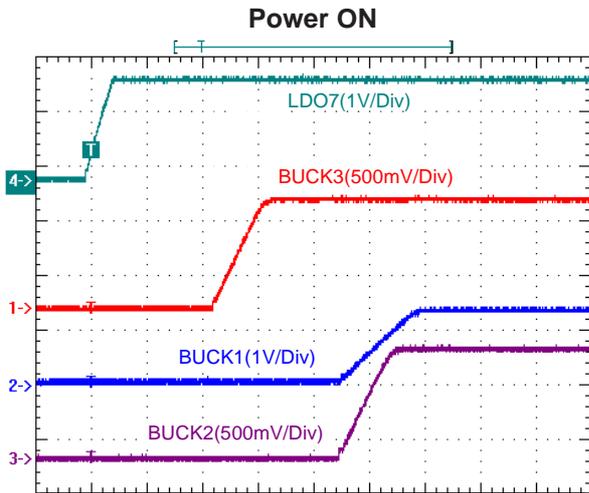
**Typical Operation Characteristics**



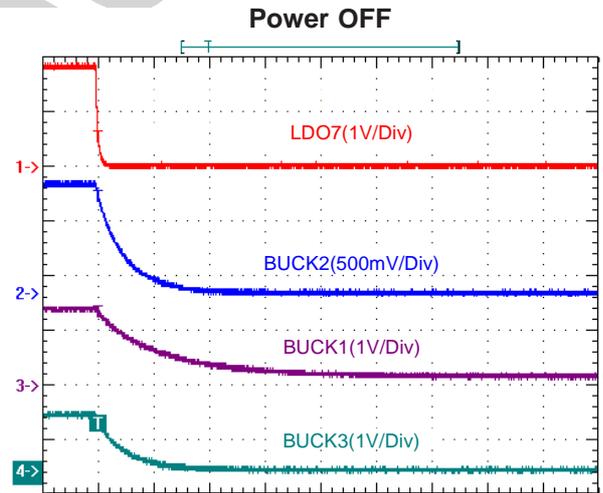
10ms/Div  
BAT = 3.8V, Load = 0mA



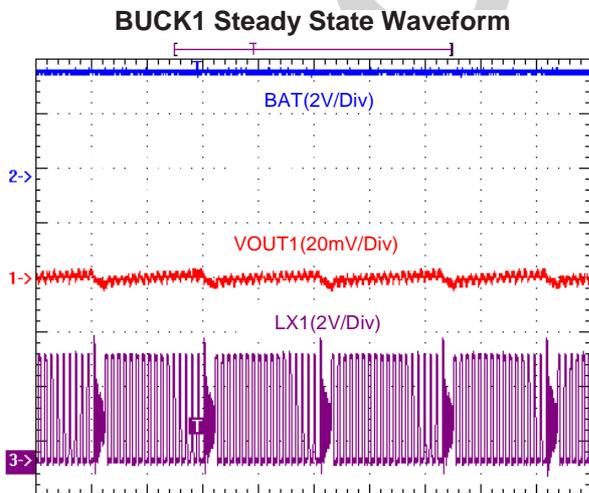
20ms/Div  
BAT = 3.8V, Load = 0mA



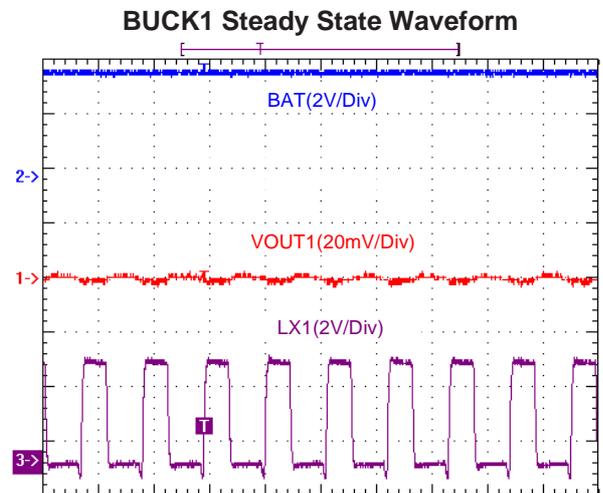
1ms/Div  
BAT = 3.8V, Load = 0mA



100ms/Div  
BAT = 3.8V, Load = 0mA



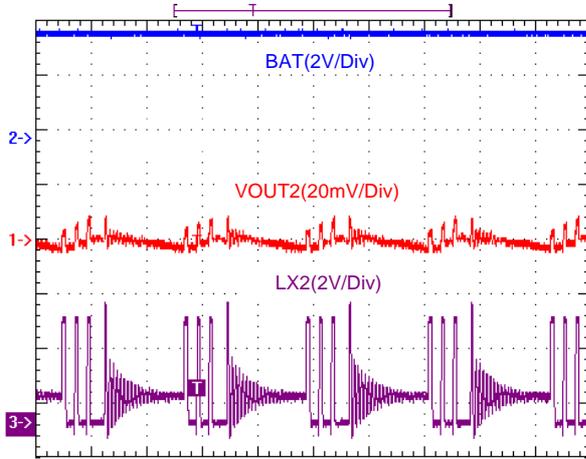
4us/Div  
BAT = 3.8V, Load = 50mA



400ns/Div  
BAT = 3.8V, Load = 1A

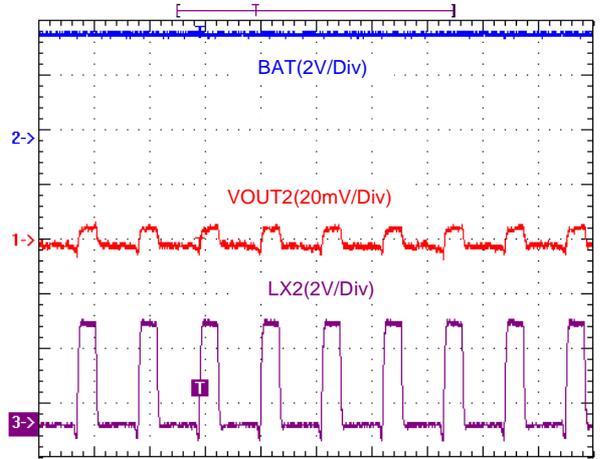
**Typical Operation Characteristics**

**BUCK2 Steady State Waveform**



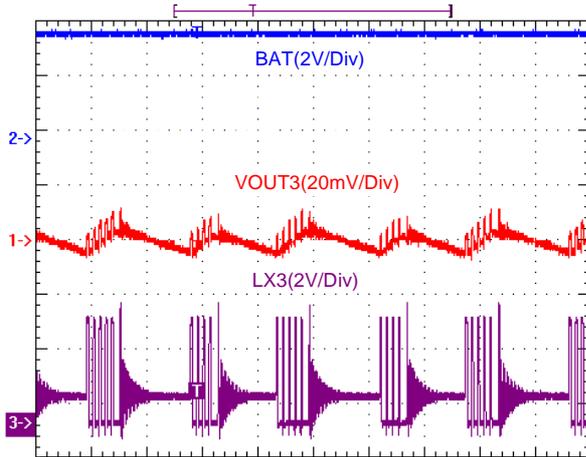
2µs/Div  
BAT = 3.8V, Load = 50mA

**BUCK2 Steady State Waveform**



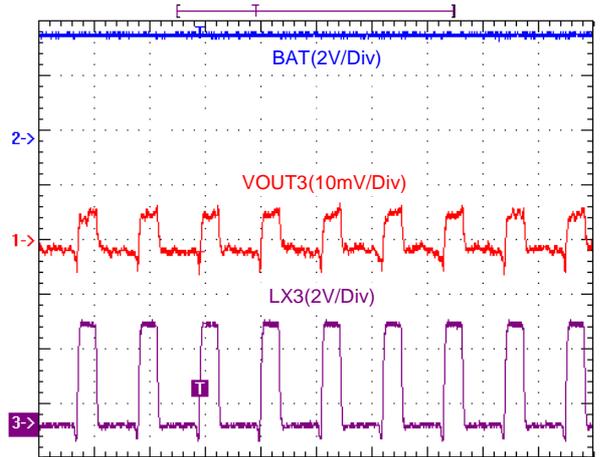
2µs/Div  
BAT = 3.8V, Load = 1A

**BUCK3 Steady State Waveform**



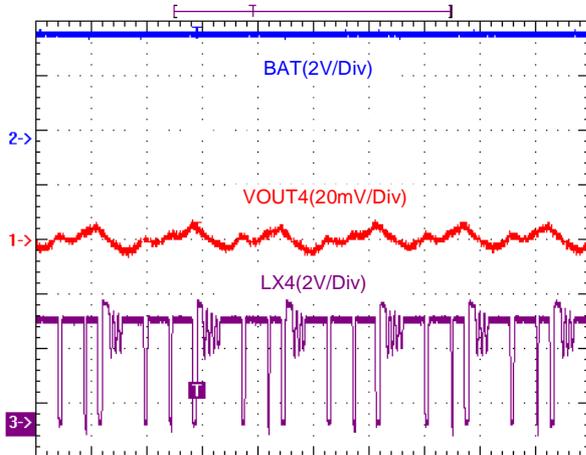
4µs/Div  
BAT = 3.8V, Load = 50mA

**BUCK3 Steady State Waveform**



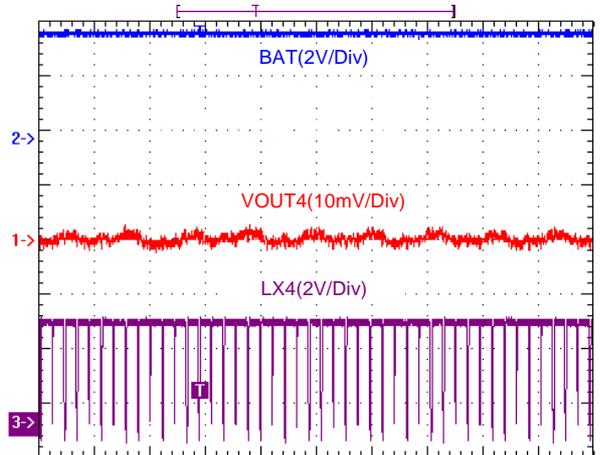
400ns/Div  
BAT = 3.8V, Load = 1A

**BUCK4 Steady State Waveform**



2µs/Div  
BAT = 3.8V, Load = 50mA

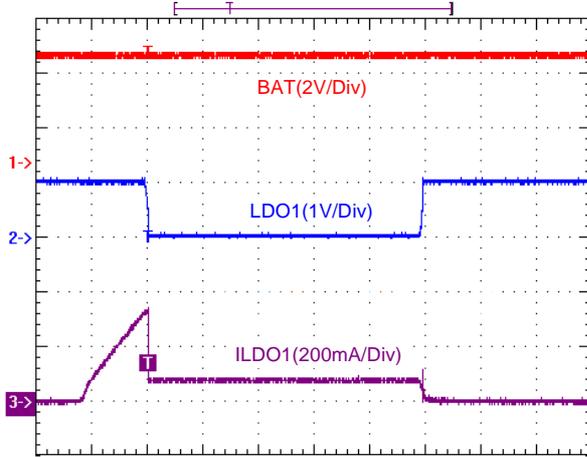
**BUCK4 Steady State Waveform**



2µs/Div  
BAT = 3.8V, Load = 1A

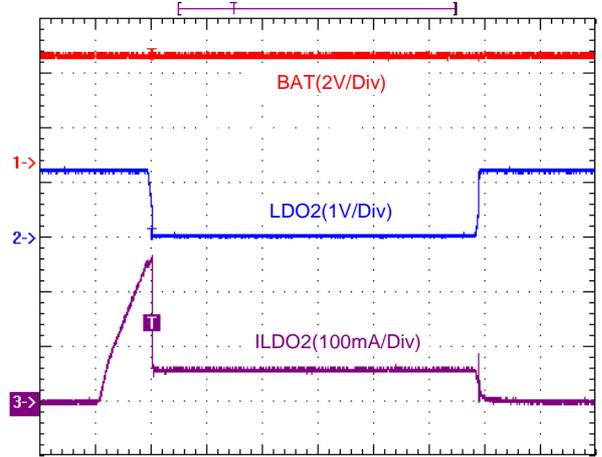
**Typical Operation Characteristics**

**LDO1 Current Limit Waveforms**



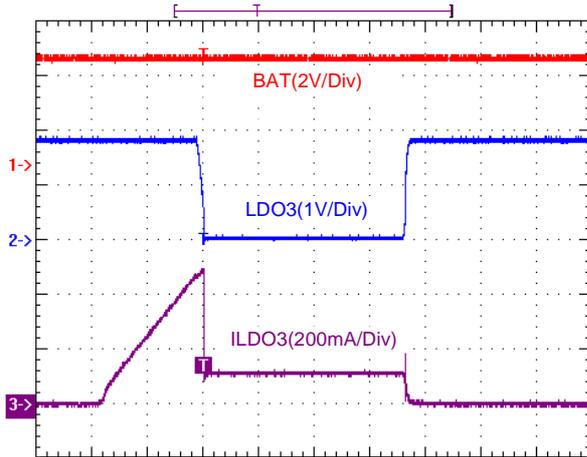
1ms/Div  
BAT = 3.8V

**LDO2 Current Limit Waveforms**



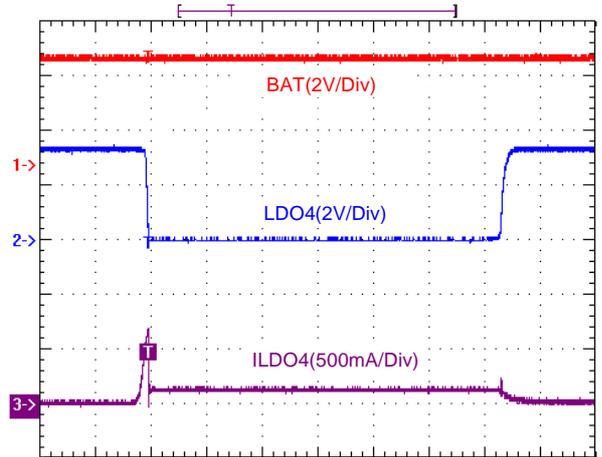
1ms/Div  
BAT = 3.8V

**LDO3 Current Limit Waveforms**



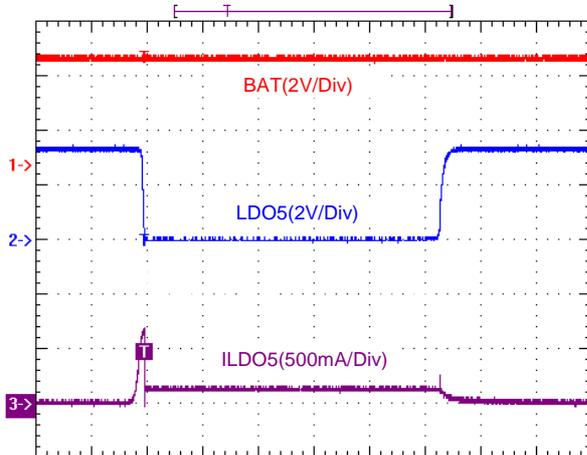
1ms/Div  
BAT = 3.8V

**LDO4 Current Limit Waveforms**



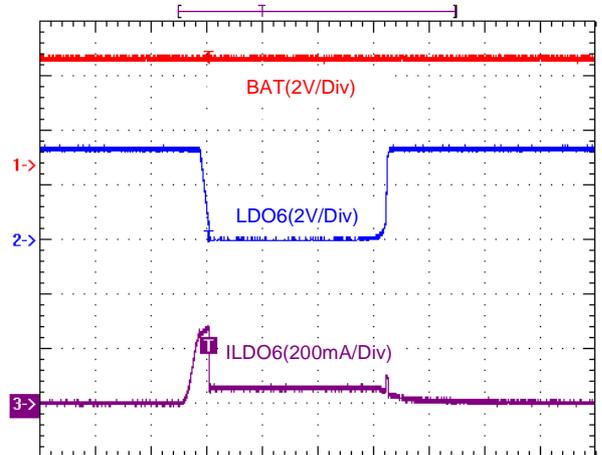
1ms/Div  
BAT = 3.8V

**LDO5 Current Limit Waveforms**



1ms/Div  
BAT = 3.8V

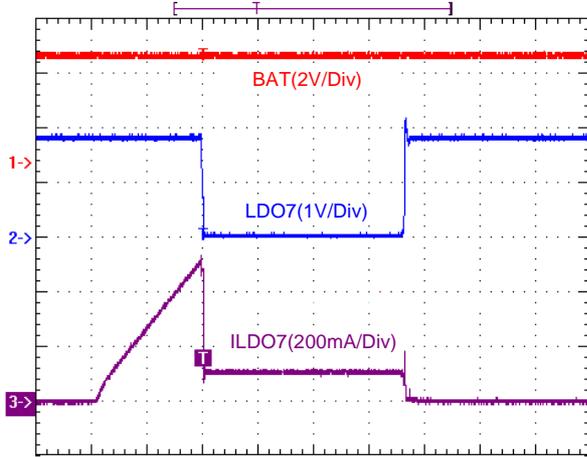
**LDO6 Current Limit Waveforms**



1ms/Div  
BAT = 3.8V

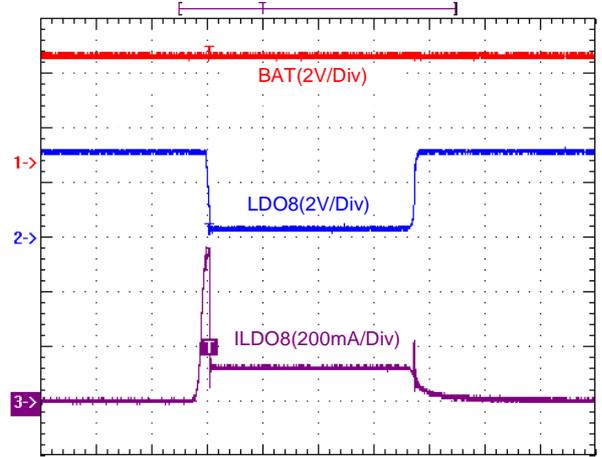
**Typical Operation Characteristics**

**LDO7 Current Limit Waveforms**



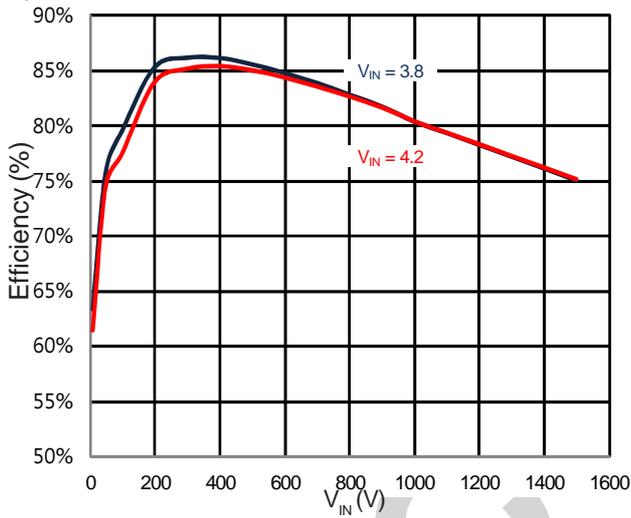
1ms/Div  
BAT = 3.8V

**LDO8 Current Limit Waveforms**

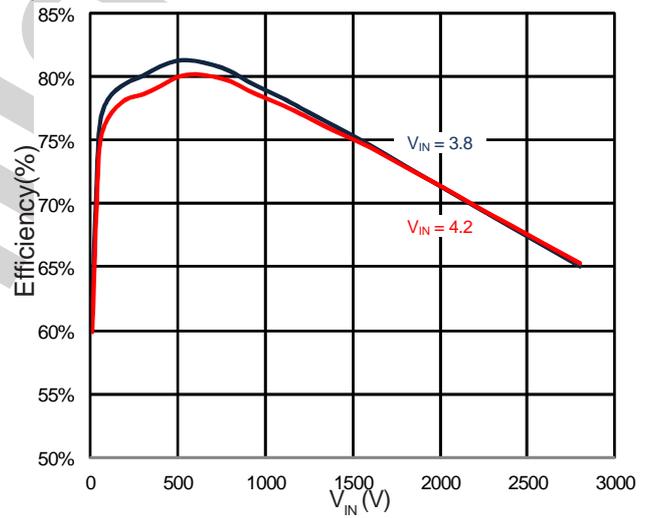


1ms/Div  
BAT = 3.8V

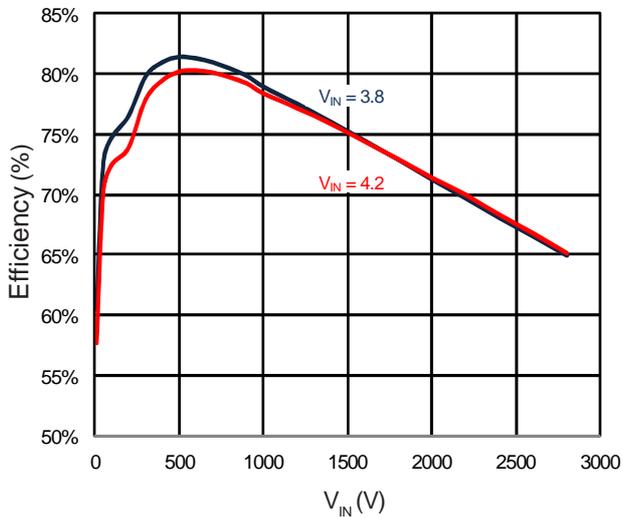
**BUCK1 Efficiency**



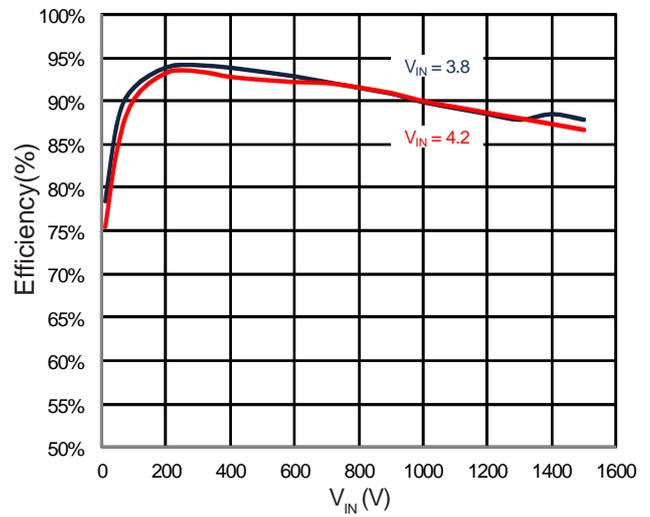
**BUCK2 Efficiency**



**BUCK3 Efficiency**



**BUCK4 Efficiency**



Application Information

**BUCK's: Output Inductor Selection**

Output inductor selection is usually based on the considerations of inductance, rated current value, size requirements and DC resistance (DCR). The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents. Higher input voltage or output voltage also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is  $\Delta I_L = 20\%$  of average load. For most applications, the value of the inductor will fall in the range of 1uH to 10uH.

$$\Delta I_L = \frac{1}{f_{SW} \times L} \times V_O \times \left[ 1 - \frac{V_O}{V_I} \right]$$

where  $\Delta I_L$  = ripple current in the inductor,  $f_{SW}$  = operating frequency,  $L$  = inductor,  $V_O$  = output voltage, and  $V_I$  = input voltage.

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

**BUCK's : Output Capacitor Selection**

The uP1720P is specifically designed to operate with minimum 10uF X5R or X7R ceramic capacitor. The value can be increased to improve load/line transient performance. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise. The ESR of the output capacitor determines the output ripple voltage and the initial voltage drop following a high slew rate load transient edge. The output ripple voltage can be calculated as:

$$\Delta V_O = \Delta I_L \times \left[ ESR + \frac{1}{8 \times f_{SW} \times C_O} \right]$$

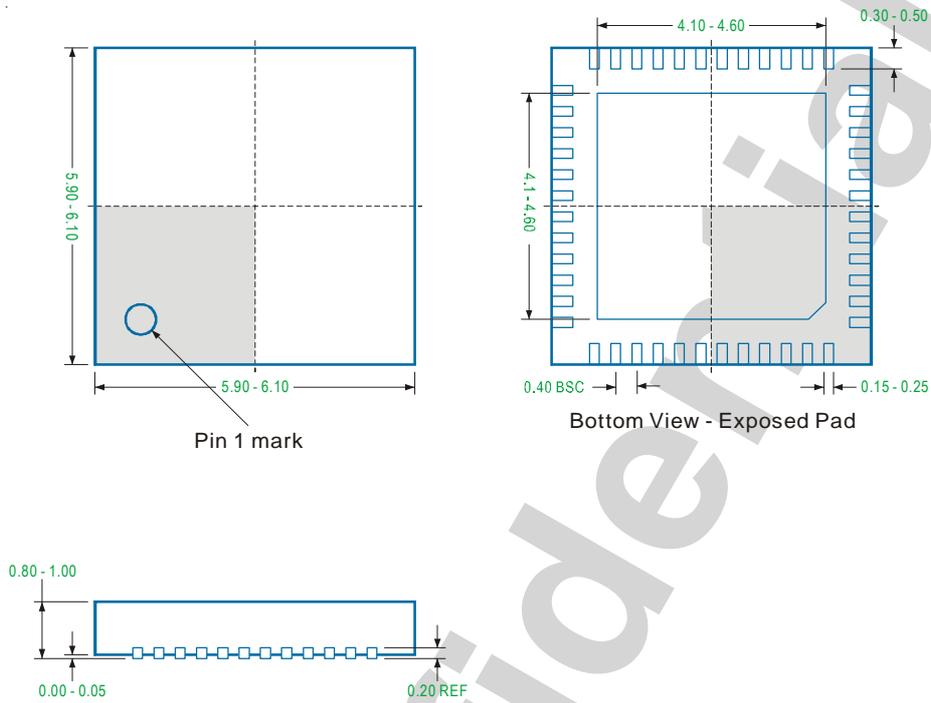
where  $\Delta V_O$  = output voltage ripple,  $\Delta I_L$  = ripple current in the inductor,  $f_{SW}$  = operating frequency, and  $C_O$  = output capacitance.

The ceramic capacitor with low ESR value provides the low output ripple and low size profile. Connect 10uF~22uF ceramic capacitor at output terminal for good performance and place the input and output capacitors as close as possible to the device.

**LDO's: Input / Output Capacitors**

The uP6636 is designed and optimized to work with low value, low-cost ceramic capacitors in space saving and performance consideration. A minimum 1uF capacitor is required from-input-to-ground to provide stability. Input capacitors greater than 1uF offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection ratio (PSRR). Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for CIN. Typical output capacitor values for maximum output current conditions range from 1uF to 10uF. Larger capacitors are recommended for applications expecting low output noise and optimum power supply ripple rejection characteristics. Place the capacitors physically as close as possible to the device with wide and direct PCB traces. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors loss capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U or Y5V dielectric capacitors loss their capacitance by 50% and 60% respectively over their operating temperature ranges.

VQFN 6x6-48L



**Note**

**1. Package Outline Unit Description:**

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP. Typical. Provided as a general value. This value is not a device specification.

**2. Dimensions in Millimeters.**

**3. Drawing not to scale.**

**4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.**

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