

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB 84256-10/10L/10LL
MB 84256-12/12L/12LL
MB 84256-15/15L/15LL

T-46-23-14

August 1988
Edition 2.0

256K-BIT (32,768 x 8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

The Fujitsu MB 84256 is a 32,768-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volts power supply is required.

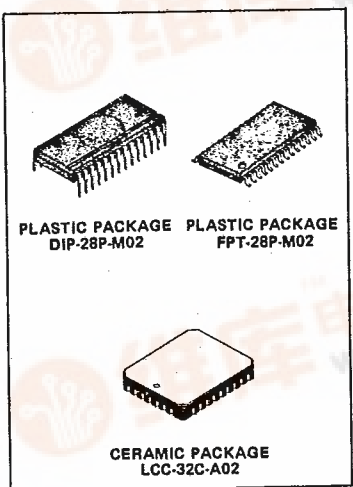
The MB 84256 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 32,768 x 8 bits
- Fast access time: 100 ns max. (MB 84256-10/10L/10LL)
120 ns max. (MB 84256-12/12L/12LL)
150 ns max. (MB 84256-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby:
 - CMOS level: 5.5 mW max. (MB 84256-10/12/15)
0.55 mW max. (MB 84256-10L/10LL/12L/12LL/
15L/15LL)
 - TTL level: 16.5 mW max. (MB 84256-10/10L/10LL/12/12L/12LL/
15/15L/15LL)
- Data retention: 2.0V
- Standard 28-pin DIP (600 mil) (Suffix: -P)
- Standard 28-pin Bend-type Plastic Flat Package (450 mil) (Suffix: -PF)
- Standard 32-pad LCC (Suffix: -CV)

ABSOLUTE MAXIMUM RATINGS (see NOTE)

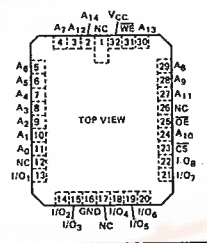
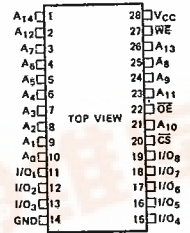
Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	V
Input Voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Output Voltage	V _{OUT}	-0.5 to V _{CC} +0.5	V
Temperature Under Bias	T _{BIAS}	-10 to +85	°C
Storage Temperature Range	CERAMIC	-65 to +150	°C
	PLASTIC		

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

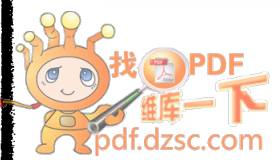


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PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

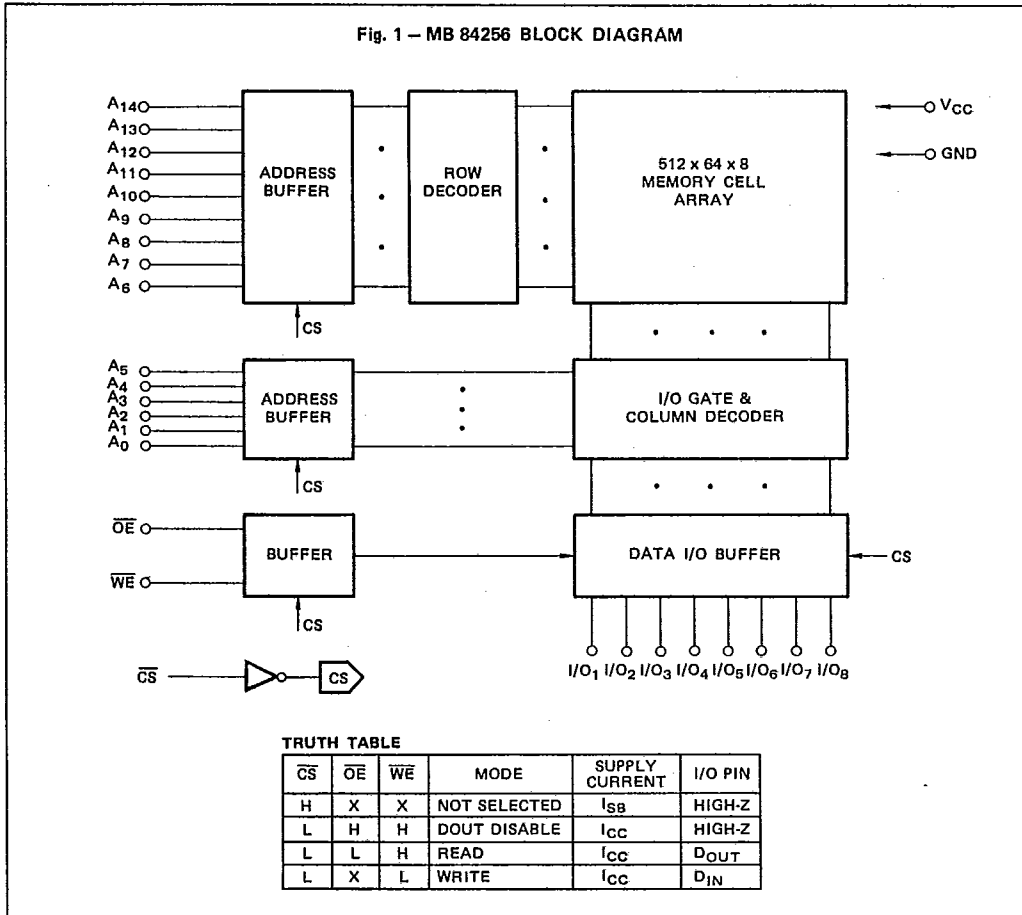


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CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (V _{I/O} = 0V)	C _{I/O}			8	pF
Input Capacitance (V _{IN} = 0V)	C _{IN}			7	pF

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RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Input Low Voltage	V _{IL}	-2.0 *		0.8	V
Input High Voltage	V _{IH}	2.2		V _{CC} +0.3	V
Ambient Temperature	T _A	0		70	°C

* -2.0 V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.3 V at DC level)

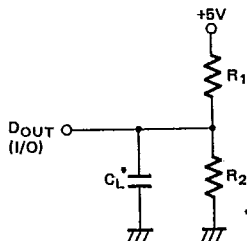
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB 84256-10/12/15		MB 84256-10L/10LL/12L/12LL/15L/15LL		Unit	Test Conditions
		Min	Max	Min	Max		
Standby Supply Current	I _{SB1}		1		0.1	mA	$\overline{CS} \geq V_{CC} - 0.2V$
	I _{SB2}		3		3		$\overline{CS} = V_{IH}$
Active Supply Current	I _{CC1}		45		45	mA	$\overline{CS} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0 mA
Operating Supply Current	I _{CC2}		70		70		Cycle = Min., Duty = 100%, I _{OUT} = 0 mA
Input Leakage Current	I _{LI}	-1	1	-1	1	μA	V _{IN} = 0V to V _{CC}
Output Leakage Current	I _{LI/O}	-1	1	-1	1	μA	V _{I/O} = 0V to V _{CC} , $\overline{CS} = V_{IH}$, OE = V _{IH} or WE = V _{IL}
Output High Voltage	V _{OH}	2.4		2.4		V	I _{OH} = -1.0 mA
Output Low Voltage	V _{OL}		0.4		0.4	V	I _{OL} = 2.1 mA

Note: All voltages are referenced to GND

Fig. 2 - AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load

* Including Jig and stray capacitance

	R ₁	R ₂	C _L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t _{CLZ} , t _{OLZ} , t _{CHZ} , t _{OHZ} , t _{WLZ} and t _{WHZ}
Load II	1.8KΩ	990Ω	5pF	t _{CLZ} , t _{OLZ} , t _{CHZ} , t _{OHZ} , t _{WLZ} and t _{WHZ}

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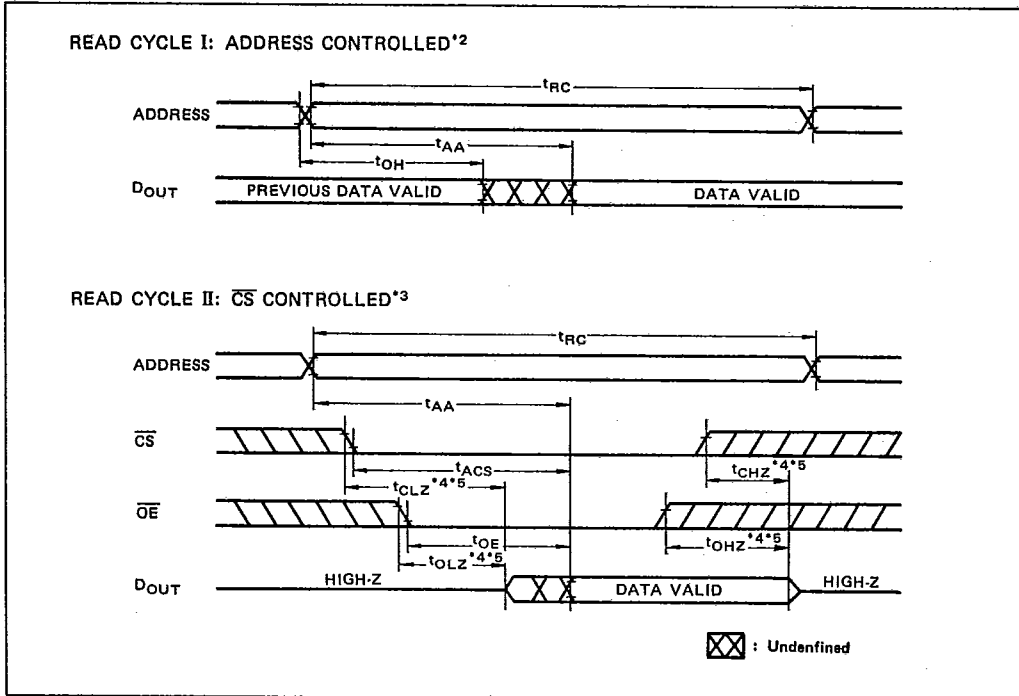
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time*2	t_{AA}		100		120		150	ns
\overline{CS} Access Time*3	t_{ACS}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		40		50		60	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Select to Output Low-Z*4*5	t_{CLZ}	10		10		10		ns
Output Enable to Output Low-Z*4*5	t_{OLZ}	5		5		5		ns
Chip Select to Output High-Z*4*5	t_{CHZ}		40		40		50	ns
Output Enable to Output High-Z*4*5	t_{OHZ}		40		40		50	ns

READ CYCLE TIMING DIAGRAM *1



- Note:**
- *1 \overline{WE} is high for Read cycle.
 - *2 Device is continuously selected, $\overline{CS} = \overline{OE} = V_{IL}$.
 - *3 Address valid prior to or coincident with \overline{CS} transition low.
 - *4 Transition is measured at the point of $\pm 500mV$ from steady state voltage.
 - *5 This parameter is specified with Load II in Fig. 2.

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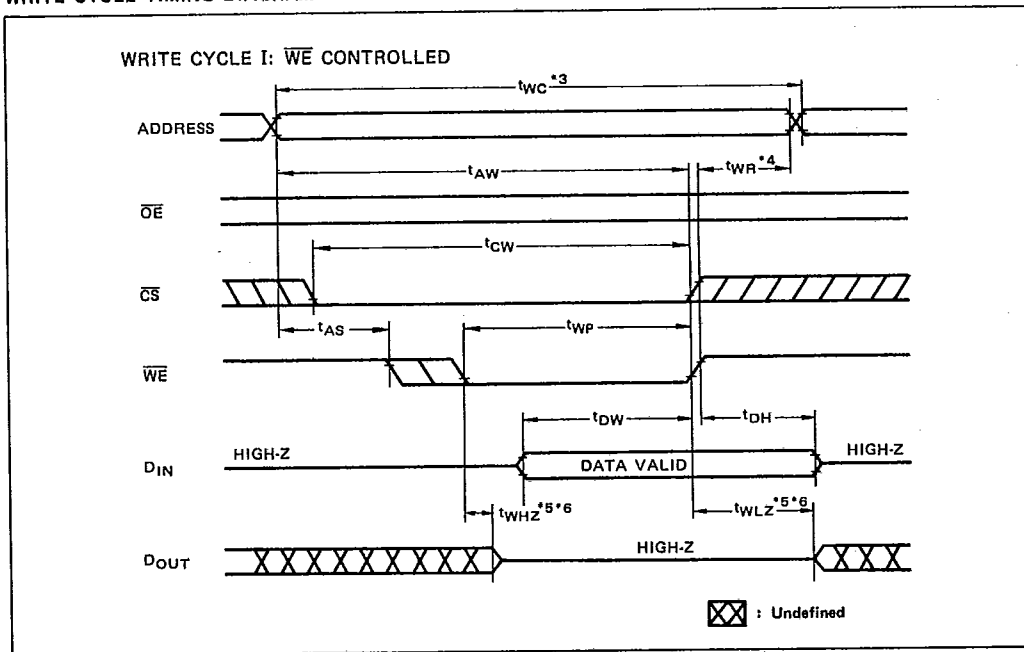


WRITE CYCLE*1*2

Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	100		120		150		ns
Address Valid to End of Write	t_{AW}	80		85		100		ns
Chip Select to End of Write	t_{CW}	80		85		100		ns
Data Valid to End of Write	t_{DW}	40		45		50		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time*4	t_{WR}	5		5		5		ns
\overline{WE} to Output Low-Z*5*6	t_{WLZ}	5		5		5		ns
\overline{WE} to Output High-Z*5*6	t_{WHZ}		40		40		50	ns



WRITE CYCLE TIMING DIAGRAM*1*2



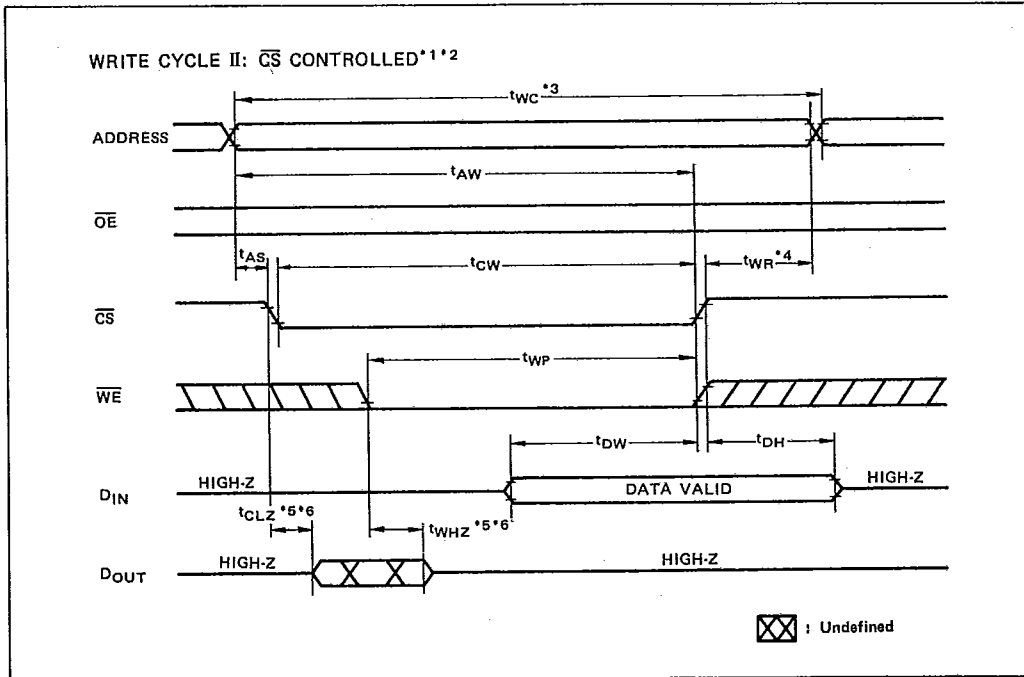
- Note: *1 If \overline{OE} , \overline{CS} are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 *2 If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in high impedance state.
 *3 All write cycle are determined form last address transition to the first address transition of the next address.
 *4 t_{WR} is defined from the end point of WRITE Mode.
 *5 Transition is measured at the point of $\pm 500mV$ from steady state voltage.
 *6 This parameter is specified with Load II in Fig. 2.

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 MB 84256-15 15L/15LL

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- Note:
- *1 If \overline{OE} , \overline{CS} are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - *2 If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in high impedance state.
 - *3 All write cycle are determined from last address transition to the first address transition of the next address.
 - *4 t_{WR} is defined from the end point of WRITE Mode.
 - *5 Transition is measured at the point of $\pm 500mV$ from steady state voltage.
 - *6 This parameter is specified with Load II in Fig. 2.

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DATA RETENTION CHARACTERISTICS

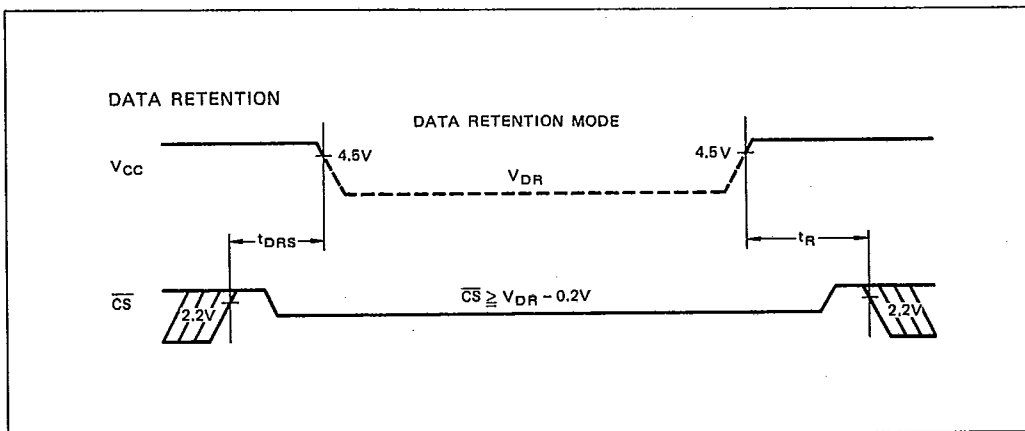
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Data Retention Supply Voltage*1	V_{DR}	2.0	5.5	V
Data Retention*2 Supply Current	Standard		1	mA
	L-Version		50	μ A
	LL-Version*3		5	μ A
Data Retention Setup Time	t_{DRS}	0		ns
Operation Recovery Time	t_R	t_{RC}		ns

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Note: *1 $\overline{CS} \geq V_{DR} - 0.2V$
 *2 $V_{DR} = 3.0V, \overline{CS} \geq V_{DR} - 0.2V$
 *3 $V_{DR} = 3.0V, T_A = 40^\circ C$

DATA RETENTION TIMING

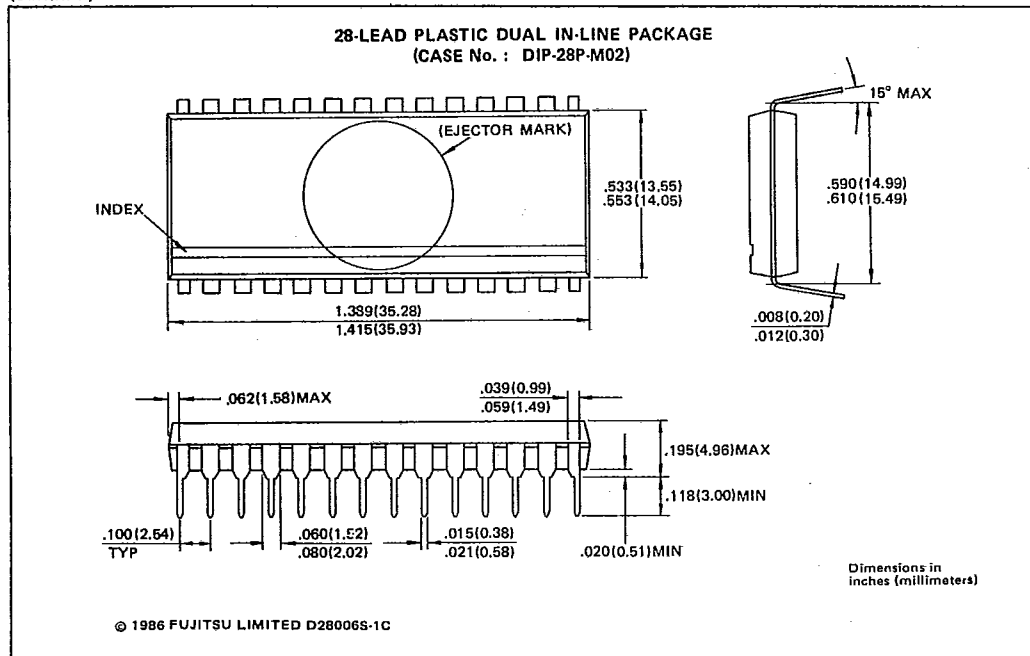


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PACKAGE DIMENSIONS

(Suffix: P)



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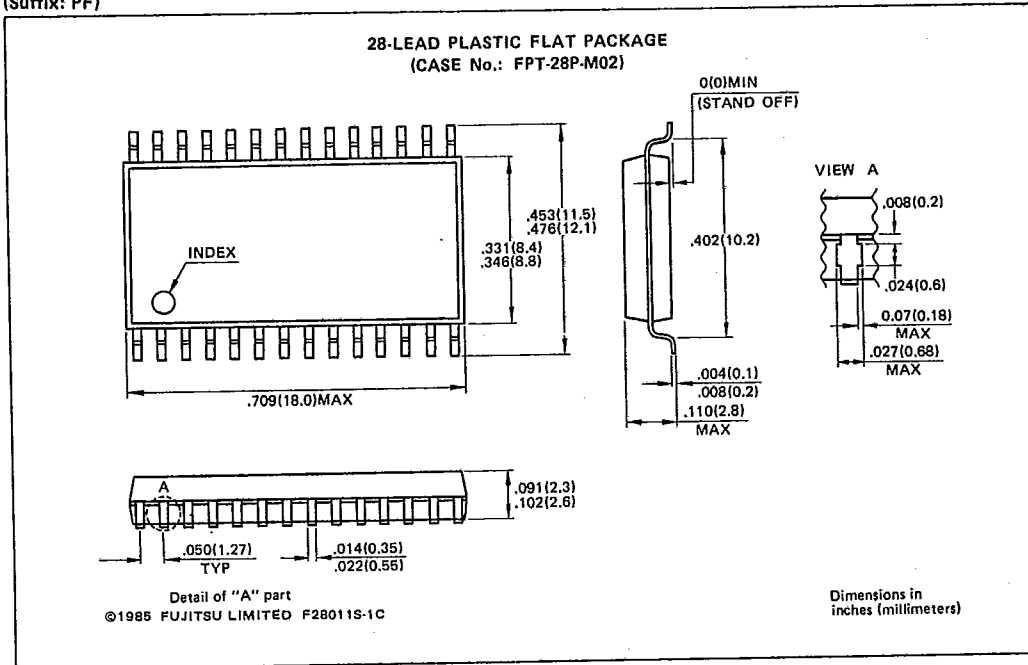
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PACKAGE DIMENSIONS

(Suffix: PF)



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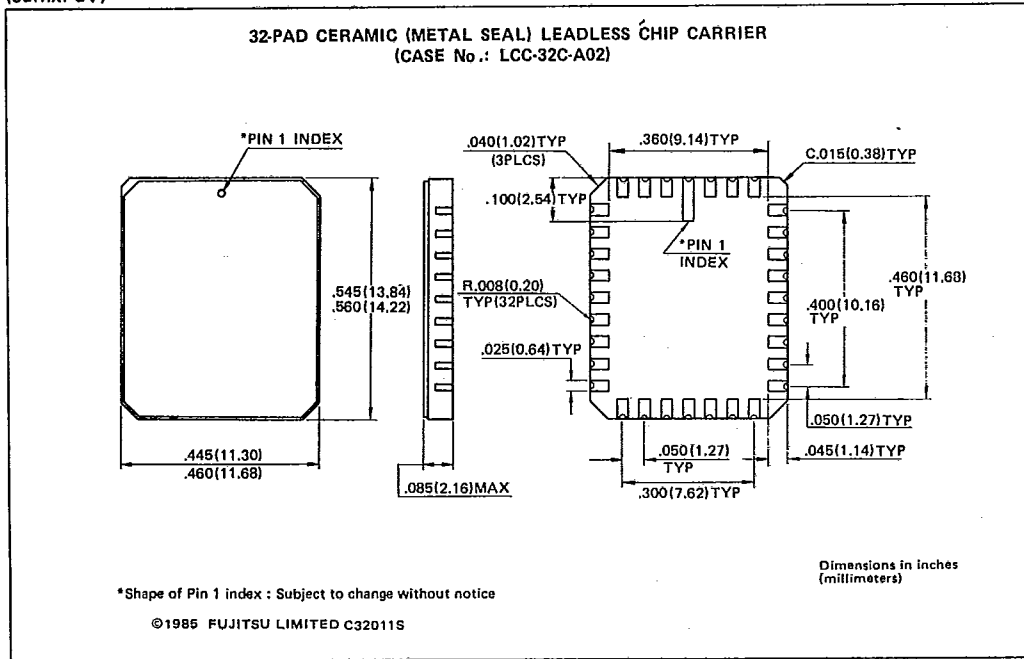
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PACKAGE DIMENSIONS

(Suffix: CV)



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