

TOSHIBA POWER MOS FET MODULE SILICON N & P CHANNEL MOS TYPE (L<sup>2</sup>-π-MOSV 4 IN 1)

# MP4212

HIGH POWER HIGH SPEED SWITCHING APPLICATIONS  
H-SWITCH DRIVER

- 4 V Gate Drive
- Small Package by Full Molding (SIP 10 Pin)
- High Drain Power Dissipation (4 Devices Operation)  
: P<sub>T</sub> = 4 W (T<sub>a</sub> = 25°C)
- Low Drain-Source ON Resistance  
: R<sub>DS(ON)</sub> = 120 mΩ (typ.) (N-ch)  
160 mΩ (typ.) (P-ch)
- High Forward Transfer Admittance  
: |Y<sub>fs</sub>| = 5.0 S (typ.) (Nch)  
4.0 S (typ.) (Pch)
- Low Leakage Current: I<sub>GSS</sub> = ±10 μA (max.) (V<sub>GS</sub> = ±16 V)  
I<sub>DSS</sub> = 100 μA (max.) (V<sub>DS</sub> = 60 V)
- Enhancement-Mode : V<sub>th</sub> = 0.8~2.0 V (V<sub>DS</sub> = 10 V, I<sub>D</sub> = 1 mA)

MAXIMUM RATINGS (T<sub>a</sub> = 25°C)

CHARACTERISTIC	SYMBOL	RATING		UNIT
		Nch	Pch	
Drain-Source Voltage	V <sub>DSS</sub>	60	-60	V
Drain-Gate Voltage (R <sub>GS</sub> = 20 kΩ)	V <sub>DGR</sub>	60	-60	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	±20	V
Drain Current	DC	I <sub>D</sub>	5	A
	Pulse	I <sub>DP</sub>	20	
Drain Power Dissipation (1 Device Operation, T <sub>a</sub> = 25°C)	P <sub>D</sub>	2.0		W
Drain Power Dissipation (4 Devices Operation, T <sub>a</sub> = 25°C)	P <sub>DT</sub>	4.0		W
Single Pulse Avalanche Energy*	E <sub>AS</sub>	129	273	mJ
Avalanche Current	I <sub>AR</sub>	5	-5	A
Repetitive Avalanche Energy**	1 Device Operation	E <sub>AR</sub>	0.2	mJ
	4 Devices Operation	E <sub>ART</sub>	0.4	
Channel Temperature	T <sub>ch</sub>	150		°C
Storage Temperature Range	T <sub>stg</sub>	-55~150		°C

Note ;

\* Avalanche energy (single pulse) applied condition

Nch : V<sub>DD</sub> = 25 V, Starting T<sub>ch</sub> = 25°C, L = 7 mH, R<sub>G</sub> = 25 Ω, I<sub>AR</sub> = 5 A

Pch : V<sub>DD</sub> = -25 V, Starting T<sub>ch</sub> = 25°C, L = 14.84 mH, R<sub>G</sub> = 25 Ω, I<sub>AR</sub> = -5 A

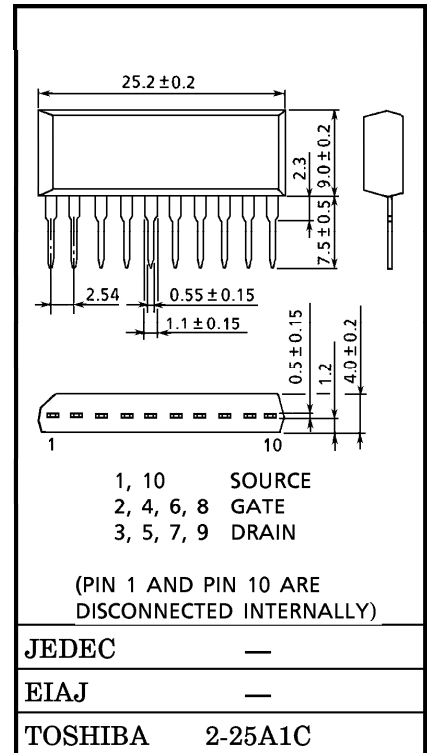
\*\* Repetitive rating; Pulse Width Limited by maximum channel temperature.

**This transistor is an electrostatic sensitive device. Please handle with caution.**

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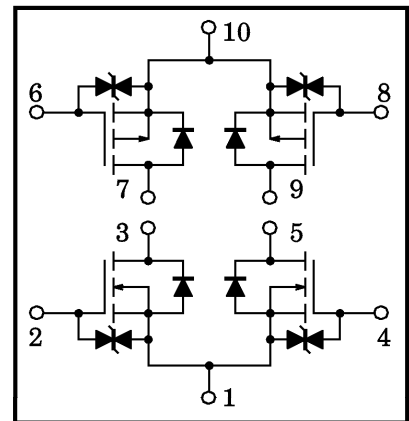
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INDUSTRIAL APPLICATIONS  
Unit in mm



Weight : 2.1 g (typ.)

ARRAY CONFIGURATION



**THERMAL CHARACTERISTICS**

CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance of Channel to Ambient (4 Devices Operation, Ta = 25°C)	$\Sigma R_{th} (ch-a)$	31.2	°C/W
Maximum Lead Temperature for Soldering Purposes (3.2 mm from Case for t = 10 s)	T <sub>L</sub>	260	°C

**ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Nch MOS FET)**

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V	—	—	±10	μA
Drain Cut-off Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	—	—	100	μA
Drain-Source Breakdown Voltage	V (BR) DSS	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	60	—	—	V
Gate Threshold Voltage	V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	0.8	—	2.0	V
Drain-Source ON Resistance	R <sub>DS (ON)</sub>	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 2.5 A	—	0.21	0.32	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A	—	0.12	0.16	
Forward Transfer Admittance	Y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.5 A	3.0	5.0	—	S
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	370	—	pF
Reverse Transfer Capacitance	C <sub>rss</sub>		—	60	—	
Output Capacitance	C <sub>oss</sub>		—	180	—	
Switching Time	Rise Time	t <sub>r</sub>		—	18	ns
	Turn-on Time	t <sub>on</sub>		—	25	
	Fall Time	t <sub>f</sub>		—	55	
	Turn-off Time	t <sub>off</sub>		V <sub>IN</sub> : t <sub>r</sub> , t <sub>f</sub> < 5 ns, Duty ≤ 1%, t <sub>w</sub> = 10 μs	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q <sub>g</sub>	V <sub>DD</sub> ≐ 48 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	—	12	—	nC
Gate-Source Charge	Q <sub>gs</sub>		—	8	—	
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>		—	4	—	

**SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	I <sub>DR</sub>	—	—	—	5	A
Pulse Drain Reverse Current	I <sub>DRP</sub>	—	—	—	20	A
Diode Forward Voltage	V <sub>DSF</sub>	I <sub>DR</sub> = 5 A, V <sub>GS</sub> = 0 V	—	—	-1.7	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>DR</sub> = 5 A, V <sub>GS</sub> = 0 V	—	70	—	ns
Reverse Recovery Charge	Q <sub>rr</sub>	dI <sub>DR</sub> / dt = 50 A / μs	—	0.1	—	μC

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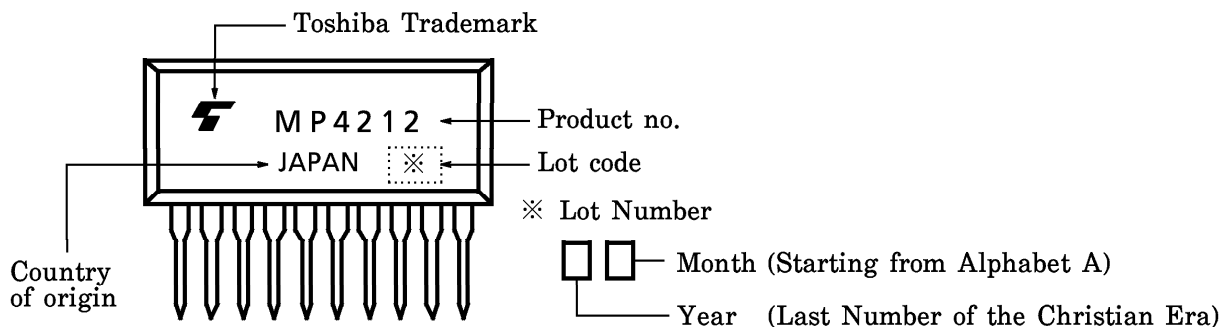
ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Pch MOS FET)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain Cut-off Current		$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$	—	—	-100	$\mu\text{A}$
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-60	—	—	V
Gate Threshold Voltage		$V_{th}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-0.8	—	-2.0	V
Drain-Source ON Resistance		$R_{DS(ON)}$	$V_{GS} = -4\text{ V}, I_D = -2.5\text{ A}$	—	0.24	0.28	$\Omega$
			$V_{GS} = -10\text{ V}, I_D = -2.5\text{ A}$	—	0.16	0.19	
Forward Transfer Admittance		$ Y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -2.5\text{ A}$	2.0	4.0	—	S
Input Capacitance		$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	630	—	pF
Reverse Transfer Capacitance		$C_{rss}$		—	95	—	
Output Capacitance		$C_{oss}$		—	290	—	
Switching Time	Rise Time	$t_r$		—	25	—	ns
	Turn-on Time	$t_{on}$		—	45	—	
	Fall Time	$t_f$		—	55	—	
	Turn-off Time	$t_{off}$		$V_{IN} : t_r, t_f < 5\text{ ns}$ $Duty \leq 1\%, t_w = 10\ \mu\text{s}$	—	200	
Total Gate Charge (Gate-Source Plus Gate-Drain)		$Q_g$	$V_{DD} \doteq -48\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -5\text{ A}$	—	22	—	nC
Gate-Source Charge		$Q_{gs}$		—	16	—	
Gate-Drain ("Miller") Charge		$Q_{gd}$		—	6	—	

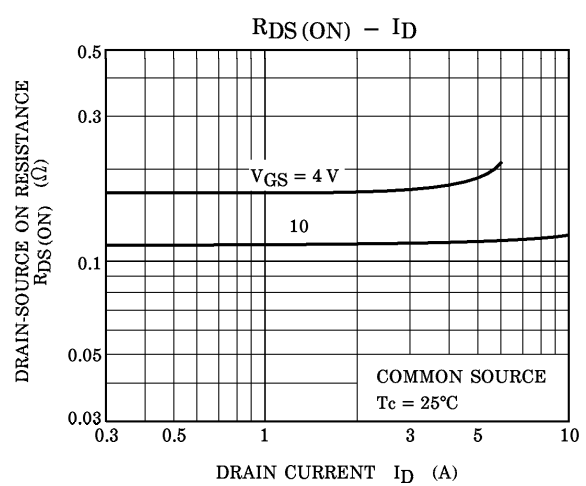
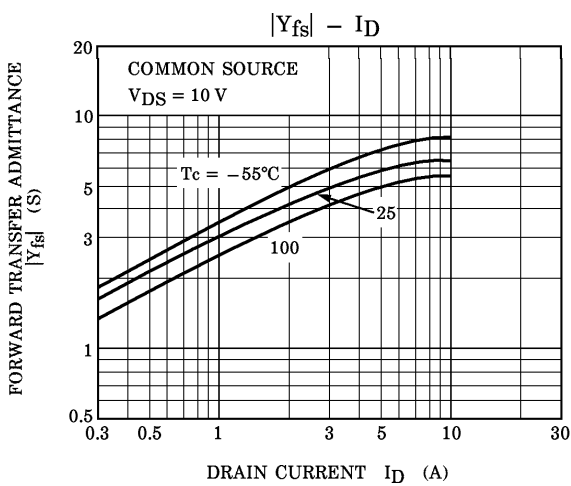
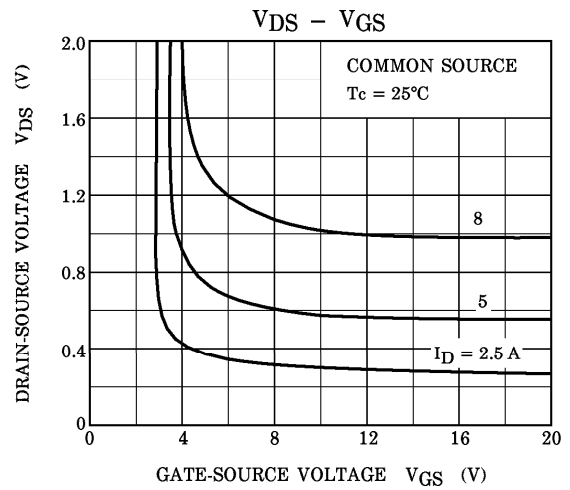
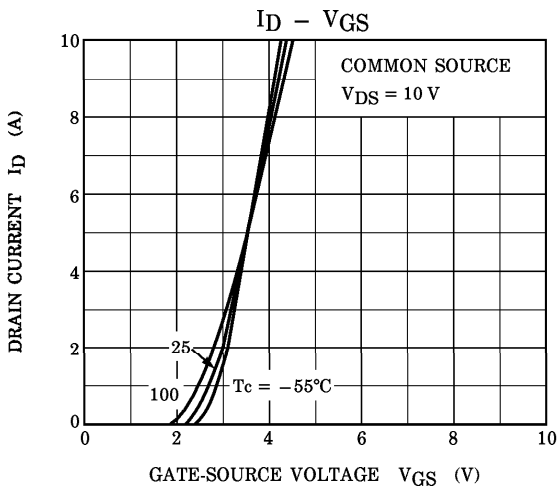
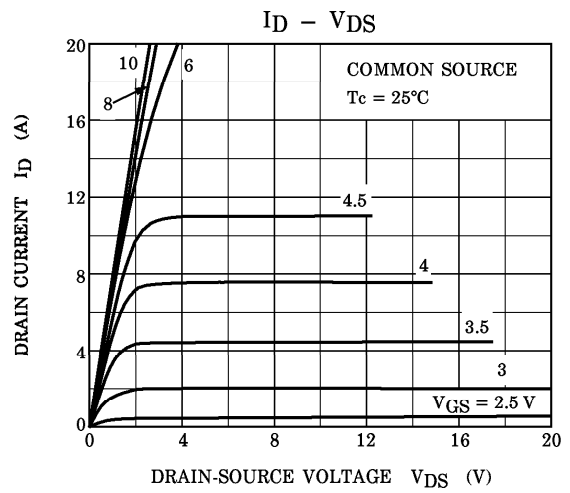
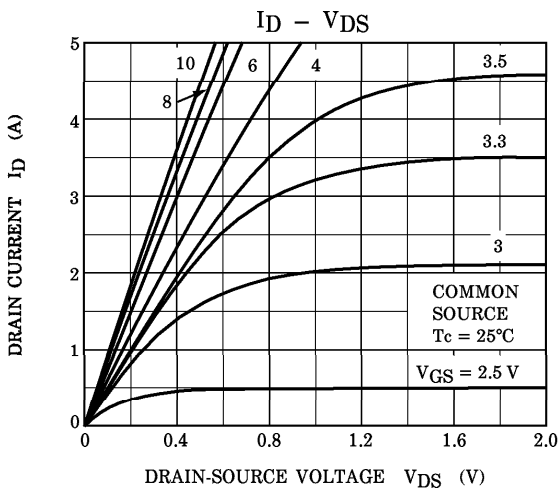
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS (Ta = 25°C)

	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	$I_{DR}$	—	—	—	-5	A
Pulse Drain Reverse Current	$I_{DRP}$	—	—	—	-20	A
Diode Forward Voltage	$V_{DSF}$	$I_{DR} = -5\text{ A}, V_{GS} = 0\text{ V}$	—	—	1.7	V
Reverse Recovery Time	$t_{rr}$	$I_{DR} = -5\text{ A}, V_{GS} = 0\text{ V}$	—	80	—	ns
Reverse Recovery Charge	$Q_{rr}$	$dI_{DR} / dt = 50\text{ A} / \mu\text{s}$	—	0.1	—	$\mu\text{C}$

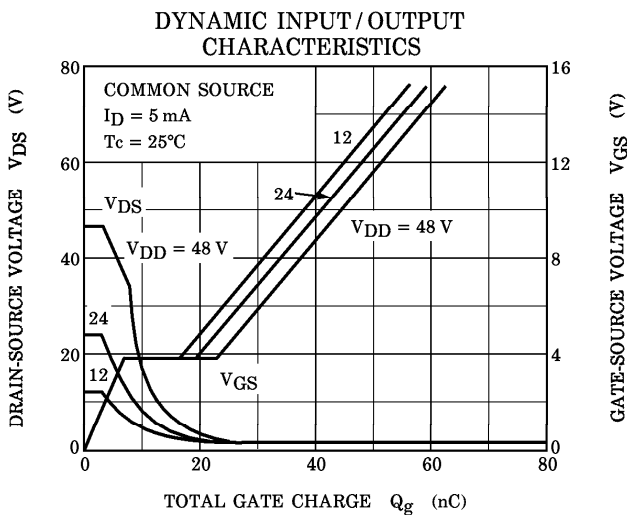
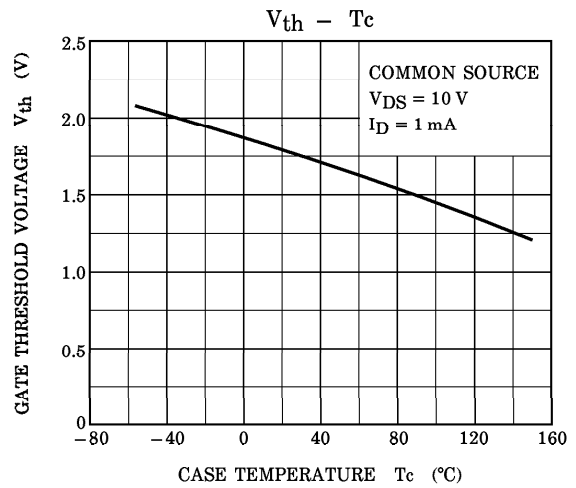
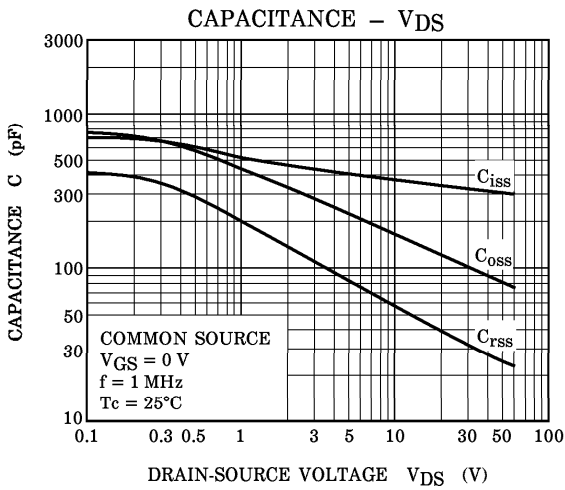
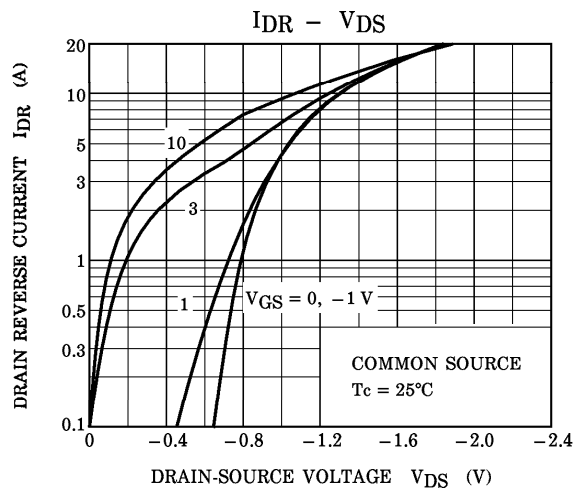
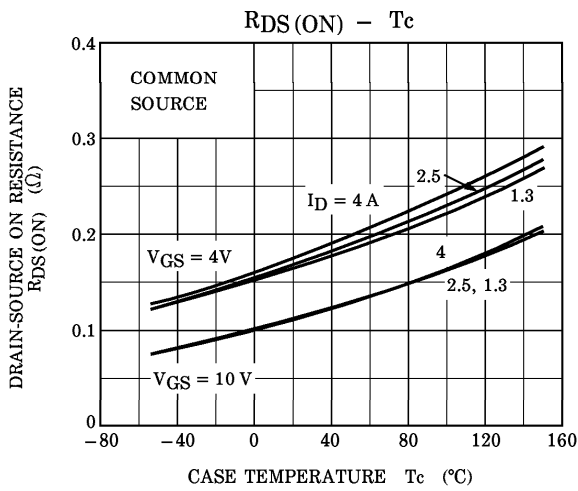
MARKING



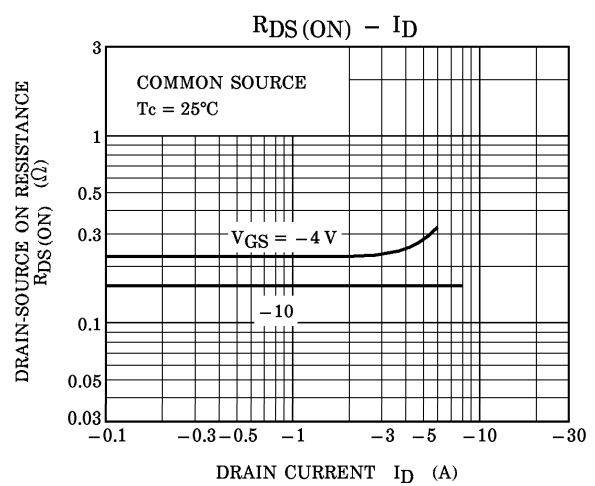
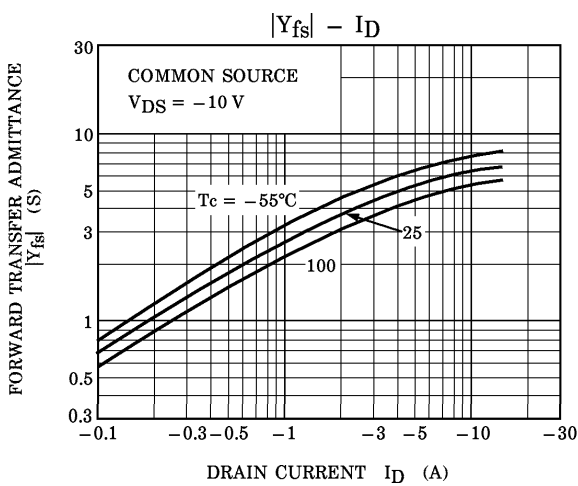
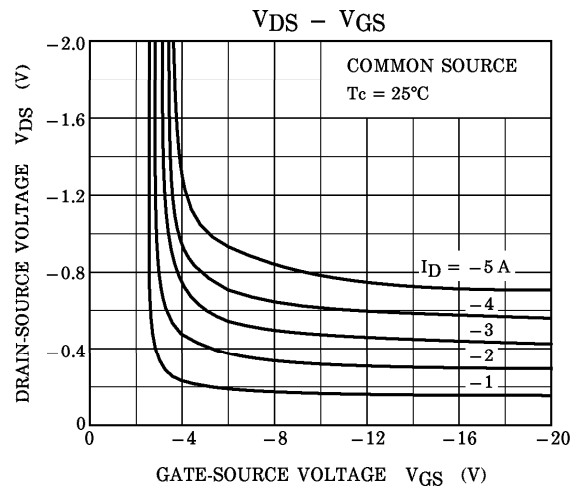
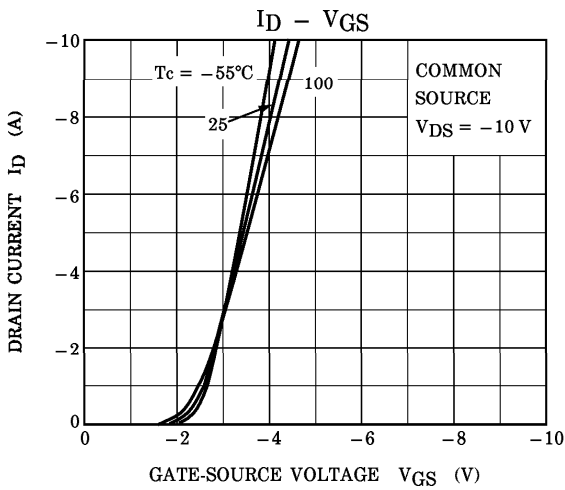
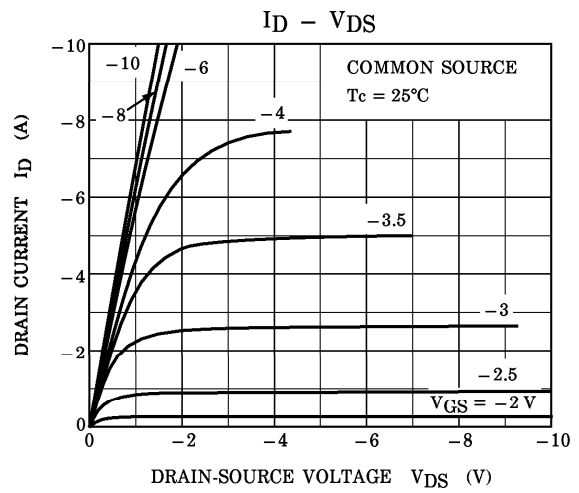
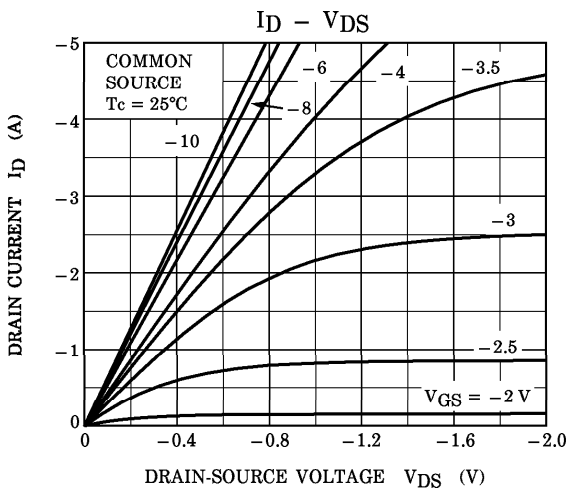
Nch MOS FET



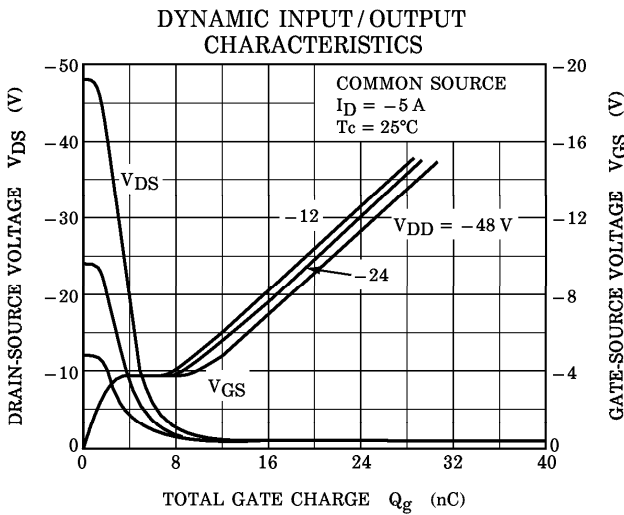
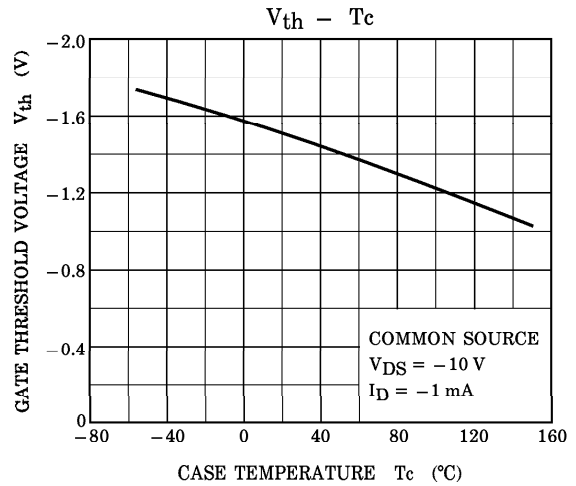
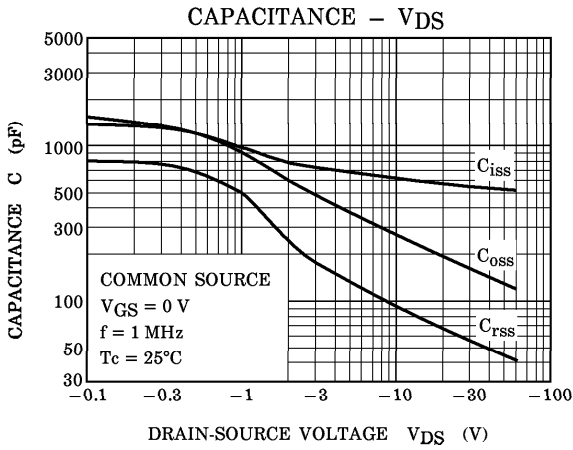
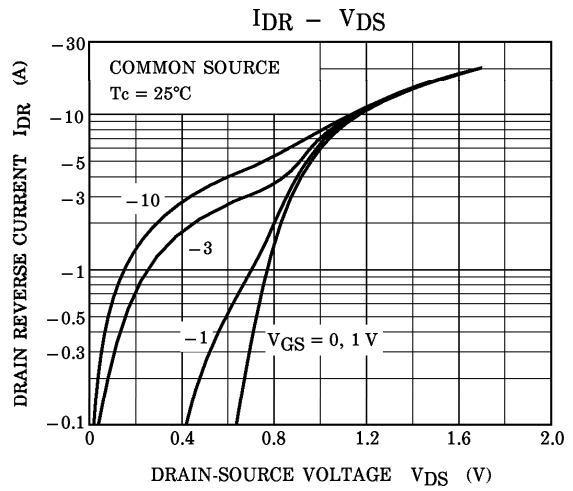
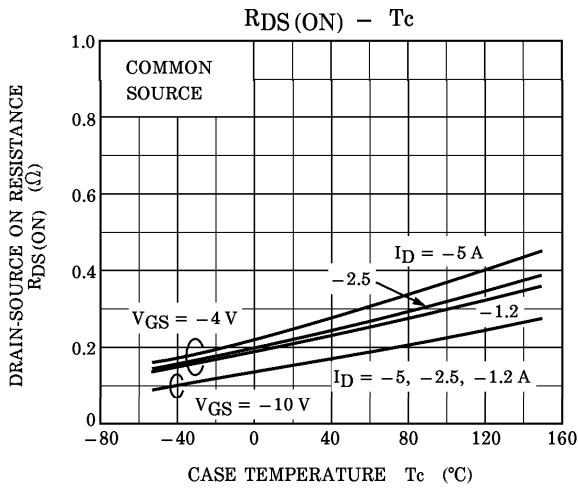
Nch MOS FET

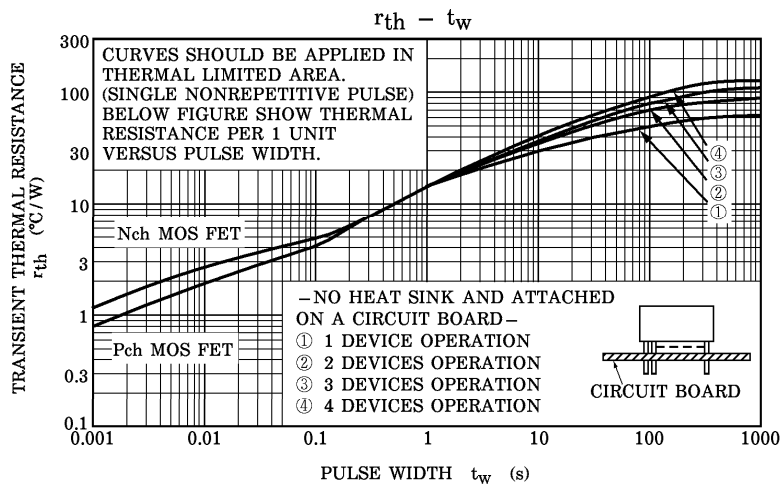
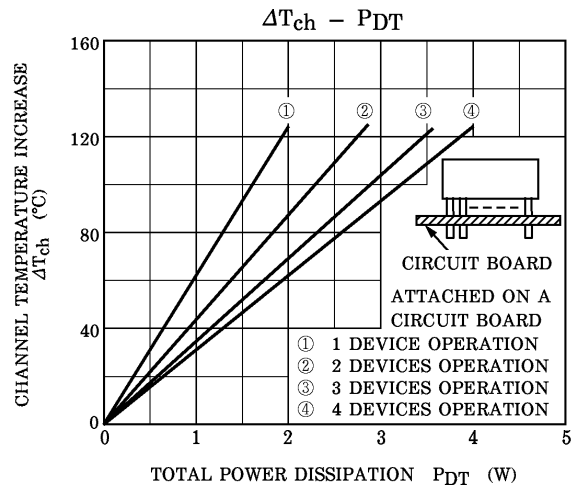
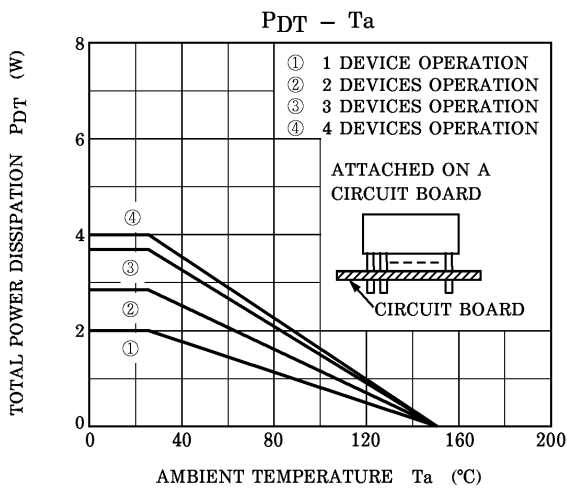


Pch MOS FET



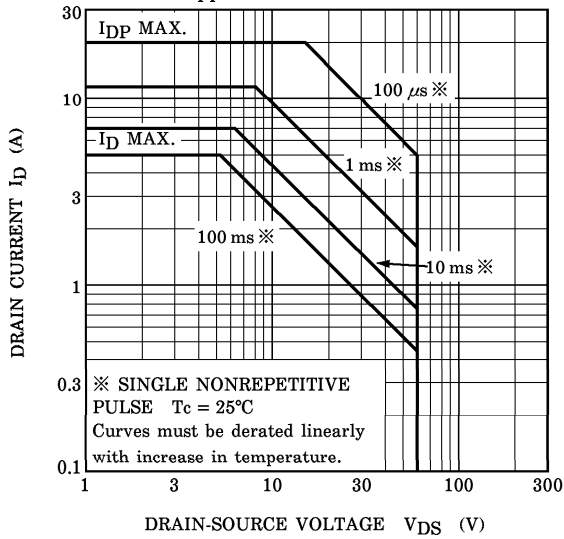
Pch MOS FET



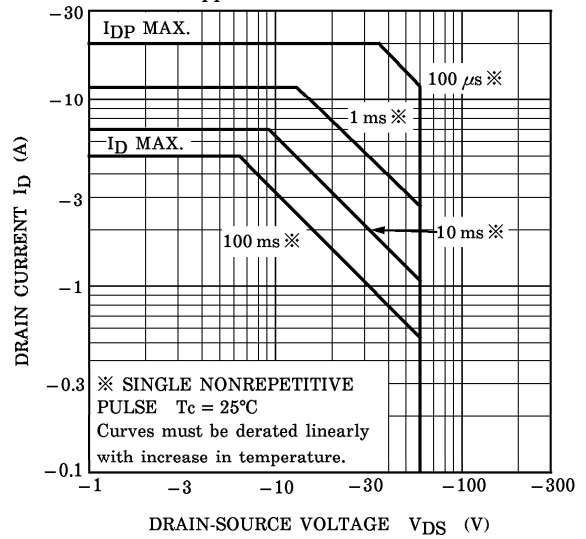




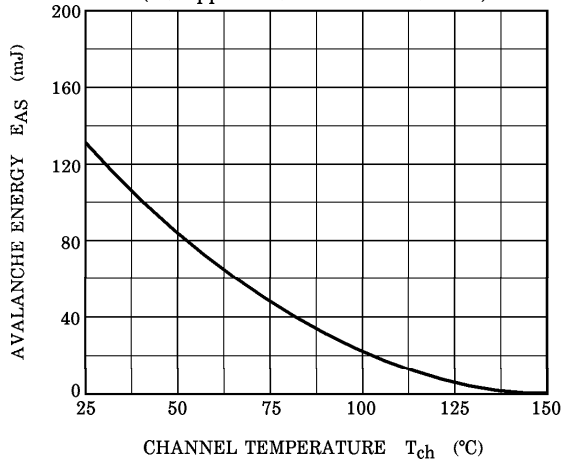
**SAFE OPERATING AREA**  
(Be applicable to Nch MOS FET)



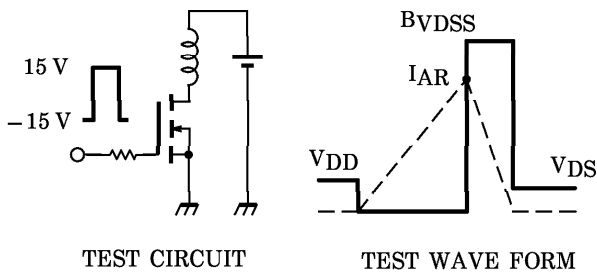
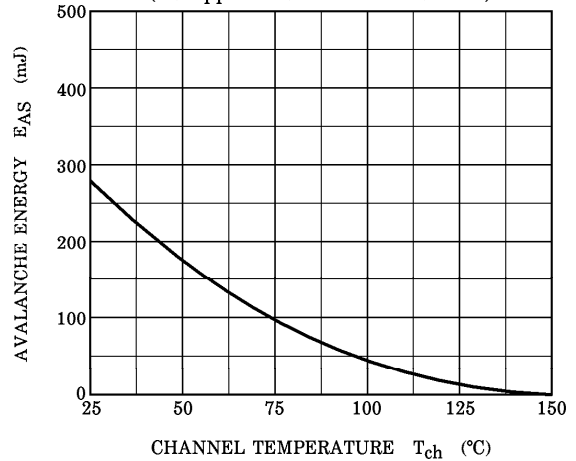
**SAFE OPERATING AREA**  
(Be applicable to Pch MOS FET)



**$E_{AS} - T_{ch}$**   
(Be applicable to Nch MOS FET)

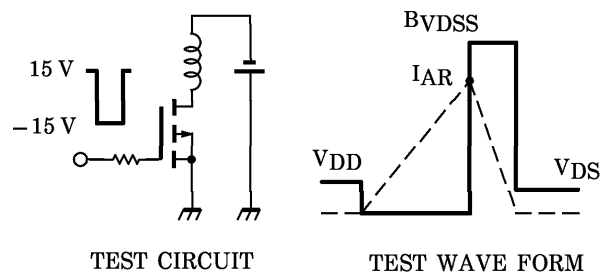


**$E_{AS} - T_{ch}$**   
(Be applicable to Pch MOS FET)



Peak  $I_{AR} = 5\text{ A}$ ,  $R_G = 25\Omega$   
 $V_{DD} = 25\text{ V}$ ,  $L = 7\text{ mH}$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \right)$$



Peak  $I_{AR} = -5\text{ A}$ ,  $R_G = 25\Omega$   
 $V_{DD} = -25\text{ V}$ ,  $L = 14.84\text{ mH}$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \right)$$