

ISL98607

High Efficiency Power Supply for Small Size Displays

The [ISL98607](#) is a high efficiency power supply for small size displays, like smart phones, requiring  $\pm$ supply rails. It integrates boost regulator, LDO, and inverting charge pump that are used to generate two output rails: +5V (default) and -5V (default). The  $\pm$ 5V output voltages can be adjusted up to  $\pm$ 5.7V with 50mV steps using the I<sup>2</sup>C interface.

The ISL98607 integrates synchronous rectification MOSFETs for the boost regulator and inverting charge pump, which maximizes conversion efficiency.

The ISL98607 integrates all compensation and feedback components, which minimizes BOM count and reduces the solution PCB size to 21mm<sup>2</sup>.

The input voltage range, high efficiency operation, and also very low shutdown current make the device ideal for use in single cell Li-ion battery operated applications.

The ISL98607 is offered in the 1.82x2.15mm WLCSP and 20 Ld 3x4mm TQFN packages, and the device is specified for operation across the -40°C to +85°C ambient temperature range.

Related Literature

For a full list of related documents, visit our website:

- [ISL98607](#) device page

Features

- Two outputs:
  - VP = +5.0V (default)
  - VN = -5.0V (default)
- 2.8V to 4.4V Input voltage range
- >85.5% Efficiency with 12mA load between VP and VN
- 21mm<sup>2</sup> Solution PCB area
- Fully integrated FETs for synchronous rectification
- Integrated compensation and feedback circuits
- I<sup>2</sup>C adjustable output voltages and settings
- Integrated VP/VN discharge resistors
- 1 $\mu$ A shutdown supply current
- Multiple package options:
  - 1.82x2.15mm, 4x5 array WLCSP with 0.4mm pitch
  - 20 Ld 3x4mm TQFN
- Pb-Free (RoHS compliant)

Applications

- TFT-LCD Smart phone displays
- Small size/handheld displays

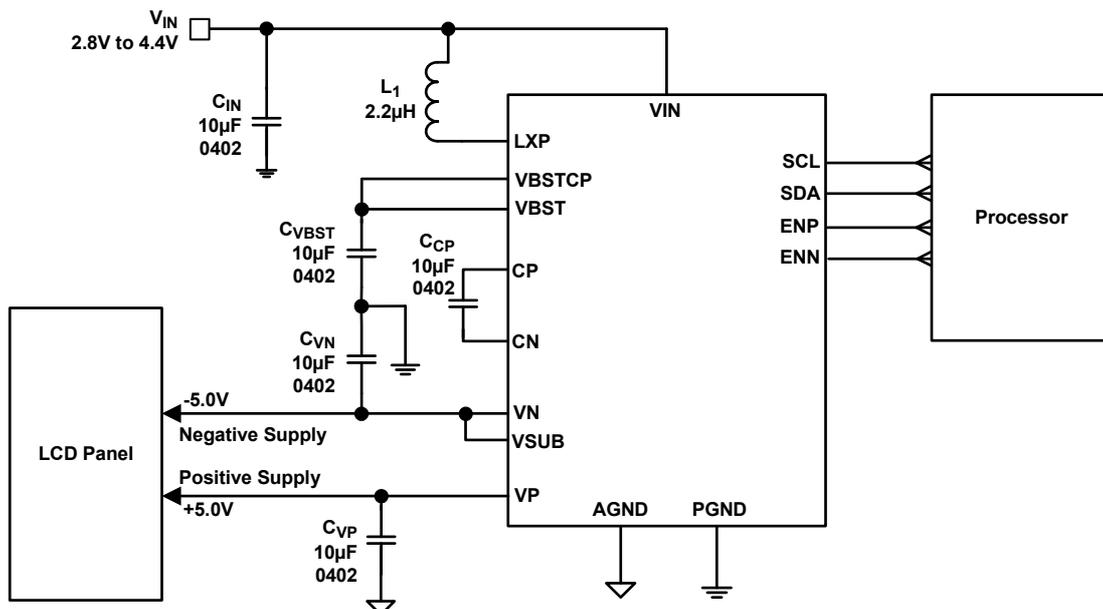


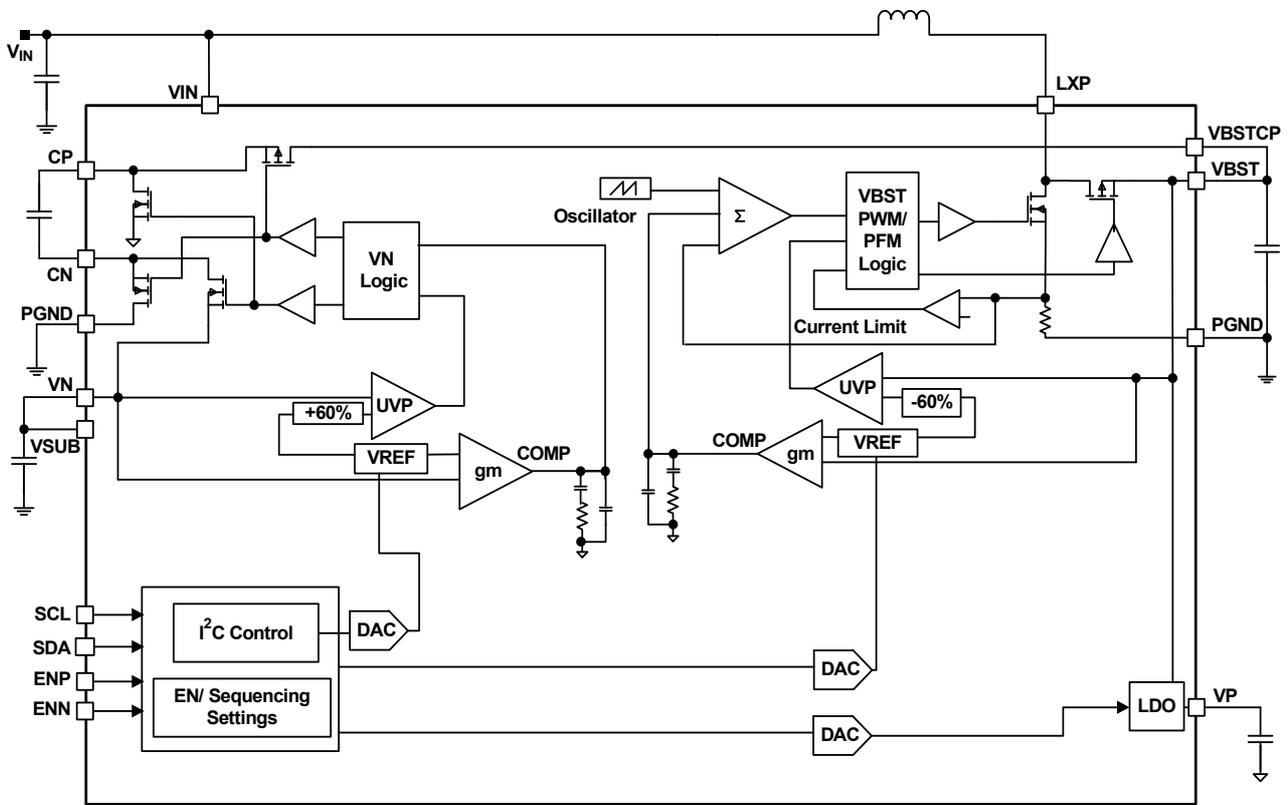
Figure 1. Typical Application Circuit: TFT-LCD Smart Phone Display

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# 1. Overview

## 1.1 Block Diagram



## 1.2 Ordering Information

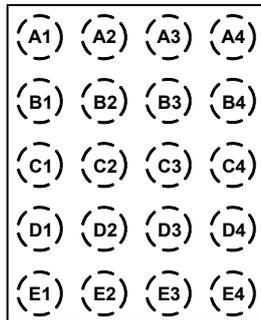
Part Number ( <a href="#">Note 4</a> )	Part Marking	Temp Range (°C)	Tape and Reel (Units) ( <a href="#">Note 1</a> )	Package (RoHS Compliant)	Pkg. Dwg. #
ISL98607EIAZ-T ( <a href="#">Note 2</a> )	607A	-40 to +85	3k	20 Ball (4x5 bump, 0.4mm pitch) WLCSP	W4x5.20E
ISL98607IRTZ-T( <a href="#">Note 3</a> )	8607	-40 to +85	6k	20 LD 3x4 TQFN	L20.3x4A
ISL98607-EVZ	ISL98607EIAZ Evaluation Board				
ISL98607IRTZ-EVZ	ISL98607IRTZ Evaluation Board				

Notes:

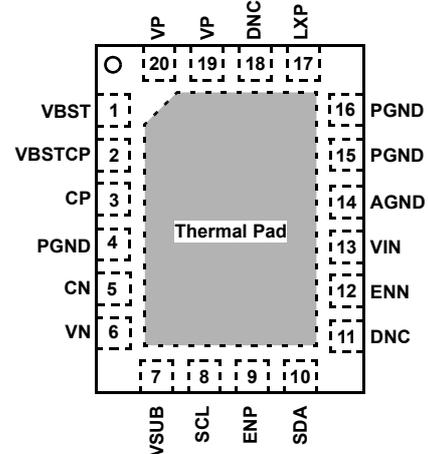
1. See [TB347](#) for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the [ISL98607](#) device page. For more information about MSL, see [TB363](#).

### 1.3 Pin Configurations

20 Bump, 4x5 ARRAY, 0.4mm Pitch WLCSP  
Top View



20 Ld 3x4 TQFN  
Top View



### 1.4 Pin Descriptions

Pin Number (WLCSP)	Pin Number (TQFN)	Pin Name	Description
A1, B1	15, 16	PGND	Power ground for the boost converter.
A2, E1	11, 18	DNC	Do not connect to external circuitry. This pin should be left floating.
A3, A4	19, 20	VP	VP Output. Connect a 10µF capacitor to ground. The VP pins must always be shorted together on the PCB.
B2	17	LXP	Switch node for boost converter. Connect an inductor between the VIN and LXP pins for boost converter operation.
B3	1	VBST	Boost Converter Output. The boost converter output supplies the power to the negative charge pump and LDO. Connect a 10µF capacitor to ground.
B4	2	VBSTCP	Charge pump input. This pin must be connected to VBST on the PCB, so that the boost regulator provides the input voltage supply for the charge pump.
C1	14	AGND	Analog ground.
C2	12	ENN	VBST and VN enable input. Note, this pin has 200kΩ (typical) pull-down to AGND.
C3	9	ENP	VBST and VP enable input. Note, this pin has 200kΩ (typical) pull-down to AGND.
C4	3	CP	Charge pump positive connection. Place a capacitor between CP and CN to create the VN voltage.
D1	13	VIN	Input Supply. Connect a 10µF capacitor to ground.
D2	10	SDA	Serial Data Connection for the I <sup>2</sup> C Interface.
D3	8	SCL	Serial Clock Connection for the I <sup>2</sup> C Interface.
D4	4	PGND	Power ground for the negative charge pump.
E2	7	VSUB	Substrate connection. VSUB must be the most negative potential on the IC, connect VSUB to VN.
E3	6	VN	Negative charge pump output. Connect a 10µF capacitor to ground. Connecting two 10µF capacitors to ground lowers the negative charge pump output voltage ripple.
E4	5	CN	Charge pump negative connection. Place a capacitor between CP and CN to generate the VN voltage.
N/A	-	Thermal Pad	Connect to ground plane on PCB to maximize the thermal performance.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VBST, VBSTCP, CP, VP to AGND	-0.3	7	V
VN, VSUB to AGND	+0.3	-7	V
VIN, SCL, SDA, ENN, ENP to AGND	-0.3	6	V
LXP to AGND	-0.3	VBST + 0.3	V
CN to AGND	VN - 0.3	PGND + 0.3	V
Maximum Average Current Out of VBST Pin		1	A
Maximum Average Current Into LXP Pin		1	A
Maximum Average Current Into CN, CP Pin		-1	A
<b>ESD Rating</b>	<b>Value</b>		<b>Unit</b>
Human Body Model (Tested per JESD22-A114)	2		kV
Machine Model (Tested per JESD22-A115)	200		V
Charged Device Model (Tested per JESD22-C101)	750		V
Latch-Up (Tested per JESD78; Class II, Level A)	100		mA

### 2.2 Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
4x5 Bump 0.4mm pitch WLCSP ( <a href="#">Notes 5, 6</a> )	66	0.95
20 Ld 3x4 TQFN ( <a href="#">Notes 5, 7</a> )	48	16

Notes:

- $\theta_{JA}$  is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See [TB379](#).
- For  $\theta_{JC}$ , the “case temp” location is taken at the package top center.
- For  $\theta_{JC}$ , the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+125	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see <a href="#">TB493</a>		

### 2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+85	°C
VIN	2.8	4.4	V
VP	+5	+5.7	V
VN	-5	-5.7	V
VBST	+5.15	+6.0	V
Output Current Maximum (between VP and VN)		100	mA

## 2.4 Electrical Specifications

$V_{IN} = 3.7V$ , unless otherwise noted. Typical specifications are characterized at  $T_A = +25^\circ C$  unless otherwise noted. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
<b>General</b>						
$V_{IN}$ Supply Voltage Range	$V_{IN}$		<b>2.8</b>		<b>4.4</b>	V
$V_{IN}$ Supply Current	$I_{IN}$	ENP = ENN = 3.7V Enabled, LXP not switching		620	<b>900</b>	$\mu A$
$V_{IN}$ Supply Current When Shutdown	$I_{SHUTDOWN}$	ENP = ENN = 0V		1	<b>3</b>	$\mu A$
Undervoltage Lockout Threshold	$V_{UVLO}$	$V_{IN}$ rising	<b>2.40</b>	2.52	<b>2.65</b>	V
Undervoltage Lockout Hysteresis	$V_{UVLO\_HYS}$	5ms falling		216		mV
<b>Boost Regulator (VBST)</b>						
VBST Output Voltage	$V_{VBST}$	Register VBST_OUT = 0x00, no load		5.15		V
Boost nFET Current Limit	$I_{LIM\_VBST}$		<b>1.2</b>	1.4	<b>1.8</b>	A
Low-Side Switch ON-Resistance	$r_{ON\_VBSTH}$	$T_A = +25^\circ C$ , $I_{LOAD\_VBST} = 100mA$ , LXP to PGND		137		m $\Omega$
High-Side Switch ON-Resistance	$r_{ON\_VBSTL}$	$T_A = +25^\circ C$ , $I_{LOAD\_VBST} = 100mA$ , LXP to VBST		220		m $\Omega$
LXP Leakage Current	$I_{L\_LXP}$	VLXP = 6V, ENP = ENN = 0V			<b>10</b>	$\mu A$
Boost Minimum Duty Cycle	$D_{MIN}$	Boost frequency = 1.45MHz		12.5		%
Boost Maximum Duty Cycle	$D_{MAX}$	Boost frequency = 1.45MHz		91		%
Boost Switching Frequency	$f_{SWV\_VBST}$	Boost frequency = default	<b>1.3</b>	1.45	<b>1.6</b>	MHz
Boost Soft-Start Time	$t_{SS\_VBST}$	$C_{VBST} = 10\mu F$ (not derated), $V_{IN} > V_{UVLO}$		0.7	<b>2</b>	ms
<b>Negative Regulator (VN)</b>						
VN Output Voltage	$V_{VN}$	VN_OUT = 0x00, no load		-5		V
VN Output Voltage Accuracy	$V_{ACC\_VN}$	VN_OUT = 0x00, VBST_OUT = 0x00, $-30mA < I_{LOAD\_VN} < 0mA$	<b>-2</b>		<b>2</b>	%
Charge Pump Switching Frequency	$f_{SW\_VN}$	CP Frequency = default, 50% duty cycle	<b>1.3</b>	1.45	<b>1.6</b>	MHz
Charge Pump Leakage Current	$I_{L\_CP}$	CP pin, CP = 6V, ENN = 0V			<b>10</b>	$\mu A$
VN Discharge Resistance	$R_{DCH\_VN}$	VN = -1V		35		$\Omega$
VN Soft-Start Time	$t_{SS\_VN}$			0.7	<b>2</b>	ms
<b>Positive Regulator (VP)</b>						
VP Output Voltage	$V_{VP}$	VBST_OUT = 0x00, No Load		5		V
VP Output Voltage Accuracy	$V_{ACC\_VP}$	VP_OUT = 0x00, VBST_OUT = 0x00, $0mA < I_{LOAD\_VP} < 30mA$	<b>-2</b>		<b>2</b>	%
VP Dropout Voltage	$V_{DRP\_VP}$	$I_{LOAD\_VP} = 100mA$			<b>100</b>	mV
VP Leakage Current	$I_{L\_VP}$	VP pin, VP = 0V, ENP = 0V			<b>2</b>	$\mu A$
VP Discharge Resistance	$R_{DCH\_VP}$	VP = 1V		80		$\Omega$
VP Soft-Start	$t_{SS\_VP}$			0.7	<b>2</b>	ms
<b>Protection</b>						
Thermal Shutdown Temperature	$T_{OFF}$	Die temperature (rising) when the device will disable/shutdown all outputs until it cools by $T_{HYS}^\circ C$		130		$^\circ C$
Thermal Shutdown Hysteresis	$T_{HYS}$	Die temperature below $T_{OFF}^\circ C$ when the device will re-enable the outputs after shutdown		10		$^\circ C$
VP Undervoltage Protection Threshold	$V_{UVP\_VP}$			$0.6 \times VP$		V
VN Undervoltage Protection Threshold	$V_{UVP\_VN}$			$0.6 \times VN$		V

$V_{IN} = 3.7V$ , unless otherwise noted. Typical specifications are characterized at  $T_A = +25^\circ C$  unless otherwise noted. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

Parameter	Symbol	Test Conditions	Min ( <a href="#">Note 8</a> )	Typ	Max ( <a href="#">Note 8</a> )	Unit
<b>Logic/Digital</b>						
Logic Input Low Voltage	$V_{IL}$	ENN, ENP, SCL, SDA			<b>0.4</b>	V
Logic Input High Voltage	$V_{IH}$	ENN, ENP, SCL, SDA	<b>1.1</b>			V
I <sup>2</sup> C SCL Clock Frequency	$f_{CLK}$	( <a href="#">Note 9</a> )			<b>400</b>	kHz
Debounce Time	$t_d$	ENN, ENP		10		$\mu s$
Internal Pull-Down Resistance	$R_{EN}$	ENN, ENP		200		k $\Omega$

Notes:

8. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. For more detailed information regarding I<sup>2</sup>C timing characteristics see [Table 1 on page 10](#).

### 3. Typical Performance Curves

$T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ , Registers VP\_OUT, VN\_OUT and VBST\_OUT = 0x00, DFE252012C (2.5mmx2mm) Toko Inductor,  $C_{VBST} = 10\mu\text{F}/0402$ ,  $C_{VP} = 10\mu\text{F}/0402$  and  $C_{VN} = 2 \times 10\mu\text{F}/0402$  unless otherwise noted.

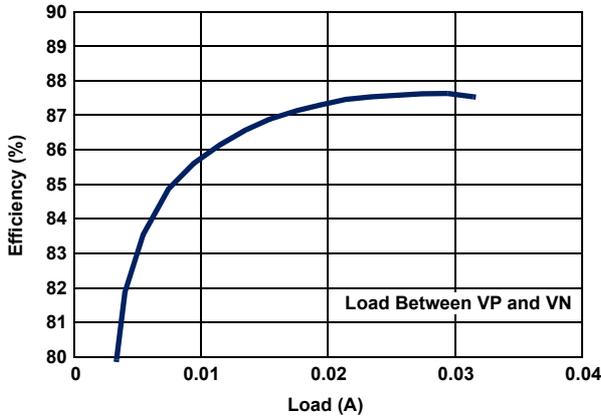


Figure 2. Efficiency vs Load - Register 0x0D = 0x04, Register 0x0F = 0xDF

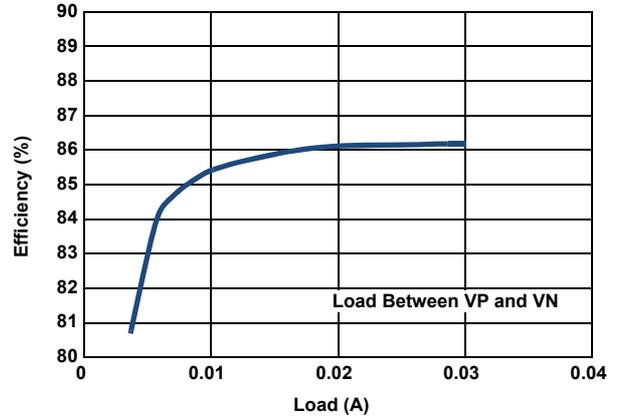


Figure 3. Efficiency vs Load - Register 0x0D = 0x34, Register 0x0F = 0xDA

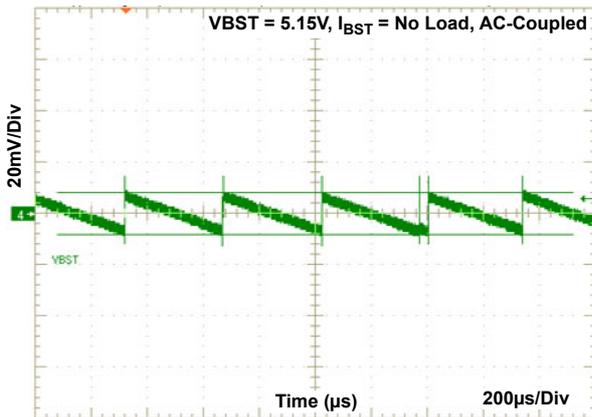


Figure 4. VBST Output Voltage Ripple with No Load

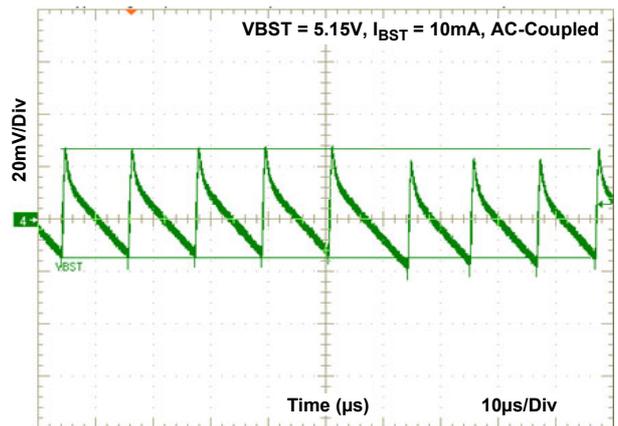


Figure 5. VBST Output Voltage Ripple with 10mA Load

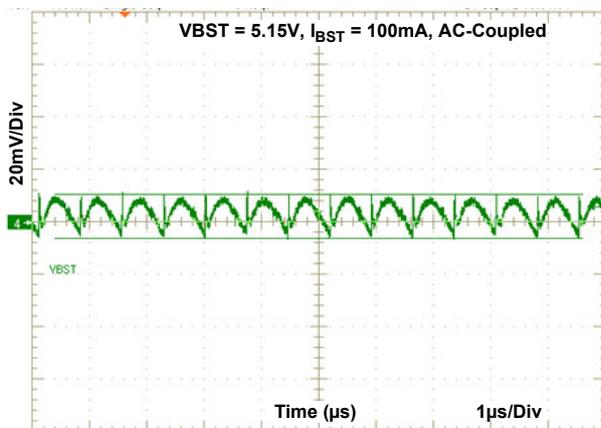


Figure 6. VBST Output Voltage Ripple with 100mA Load

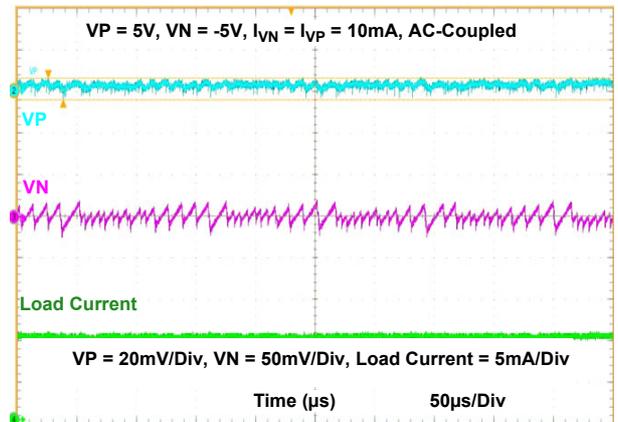


Figure 7. VP and VN Output Voltage Ripple - 10mA Load

$T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ , Registers VP\_OUT, VN\_OUT and VBST\_OUT = 0x00, DFE252012C (2.5mmx2mm) Toko Inductor,  $C_{VBST} = 10\mu\text{F}/0402$ ,  $C_{VP} = 10\mu\text{F}/0402$  and  $C_{VN} = 2 \times 10\mu\text{F}/0402$  unless otherwise noted. (Continued)

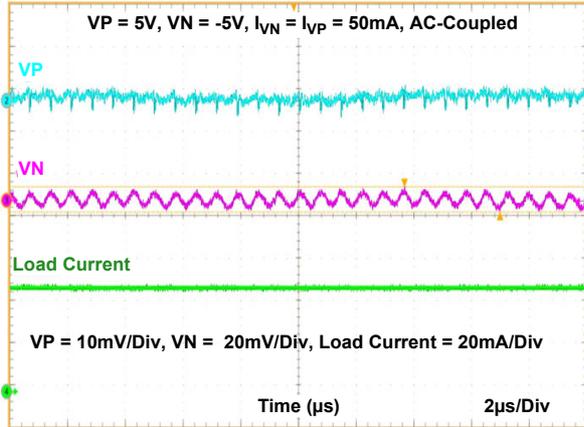


Figure 8. VP and VN Output Voltage Ripple - 50mA Load

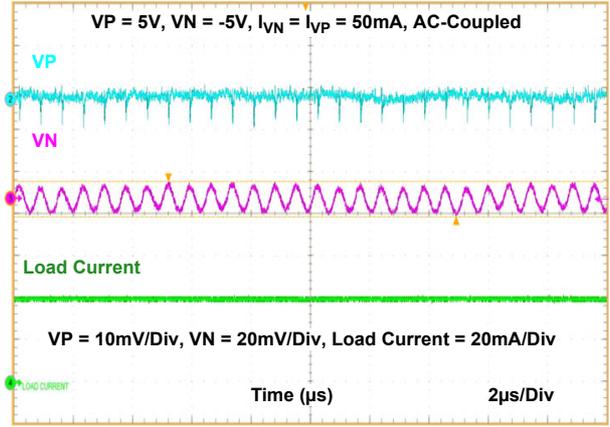


Figure 9. VP and VN Output Voltage Ripple - 100mA Load

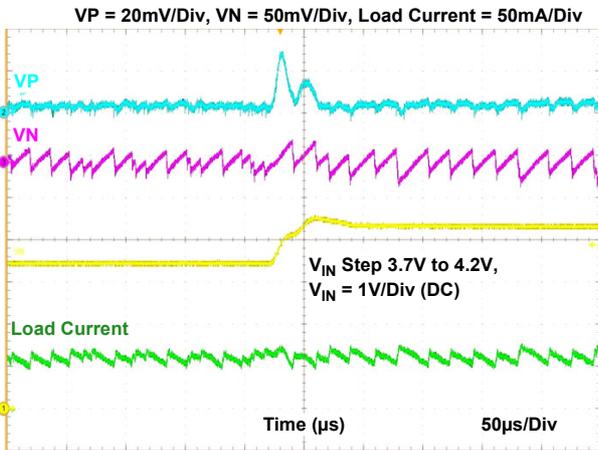


Figure 10. Line Transient

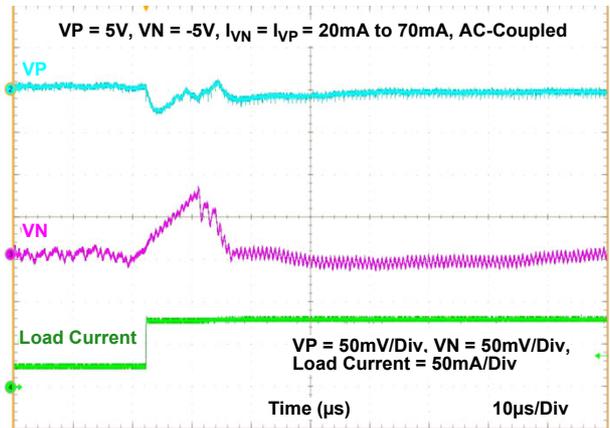


Figure 11. VP and VN Load Transient - Load Step Up

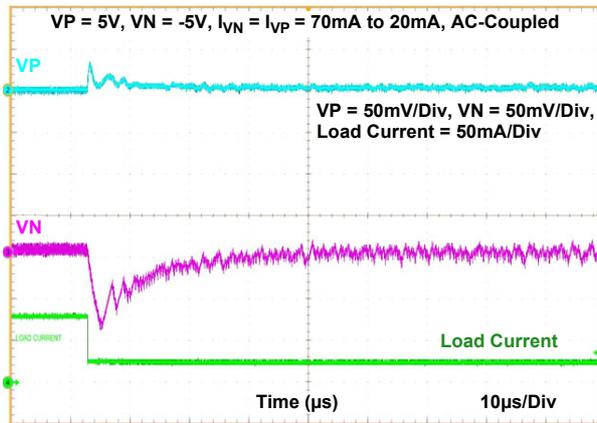


Figure 12. VP and VN Load Transient - Load Step Down

## 4. Application Information

### 4.1 I<sup>2</sup>C Digital Interface

The ISL98607 uses a standard I<sup>2</sup>C interface bus for communication. The two-wire interface links a Master(s) and uniquely addressable Slave devices. The Master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line and the serial data (bi-directional) is on the SDA line. The ISL98607 supports clock rates up to 400kHz (Fast-Mode), and is backwards compatible with standard 100kHz clock rates (Standard-mode).

The SDA and SCL lines must be HIGH when the bus is free (not in use). An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) or current-source is required for SDA and SCL.

The ISL98607 meets standard I<sup>2</sup>C timing specifications. [Figure 13](#) and [Table 1 on page 10](#) show the standard timing definitions and specifications for I<sup>2</sup>C communication.

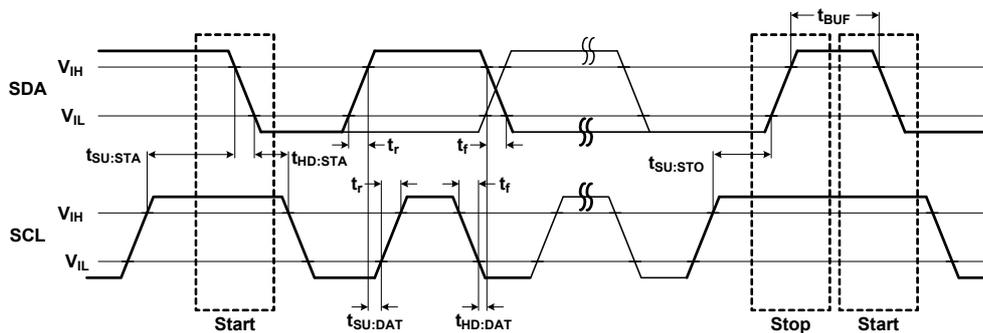


Figure 13. I<sup>2</sup>C Timing Definitions

Table 1. I<sup>2</sup>C Timing Characteristics

Parameter	Symbol	Fast-Mode		Standard-Mode		Unit
		Min	Max	Min	Max	
SCL Clock Frequency	f <sub>SCL</sub>	0	400	0	100	kHz
Set-Up Time for a Start Condition	t <sub>SU:STA</sub>	0.6	-	4.7	-	μs
Hold Time for a Start Condition	t <sub>HD:STA</sub>	0.6	-	4.0	-	μs
Set-Up Time for a Stop Condition	t <sub>SU:STO</sub>	0.6	-	4.0	-	μs
Bus Free Time between a Stop and Start Condition	t <sub>BUF</sub>	1.3	-	4.7	-	μs
Data Set-up Time	t <sub>SU:DAT</sub>	100	-	250	-	ns
Data Hold Time	t <sub>HD:DAT</sub>	0	-	0	-	μs
Rise Time of SDA and SCL ( <a href="#">Note 10</a> )	t <sub>r</sub>	20 + 0.1C <sub>b</sub>	300	-	1000	ns
Fall Time of SDA and SCL ( <a href="#">Note 10</a> )	t <sub>f</sub>	20 + 0.1C <sub>b</sub>	300	-	300	ns
Capacitive Load on Each Bus Line (SDA/SCL)	C <sub>b</sub>	-	400	-	400	pF

Note:

10. C<sub>b</sub> = total capacitance of one bus line in pF.

#### 4.1.1 Low-Power Mode

The I<sup>2</sup>C interface of ISL98607 remains active even when both ENN and ENP are LOW for up to 30ms. When ENN and ENP both remain LOW, and no I<sup>2</sup>C communication occurs for more than 30ms, the ISL98607 enters a low-power mode. This mode disables the I<sup>2</sup>C interface, but the interface is re-activated as soon as ISL98607 detects a logic LOW on SCL or SDA.

For the ISL98607, when the I<sup>2</sup>C interface is not used, both the SDA and SCL inputs must be tied HIGH (such as to VIN) or pulled-up to a logic HIGH level, to ensure the part enters the Low-Power consumption mode when ENN and ENP are held LOW longer than 30ms. This feature optimizes battery power saving in handheld products, such as, when the display system is put into a standby/sleep mode.

### 4.1.2 Start and Stop Condition

All I<sup>2</sup>C communication begins with a Start condition (indicating the beginning of a transaction) and ends with a Stop condition (signaling the end of the transaction).

A Start condition is signified by a HIGH-to-LOW transition on the serial data line (SDA) while the serial clock line (SCL) is HIGH. A Stop condition is signified by a LOW-to-HIGH transition on the SDA line while SCL is HIGH. See the timing specifications in [Table 1 on page 10](#).

The Master always initiates Start and Stop conditions. After a Start condition, the bus is considered “busy.” After a Stop condition, the bus is considered “free.” The ISL98607 also supports repeated Starts, where the bus remains busy for the continued transaction(s).

### 4.1.3 Data Validity

The data on the SDA line must be stable (clearly defined as HIGH or LOW) during the HIGH period of the clock signal. The state of the SDA line can only change when the SCL line is LOW (except to create a Start or Stop condition). See the timing specifications in [Table 1](#).

The voltage levels indicating a logical ‘0’ (LOW) and logical ‘1’ (HIGH) are determined by the  $V_{IL}$  and  $V_{IH}$  thresholds, respectively, see the “Electrical Specifications” table on [page 7](#).

### 4.1.4 Byte Format

Every byte transferred on SDA must be 8 bits in length. After every byte of data sent by the transmitter there must be an Acknowledge bit (from the receiver) to signify that the previous 8 bits were transferred successfully. Data is always transferred on SDA with the Most Significant Bit (MSB) first. See [Acknowledge \(ACK\)](#).

### 4.1.5 Acknowledge (ACK)

Each 8-bit data transfer is followed by an Acknowledge (ACK) bit from the receiver. The Acknowledge bit signifies that the previous 8 bits of data was transferred successfully (master-slave or slave-master).

When the Master sends data to the Slave (such as, during a WRITE transaction), after the 8th bit of a data byte is transmitted, the Master tri-states the SDA line during the 9th clock. The Slave device acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

When the Master receives data from the Slave (such as during a data READ transaction), after the 8th bit is transmitted, the Slave tri-states the SDA line during the 9th clock. The Master acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

### 4.1.6 Not Acknowledge (NACK)

A Not Acknowledge (NACK) is generated when the receiver does not pull-down the SDA line during the acknowledge clock (for example, SDA line remains HIGH during the 9th clock), which indicates to the Master that it can generate a Stop condition to end the transaction and free the bus.

A NACK can be generated for various reasons, for example:

- After an I<sup>2</sup>C device address is transmitted, there is NO receiver with that address on the bus to respond.
- The receiver is busy performing an internal operation (such as, reset, recall, etc), and cannot respond.
- The Master (acting as a receiver) needs to indicate the end of a transfer with the Slave (acting as a transmitter).

### 4.1.7 Device Address and R/W Bit

Data transfers follow the format shown in [Figures 15](#) and [16](#). After a valid Start condition, the first byte sent in a transaction contains the 7-bit Device (Slave) Address plus a direction (R/W) bit. The Device Address identifies which device (of up to 127 devices on the I<sup>2</sup>C bus) the Master wishes to communicate with.

After a Start condition, the ISL98607 monitors the first 8 bits (Device Address Byte) and checks for its 7-bit Device Address in the MSBs. If it recognizes the correct Device Address, it acknowledges and becomes ready for further communication. If it does not see its Device Address, it sits idle until another Start condition is issued on the bus.

To access the ISL98607, the 7-bit Device Address is 0x29 (0101001x), located in MSB bits <b<sub>7</sub>:b<sub>1</sub>>. The 8th bit of the Device Address byte (LSB bit <b<sub>0</sub>>) indicates the direction of transfer, READ or WRITE (R/W). A “0” indicates a WRITE operation (the Master transmits data to the ISL98607 (receiver)). A “1” indicates a Read operation (the Master receives data from the ISL98607 (transmitter)), see [Figure 14](#).

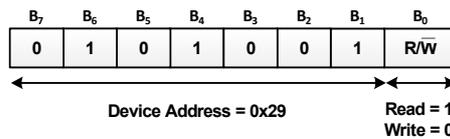


Figure 14. Device Address Byte Format

### 4.2 Write Operation

A WRITE sequence requires an I<sup>2</sup>C Start condition, followed by a valid Device Address Byte with the R/W bit set to ‘0’, a valid Register Address Byte, a Data Byte, and a Stop condition. After each valid byte is sent, the ISL98607 (slave) responds with an ACK. When the Write transaction is completed, the Master should generate a Stop condition. For sent data to be latched by the ISL98607, the Stop condition should occur after a full byte (8-bits) is sent and ACK. If a Stop is generated in the middle of a byte transaction, the data is ignored. See [Figure 15](#) for the ISL98607 I<sup>2</sup>C Write protocol.

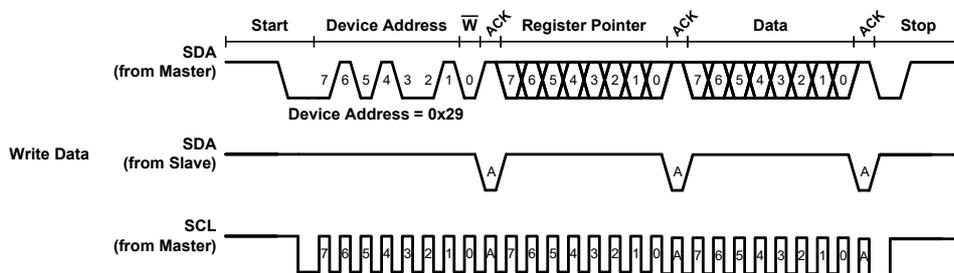


Figure 15. I<sup>2</sup>C Write Timing Diagram

### 4.3 Read Operation

A READ sequence requires the Master to first write to the ISL98607 to indicate the Register Address/pointer to read from. Send a Start condition, followed by a valid Device Address Byte with the R/W set to ‘0’, and then a valid Register Address Byte. Then the Master generates either a Repeat Start condition, or a Stop condition followed by a new Start condition, and a valid Device Address Byte with the R/W bit set to ‘1’. Finally, the ISL98607 is ready to send data to the Master from the requested Register Address.

The ISL98607 sends out the Data Byte by asserting control of the SDA pin while the Master generates clock pulses on the SCL pin. When transmission of the desired data is complete, the Master generates a NACK condition followed by a Stop condition, and this completes the I<sup>2</sup>C Read sequence. See [Figure 16 on page 13](#) for the ISL98607 I<sup>2</sup>C Read protocol.

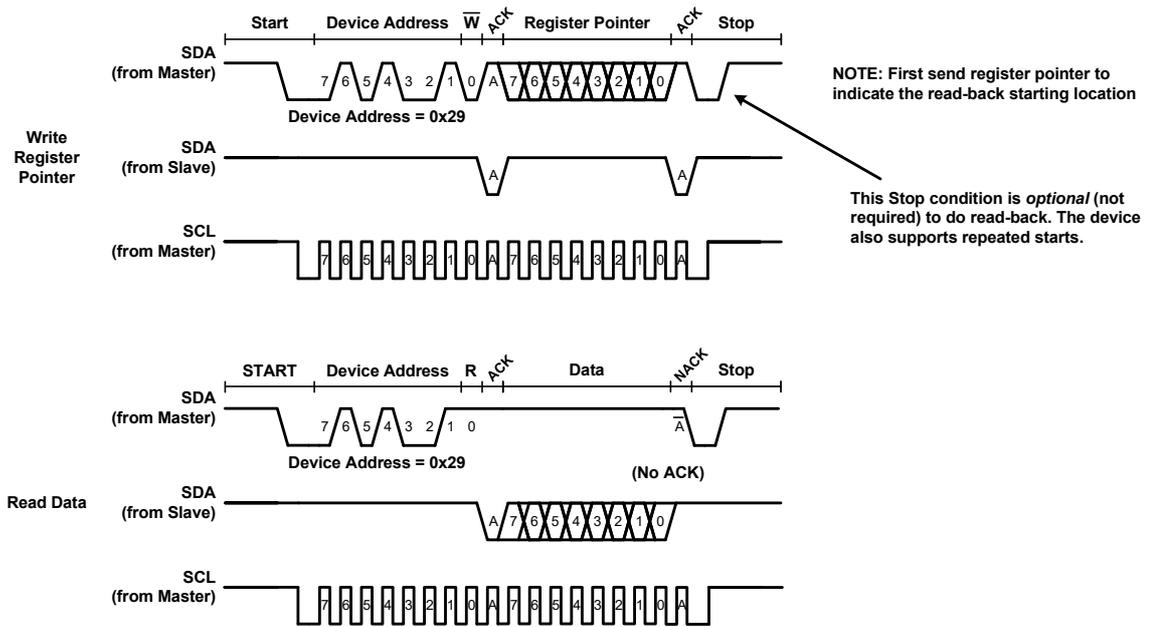


Figure 16. I<sup>2</sup>C Read Timing Diagram

### 4.4 Register Descriptions and Addresses

Table 2 on page 15 contains the detailed register map, with descriptions and addresses for ISL98607 registers. Each volatile register is one byte (8-bit) in size. When writing data to adjust register settings using I<sup>2</sup>C, the data is latched-in after the 8th bit (LSB) is received.

The ISL98607 has default register settings that are always applied at IC power-ON or after a reset. In Table 2, the default register settings are indicated with **Bold** face text.

Reserved registers should only be written with the bit value indicated in the Register Map. Also, Register Addresses (pointers) not indicated in the Register Map are reserved and should not be written to.

Note: To clear/reset all the volatile registers to the default values, power cycle VIN.

### 4.5 Register Functions

The ISL98607 has various registers that can be used to adjust and control IC operating voltages, modes, thresholds, and sequences.

#### 4.5.1 ENABLE

The “ENABLE” register (Register Address 0x05) controls the enable/disable state of the boost (VBST), positive LDO (VP), and negative charge pump (VN) regulators, which sequences the regulators.

#### 4.5.2 VBST\_OUT, VN\_OUT, VP\_OUT

The output voltages of VBST, VP, and VN regulators are changed using the registers VBST\_OUT (Register Address 0x06), VP\_OUT (Register Address 0x09), and VN\_OUT (Register Address 0x08), respectively.

The output voltages of all three regulators are changed from their default values using I<sup>2</sup>C. The VP regulator is programmed from +5V to +5.7V, the VN regulator is programmed from -5V to -5.7V, and the VBST regulator is programmed from +5.15V to +6.0V (each adjustable with 50mV step size). Do not use register settings that result in an expected output voltage above these maximum levels. To determine the expected output voltage for a specific register value, see “Output Voltage Calculation” on page 14.

Note: The output voltage registers should not be changed during their respective soft-start sequence.

#### 4.5.2.1 Output Voltage Calculation

The expected output voltage for each regulator is determined using [Equations 1](#) through [3](#). For the calculations: VBST = 5.15V (typical) default, VP = +5V (typical) default, VN = -5V (typical) default. Note: VBST\_OUT, VP\_OUT, and VN\_OUT are the respective 5-bit register settings in decimal.

- Boost Output Voltage, VBST:

$$(EQ. 1) \quad VBST(V) = VBST + VBST\_OUT \times 50mV$$

- LDO Output Voltage, VP

$$(EQ. 2) \quad VP(V) = VP + VP\_OUT \times 50mV$$

- Negative Charge Pump Output Voltage, VN:

$$(EQ. 3) \quad VN(V) = VN - VN\_OUT \times 50mV$$

Example Calculations:

If VBST\_OUT = 10 (dec):

$$VBST(V) = 5.15V + 10 \times 50mV = 5.65V$$

If VP\_OUT = 10 (dec):

$$VP(V) = 5V + 10 \times 50mV = 5.5V$$

If VN\_OUT = 10 (dec):

$$VN(V) = -5V - 10 \times 50mV = -5.5V$$

#### 4.5.3 VBST\_CNTRL, VN\_CNTRL

In addition to output voltages adjustments, key operation parameters are changed using the I<sup>2</sup>C to optimize the ISL98607 performance.

The “VBST\_CNTRL” register (Register Address 0x0D) controls and optimizes boost PFM mode, boost FET slew rate, and switching frequency of the boost and charge pump.

The VN\_CNTRL register (Register Address 0x0F) enables and disables the PFM mode, and optimizes the charge pump PFM operation with adjustments to the PFM peak current, and pulse length.

#### 4.5.4 FAULT

The “FAULT” register (Register Address 0x04) reads back the current fault status of the IC. The fault conditions that are read back by I<sup>2</sup>C are:

- VBST undervoltage fault
- VP undervoltage fault
- VN undervoltage fault
- Over-Temperature Protection (OTP)

FAULT register bits <b<sub>3</sub>:b<sub>0</sub>> are reset by cycling the logic voltage on both the ENP and ENN pins simultaneously (set ENN = ENP = LOW, then ENN = ENP = HIGH) or power cycling VIN.

If FAULT register bit <b<sub>0</sub>> (OTP status bit) is latched HIGH for an OTP fault, it is reset after it is read twice by the I<sup>2</sup>C. A single I<sup>2</sup>C read returns the bit value (status), and a second read resets only the OTP bit.

## 4.6 Register Map

Table 2. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	R/W	FUNCTION	BIT <b <sub>7</sub> >	BIT <b <sub>6</sub> >	BIT <b <sub>5</sub> >	BIT <b <sub>4</sub> >	BIT <b <sub>3</sub> >	BIT <b <sub>2</sub> >	BIT <b <sub>1</sub> >	BIT <b <sub>0</sub> >	DEFAULT VALUE (HEX)	IC RESET
0x04	FAULT	R	Fault Status read-back	Reserved (Always set to '0')	Not Used			VP UVP: 0 = Output Voltage OK 1 = UVP Detect	VN UVP: 0 = Output Voltage OK 1 = UVP Detect	VBST UVP: 0 = Output Voltage OK 1 = UVP Detect	OTP: 0 = Temp Ok 1 = OTP detected	0x00	Cycle ENN and ENP, or cycle VIN
0x05	ENABLE	R/W	IC Enable / Sequencing	Reserved (Always set to '0')	VP Pull-down resistor <b>0 = Enabled</b> 1 = Disabled	Not Used			VP: 0 = Disable <b>1 = Enable</b>	VN: 0 = Disable <b>1 = Enable</b>	VBST: 0 = Disable <b>1 = Enable</b>	0x07	Cycle VIN
0x06	VBST_OUT	R/W	VBST Voltage Adjustment	Not Used			VBST_OUT <4:0>					0x00	Cycle VIN
0x08	VN_OUT	R/W	VN Voltage Adjustment	Not Used			VN_OUT <4:0>					0x00	Cycle VIN
0x09	VP_OUT	R/W	VP Voltage Adjustment	Not Used			VP_OUT <4:0>					0x00	Cycle VIN
0x0D	VBST_CNTRL	R/W	VBST - boost regulator control	Reserved (Always set to '00')		Boost LX slew rate <b>11 = Slowest</b> 10 = Slow 01 = Fast 00 = Fastest		PFM mode (synchronous PFM) <b>0 = Enable</b> 1 = Disable	Boost and Charge Pump Switching Frequency 000 = 0.89 MHz 001 = 1.07 MHz 010 = 1.23 MHz 011 = 1.33 MHz <b>100 = 1.45 MHz</b> 101 = 1.60 MHz 110 = 1.78 MHz 111 = 2.00 MHz			0x34	Cycle VIN
0x0F	VN_CNTRL	R/W	VN - negative charge pump control	Reserved (Always set to '11')		PFM Mode <b>0 = Enabled</b> 1 = Disabled	PWM min pulse length <b>1 = 94ns</b> 0 = 125ns	PFM peak current selection 00 = 4µA 01 = 6µA <b>10 = 5µA</b> 11 = 7µA		PFM Pulse length 00 = 188ns 01 = 219ns <b>10 = 250ns</b> 11 = 50% selected frequency		0xDA	Cycle VIN

Notes:

11. Any Register Addresses/Pointers not indicated are Reserved Registers, and should not be used.
12. Bits labeled "Not Used" can be written and read from the volatile registers, but have no influence on the operation of the IC.

## 4.7 Output Voltage Setting

The VBST, VP, and VN output voltages are adjusted (from the default value) by the VBST\_OUT, VP\_OUT, and VN\_OUT volatile registers. [Equations 1](#) through [3](#) on [page 14](#) provide the relation between the value of the I<sup>2</sup>C registers and the respective output voltages.

## 4.8 VP and VN Headroom Voltage and Output Current

The VP and VN headroom voltage is defined as the difference between the VBST output voltage and:

- the maximum VP output voltage: VP headroom
- the absolute value of the VN output voltage: VN headroom

The headroom voltage must be set high enough so that both the VP LDO and VN negative Charge Pump (CP) can maintain regulation. Primarily, the minimum headroom voltage is a function of the maximum application load current that the IC needs to support for at least few hundreds of microseconds. Fast output current peaks of only a few microseconds should not be considered (those instantaneous current peaks are supported by the output capacitors and not by the regulator).

Note: The headroom voltage should not be set overly high, because increasing headroom generally yields lower efficiency performance due to increased conduction losses.

For most applications, the ISL98607 default 150mV headroom voltage setting provides optimal performance for DC output current up to 100mA (maximum). For DC output current between 100mA and 150mA (maximum), the headroom voltage should be adjusted to 250mV. For example: if a maximum VP to VN load of 150mA is required, while VP = 5V and VN = -5V, then the minimum boost voltage should be set to VBST = 5.25V.

## 4.9 Regulator Output Enable/Disable

The boost converter, VBST, will be enabled whenever either ENP or ENN is HIGH, and the VBST enable bit <b<sub>0</sub>> in the ENABLE register is set to '1'. To disable the boost (and effectively VP and VN), ENN and ENP must be LOW, or its enable bit set to '0'.

The negative charge pump, VN, is enabled whenever ENN is HIGH, and the VN enable bit <b<sub>1</sub>> in the ENABLE register is set to '1'. To disable, ENN must be LOW, or its enable bit set to '0'.

The LDO, VP, is enabled whenever ENP is HIGH, and the VP enable bit <b<sub>2</sub>> in the ENABLE register is set to '1'. To disable ENP must be LOW, or its enable bit set to '0'.

All the ENABLE register bits <b<sub>2</sub>:b<sub>0</sub>> are set to '1' by default.

Various options to control the regulator output ON/OFF sequencing are possible with ISL98607, refer to the [“Enable Timing Control Options” on page 19](#) for more information.

Note, ENP and ENN are logic level inputs with HIGH/LOW thresholds defined by the V<sub>IH</sub>/V<sub>IL</sub> specifications, respectively. These inputs also have 200kΩ (typical) internal pull-down resistance to ground. If the pins are left hi-impedance, they will default to a LOW logic state. Refer to the “Logic” section of the “Electrical Specifications” table on [page 7](#) for more information.

## 4.10 Negative Charge Pump Operation (VN)

The ISL98607 uses a negative charge pump with internal switches to create the VN voltage rail. The charge pump input voltage VBSTCP comes from the boost regulator output, VBST. The VBST voltage must be greater than the absolute value of the VN regulation voltage (for example, the headroom voltage has to be > 0V).

Regulation is achieved through a classic voltage mode architecture where an internally compensated gm amplifier compares the VN output voltage to the internal reference and sets a duty cycle. The duty cycle controls the amount of time the output capacitor is charged during each switching cycle. The maximum duty cycle is 50%. The charge pump output capacitor (placed on the VN pin) is charged and discharged through internal 450mA current sources to minimize system noise.

## 4.11 PFM

The ISL98607 features light-load Pulse Frequency Modulation (PFM) mode for both the boost regulator and charge pump to maximize efficiency at light loads.

The ISL98607 always uses PWM mode at heavy loading, but when PFM mode is enabled using the respective PFM mode enable/disable register bit, it automatically switches to PFM mode at light loads to optimize efficiency.

There is hysteresis built-in with the PFM transition for when the transition is from light to heavy or heavy to light loading, which prevents inadvertently going back and forth between PWM and PFM modes.

## 4.12 Fault Protection and Monitoring

The ISL98607 features extensive protections to automatically handle failure conditions and protect the IC and application from damage.

### 4.12.1 Overcurrent Protection (OCP)

The overcurrent protection limits the VBST nMOSFET current on a cycle-by-cycle basis. When the nMOSFET current reaches the current limit threshold, the nMOSFET is turned off for the remainder of that cycle. Overcurrent protection does not disable any of the regulators. When the fault is removed, the IC continues with normal operation.

### 4.12.2 Undervoltage Lockout (UVLO)

If the input voltage ( $V_{IN}$ ) falls below the  $V_{UVLO\_HYS}$  level of ~2.3V (typical), the VBST, VP, and VN regulators are disabled. All the rails restart with normal soft-start operation when the  $V_{IN}$  input voltage is applied again (rising  $V_{IN} > V_{UVLO}$ ). See the “Electrical Specifications” table on [page 6](#) for the UVLO specifications.

Note: The I<sup>2</sup>C registers (logic) are not cleared/reset to default by the falling  $V_{IN}$  UVLO. The logic states are retained if  $V_{IN}$  remains above 2V (typical). When  $V_{IN}$  falls below 2V, all logic is reset.  $V_{IN}$  should fall below 2V (ideally to GND) before power is reapplied to ensure a full power cycle/reset of the device.

### 4.12.3 Over-Temperature Protection (OTP)

The ISL98607 has a hysteretic over-temperature protection threshold set at +130°C (typical). If this threshold is reached, the VBST, VP, and VN regulators are disabled immediately. As soon as temperature falls by 10°C (typical) then all the regulators automatically restart.

All register bits, except for bit  $\langle b_0 \rangle$  of the FAULT register (Register Address 0x04), remain unaffected during an OTP fault event. When an OTP event occurs, FAULT register bit  $\langle b_0 \rangle$  is latched to ‘1’. This bit is reset/cleared by cycling both ENN and ENP (set LOW, then HIGH) at the same time, or by cycling  $V_{IN}$  power. Bit  $\langle b_0 \rangle$  can also be reset after it is read twice by I<sup>2</sup>C. A single I<sup>2</sup>C read returns the bit value (status), and a second read resets only the OTP bit.

Output undervoltage protection is disabled during an OTP event. The output voltages decrease during an OTP event because the regulators are disabled, which does not trigger a UVP fault.

### 4.12.4 Undervoltage Protection (UVP)

The ISL98607 includes output undervoltage protection. Undervoltage protection disables the regulator whenever the output voltage of VBST or VP falls below 60% of its set/regulated voltage, or the output voltage of VN goes above 60% of its set/regulated voltage, for 100μs or more. If the output voltage exceeds the 60% condition for less than 100μs, no fault occurs.

Depending on which regulator(s) fault, bit(s)  $\langle b_3 \rangle$ ,  $\langle b_2 \rangle$ , or  $\langle b_1 \rangle$  in the FAULT register are latched to ‘1’ for VP, VN, and VBST faults, respectively. The bit(s) are reset/cleared by cycling both ENN and ENP (set LOW, then HIGH) at the same time, or by cycling  $V_{IN}$  power.

### 4.13 Power-ON/OFF Sequence

The boost regulator is activated when the  $V_{IN}$  input voltage is higher than the UVLO threshold, and either ENP or ENN are HIGH. The VP output is activated if ENP is HIGH and VBST has completed its soft-start. The VN charge pump is activated 2ms after VBST has completed soft-start, and the ENN has been pulled high, whichever comes later (see [Figure 17](#)).

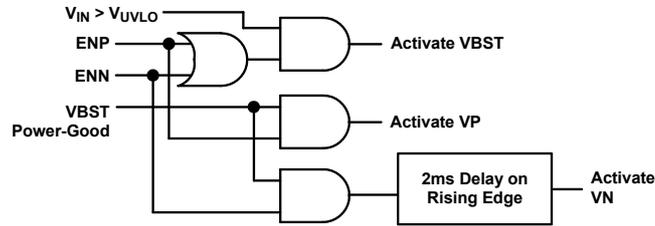


Figure 17. Power-On Logic Operation

[Figure 18](#) shows power-ON timing for the case when ENN is pulled HIGH after ENP, and after the VBST soft-start is complete. [Figure 19](#) shows power-ON timing for the case when ENN is pulled HIGH after ENP, but before VBST has completed its soft-start.

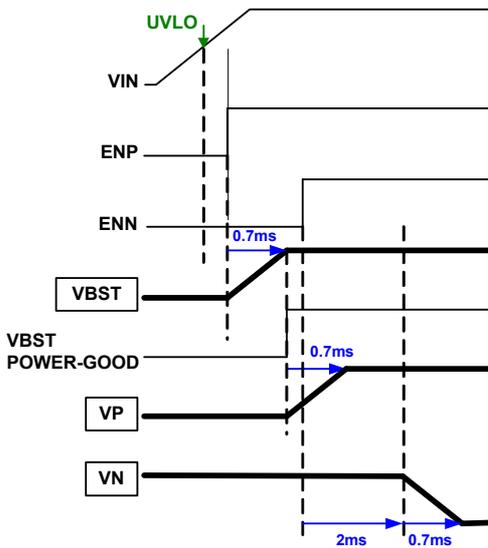


Figure 18. Power-On Sequence - ENN Rising After VP Soft-Start Finished

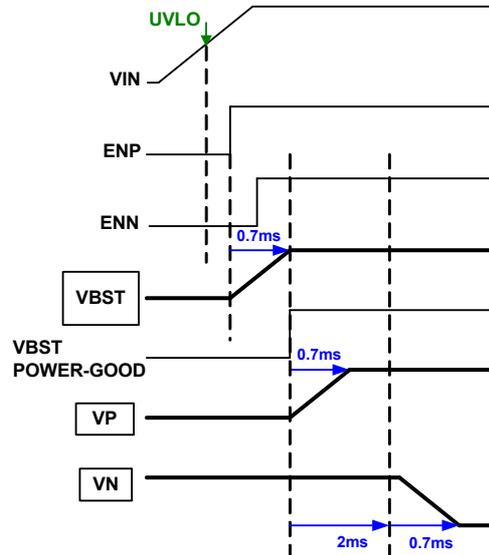
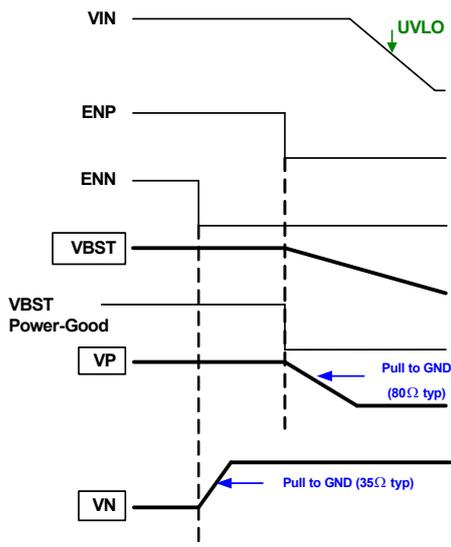
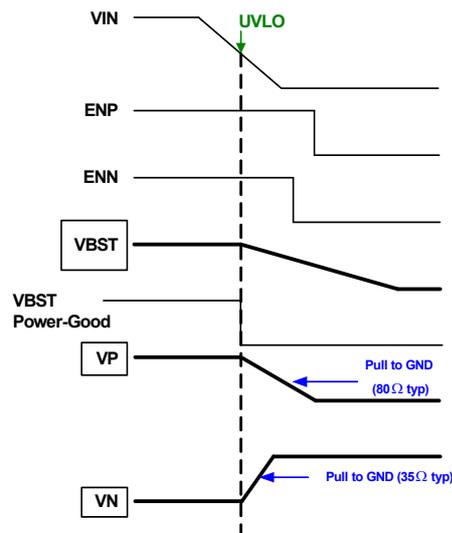


Figure 19. Power-On Sequence - Both ENP and ENN Rising Before VBST Soft-Start Finished

ENP or ENN going LOW shuts down VP or VN, respectively. If both ENP and ENN are pulled low, VP, VN, and VBST are all turned off even if  $V_{IN}$  is still above UVLO, see [Figure 20 on page 19](#). If  $V_{IN}$  falls below UVLO while ENP and ENN are high, VP, VN, and VBST are turned off at the same time (see [Figure 21 on page 19](#)).



**Figure 20. Power-Off Sequence - Activated by ENP and ENN When VIN is Above UVLO**



**Figure 21. Power-Off Sequence - Activated by VIN Falling Below UVLO**

The integrated discharge resistors on the VP and VN outputs are  $80\Omega$  (typical) and a  $35\Omega$  (typical), respectively. If the same output capacitor (value, size, rating) is used for VN and VP, the VN rail discharges faster than VP if they are both turned off at the same time, which is ideal for applications that require the VN rail to go down before VP at power-OFF.

#### 4.14 Enable Timing Control Options

Three ways to control enable sequencing of the VP and VN regulators are:

- I<sup>2</sup>C control
- Dual GPIO control
- Single GPIO control

##### 4.14.1 I<sup>2</sup>C Control

By using I<sup>2</sup>C, the sequencing of the VP and VN regulator is controlled by writing to the register 0x05. Bit  $\langle b_1 \rangle$  controls the VN regulator and  $\langle b_2 \rangle$  controls the VP regulator. Setting the bits to '1' enables the regulator and setting to '0' shuts off/disables the regulator. Delaying the writes for setting bit  $\langle b_1 \rangle$  and  $\langle b_2 \rangle$  (using separate I<sup>2</sup>C transactions) delays the turn-on and turn-off sequence of VP and VN accordingly.

[Figure 22 on page 20](#) shows a 4ms delay between when VP and VN turn on. The 4ms time is an example delay to show the power-ON sequencing possibility through I<sup>2</sup>C. This delay is set between the separate I<sup>2</sup>C writes to set the enable bits in register 0x05. If both enable bits were set to '1' in the same I<sup>2</sup>C transaction (same byte), and ENN and ENP are HIGH, both VP and VN regulators start at the same time (when the data is latched at the Stop condition).

[Figure 23](#) shows a 2.5ms delay between the VP and VN turn off. The 2.5ms time is an example delay to show the power-OFF sequencing possibility using I<sup>2</sup>C.

[Figures 24](#) (zoom in) and [25](#) (zoom out) on [page 20](#) show a typical I<sup>2</sup>C data transfer to the ENABLE register. In this example, VP and VN regulators are enabled by writing data 0x07 to register address 0x05. The VP regulator is enabled first after the I<sup>2</sup>C Stop condition, followed by the VN regulator after the internal 2ms delay.

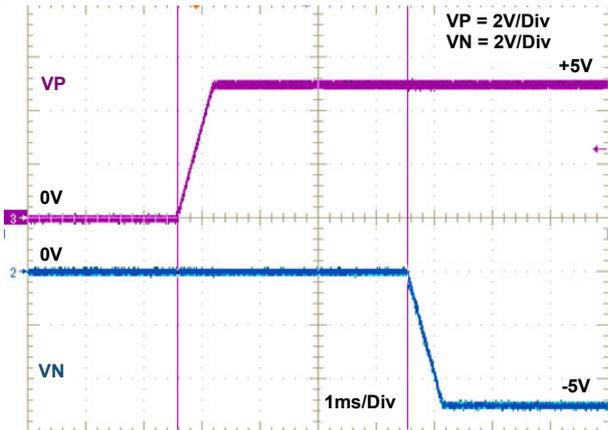


Figure 22. On-Sequence - I<sup>2</sup>C Control

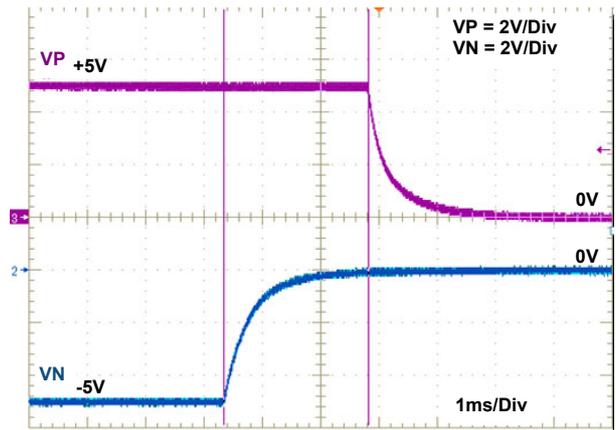


Figure 23. Off-Sequence - I<sup>2</sup>C Control

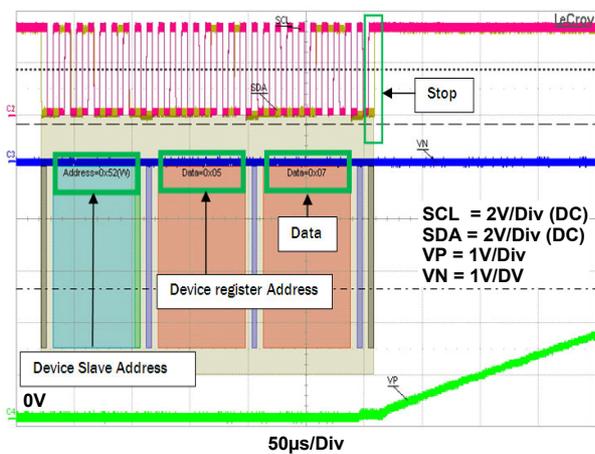


Figure 24. I<sup>2</sup>C Sequence and VP Response

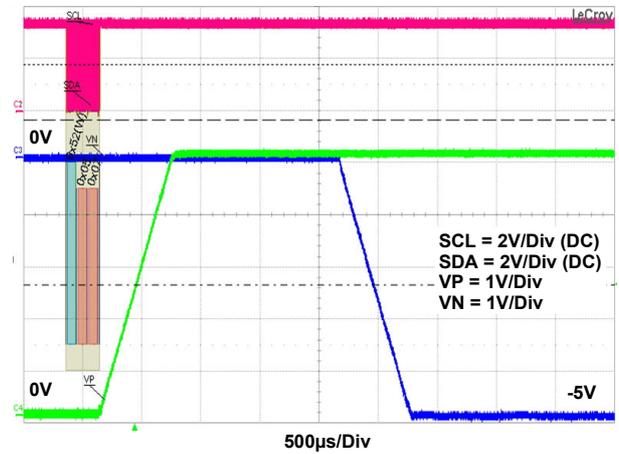


Figure 25. I<sup>2</sup>C Sequence and VP/VN Response

#### 4.14.2 Separate ENP and ENN pins (2 GPIO control)

Using two separate GPIO's, and controlling the timing between the ENP and ENN pins, the turn on/off events can be controlled. The method to control turn on/off by GPIO is valid when the respective enable bits in the ENABLE register at Register Address 0x05 are set to '1' (default). So, this method is used at IC power-ON (no I<sup>2</sup>C communication is required).

By design, the VN regulator turns on 2ms after the ENN signal goes HIGH.

[Figure 26 on page 21](#) shows a 5ms delay (example) between the ENP and ENN rise. VN turns on 2ms after ENN.

[Figure 27 on page 21](#) shows a 5ms delay (example) between the ENP and ENN fall.

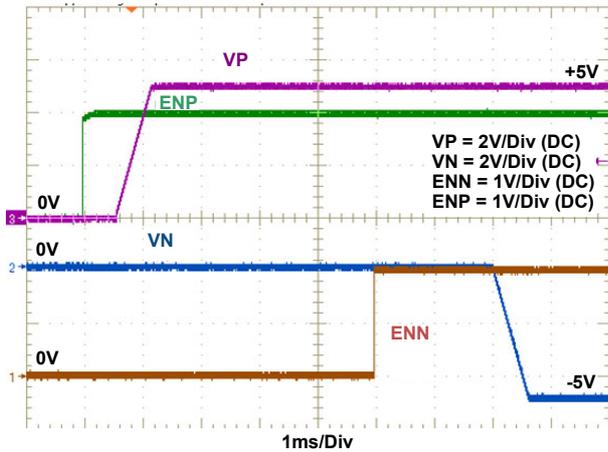


Figure 26. On Sequence - 2 GPIO Control

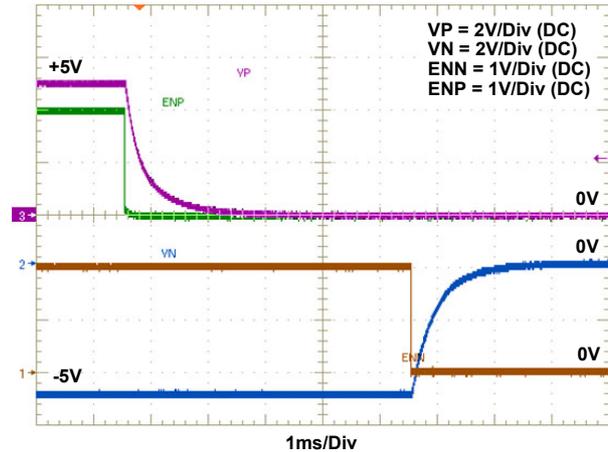


Figure 27. Off Sequence - 2 GPIO Control

### 4.14.3 Tie ENP and ENN together (1 GPIO control)

There is also an option to sequence the VN and VP regulators if there is only a single GPIO available in the system. The method to control turn on/off by GPIO is valid when the respective enable bits in the ENABLE register at Register Address 0x05 are set to '1' (default). So, this method is used at IC power-ON (no I<sup>2</sup>C communication is required).

If the ENP and ENN are tied together and both pulled HIGH, there is a default delay sequence in the IC. VP will come up first and after 2ms VN soft-starts. For turn off, both VN and VP start to shut down together, but the decay in the VP and VN voltage is controlled using the output capacitance value.

Figure 28 shows turn on when the ENN and ENP pins are tied together. There is a 2ms delay between VP and VN turning on.

Figure 29 shows turn off when the ENN and ENP are tied together.

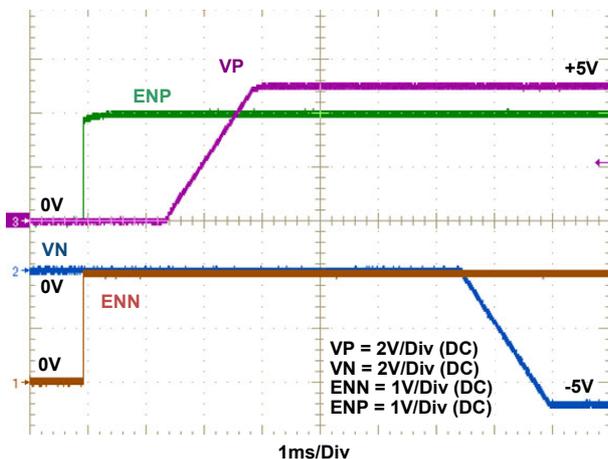


Figure 28. On Sequence - 1 GPIO Control

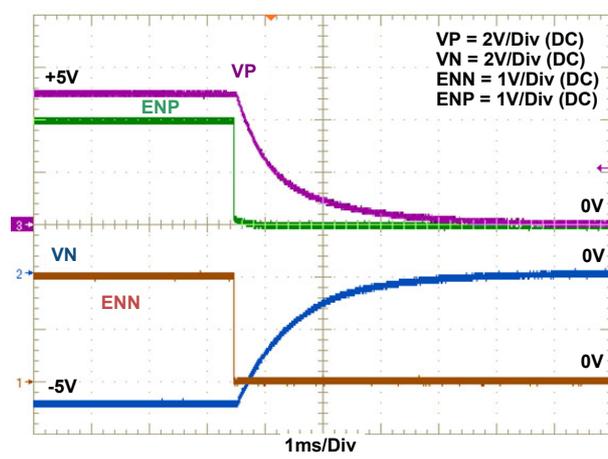


Figure 29. Off Sequence - 1 GPIO Control

### 4.15 VP Output Hi-Z Mode

The ISL98607 VP regulator can be configured in a Hi-Z mode for when the regulators are turned off. Using I<sup>2</sup>C, bit <b<sub>6</sub>> in the ENABLE register can be set to '1' to disable the internal pull-down resistor (this is Hi-Z Mode).

Configuring the VP regulator in Hi-Z mode prevents any leakage current flowing between VP and VN when the TFT-LCD is in sleep/standby mode, which minimizes the system power consumption.

## 4.16 Component Selection

The design of the boost converter is simplified by an internal compensation scheme, which allows easy system design without complicated calculations. Select component values using the following recommendations.

### 4.16.1 Input Capacitor

Renesas recommends that a 10µF X5R/X7R or equivalent ceramic capacitor is placed on the  $V_{IN}$  input supply.

### 4.16.2 Inductor

First, determine the minimum inductor saturation current required for the application.

The ISL98607 operates in Continuous Conduction Mode (CCM) at higher load current, and in Discontinuous Conduction Mode (DCM) and PFM mode at lighter loads.

In CCM, you can calculate the peak inductor current using [Equations 4](#) through [8](#).

Given these parameters:

- Input Voltage =  $V_{IN}$
- Output Voltage =  $V_O$
- Duty Cycle =  $D$
- Switching Frequency =  $f_{SW}$
- $t_{SW} = 1/f_{SW}$

Then the inductor ripple can be calculated as:

$$(EQ. 4) \quad \Delta I_{P-P} = (V_{IN}) * (D) / (L * f_{SW} * V_O)$$

where  $D = 1 - (V_{IN}/V_O)$ , then rewrite [Equation 4](#):

$$(EQ. 5) \quad \Delta I_{P-P} = (V_{IN}) * (V_O - V_{IN}) / (L * f_{SW} * V_O)$$

The average inductor current is equal to the average input current, where  $I_{IAVG}$  can be calculated from the efficiency of the converter.

$$(EQ. 6) \quad I_{IAVG} = (V_O * I_O) / (V_{IN} * \text{Efficiency})$$

To find the peak inductor current write the expression as:

$$(EQ. 7) \quad I_{PK} = \Delta I_{P-P} / 2 + I_{IAVG}$$

Substituting [Equations 5](#) and [6](#) in [Equation 7](#) calculates  $I_{PK}$ .

$$(EQ. 8) \quad I_{PK} = 0.5 * V_{IN} * (V_O - V_{IN}) / (L * f_{SW} * V_O) + (V_O * I_O) / (V_{IN} * \text{EFF})$$

Example:

Consider the following parameters in the steady-state boost regulator operating in CCM mode.

- $V_{IN} = 2.5V$
- $V_O = 5.3V$
- $f_{SW} = 1.45MHz$

- Output load current = 100mA
- Efficiency = 80%
- L = 2.2μH

Substituting previous parameters in [Equation 8](#) gives us:

$$I_{PK} = 453\text{mA}$$

The ISL98607 boost regulator operates in DCM and PFM mode at light load. In PFM mode, it uses a fixed peak inductor current of ~340mA.

To avoid the inductor core saturation, the saturation current of the inductor selected should be higher than the greater of the peak inductor current (for CCM) and the 340mA peak current in PFM mode.

The 340mA peak inductor current in PFM mode is optimized to provide maximum efficiency with a 2.2μH inductor value. If a smaller inductor is used, less energy is delivered per cycle, the ISL98607 switches at a higher frequency, and the efficiency reduces. Increasing the inductor increases the energy delivered per pulse. However, for a given inductor size the DC-resistance (DCR) increases with inductor value, so the conduction losses increase. L = 2.2μH is the optimal value for ISL98607.

[Table 3](#) shows the recommended inductors for typical ISL98607 applications (small size, handheld TFT-LCD display power).

**Table 3. Recommended Inductors**

Inductor Part Number	Inductance (μH)	DCR (mΩ)	I <sub>SAT</sub> (A)	Footprint Size
VLF302510MT-2R2M (TDK)	2.2	70	1.23	3025
DFE252012C (Toko)	2.2	90	2.00	2520
TFM201610G-2R2M (TDK)	2.2	150	1.20	2016

### 4.16.3 Output Capacitor

The output capacitor supplies current to the load during transient conditions, and reduces the ripple voltage at the output. Output ripple voltage consists of two components:

- The voltage drop due to the inductor ripple current flowing through the ESR of the output capacitor.
- Charging and discharging of the output capacitor.

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient. The effective capacitance reduces (derates) as the operating voltage/bias increases. Always see the manufacture's derating information to determine effective capacitance for the operating conditions.

The effective capacitance at the nominal output voltage should be 2.2μF for VBST and VP regulator, and 4.4μF for VN. Renesas recommends using a 10μF X5R 10V or equivalent ceramic output capacitor for both VBST and VP outputs to provide a minimum of 2.2μF effective capacitance. For the VN output, Renesas recommends use one or two 10μF X5R 10V or equivalent ceramic output capacitors. Using two VN output capacitors results in <50mV peak-to-peak output voltage ripple with input voltages from 2.8V to 4.4V.

**Table 4. Recommended Output Capacitors**

Capacitor Part Number	Value (μF)	Size	Quantity
GRM155R61A106ME11 (Murata)	10	0402	x5: C <sub>IN</sub> , C <sub>VBST</sub> , C <sub>VP</sub> , C <sub>VN</sub> , C <sub>CP</sub> x1: C <sub>VN</sub> (x2 for minimum ripple)
GRM188R61C475KAAJ (Murata)	4.7	0603	x5: C <sub>IN</sub> , C <sub>VBST</sub> , C <sub>VP</sub> , C <sub>VN</sub> , C <sub>CP</sub> x1: C <sub>VN</sub> (x2 for minimum ripple)

## 5. General Layout Guidelines

When designing the printed circuit board (PCB) layout for the ISL98607, it is very important to understand the power requirements of the system. Some general best practices should be adhered to create an optimal PCB layout:

1. Careful consideration should be taken with any traces carrying AC signals. Keep AC current loops as short and as tight as possible. The current loop generates a magnetic field, which can couple to another conductor, inducing unwanted voltage. Place components such that current flows through them in a straight line as much as possible, which helps reduce the loop sizes and the EMI from the PCB.
2. If trace lengths are long, the resistance of the trace increases, can cause some reduction in IC efficiency, and cause system instability. Make the traces carrying power wide and short.
3. In discontinuous conduction mode, the direction of the current is interrupted every few cycles. This may result in large  $di/dt$  (transient load current). When injected in the ground plane the current may cause voltage drops, which can interfere with sensitive circuitry. Connect the analog ground and power ground of the IC very close to the IC to mitigate this issue.
4. One plane/layer in the PCB is recommended to be a dedicated ground plane. A large area of metal will have lower resistance, which reduces the return current impedance. More ground plane area minimizes parasitics and avoids corruption of the ground reference.
5. Isolate low frequency digital signals from any high frequency signals generated by switching frequency and harmonics. PCB traces should not cross each other. If they must cross due to the layout restriction, they must cross perpendicularly to reduce the magnetic field interaction.
6. The amount of copper that should be poured (thickness) depends upon the power requirement of the system. Insufficient copper increases resistance of the PCB, which increases heat dissipation.
7. Generally, vias should not be used to route high current paths.
8. While designing the layout of switched controllers, do not use the auto routing function of the PCB layout software. Auto routing connects the nets with same electrical name and does not account for ideal trace lengths and positioning.

### 5.1 ISL98607 Specific Layout Guidelines

1. Connect the input capacitor to the VIN pin with the smallest trace possible. This helps reject high frequency disturbances and promotes good regulation of the VBST, VP, and VN regulators.
2. Connect the boost inductor to the LXP pin with a short and wide trace. Careful consideration should be made in selecting the inductor as it may cause electromagnetic interference, which could affect IC functionality. A shielded inductor is recommended.
3. The device has VBST and VBSTCP pins. VBST is the output of the boost regulator and VBSTCP is the input for the negative charge pump. Connect and short VBST and VBSTCP to each other on the PCB with a short and thick trace to avoid parasitic inductance and resistance. A  $10\mu\text{F}/10\text{V}$  capacitor should be used on VBST. The distance of the capacitor from the VBST and VBSTCP pin is critical (it should be placed very close to the IC with a short and thick trace).
4. Renesas highly recommends that VN and VSUB are shorted together with a short and thick trace. It is recommended that  $2 \times 10\mu\text{F}/10\text{V}$  capacitors are placed on VN to minimize output ripple. Additionally, it helps minimize noise that may be coupled from the high-frequency ripple of the charge pump.
5. The VP regulator has two output pins (VP). Connect both pins directly with a short and thick trace.
6. Connect the IC Analog ground (AGND) and power ground (PGND) to each other. It is crucial to connect/short these two grounds very close to the IC.
7. Isolate the digital input pins, ENN and ENP, from the high  $di/dt$  and  $dv/dt$  signals. Otherwise, it may cause a glitch on those inputs.
8. I<sup>2</sup>C signals, if not used, should be tied to VIN.

Figures 30 and 31 show the recommended PCB layout for a typical ISL98607 application.

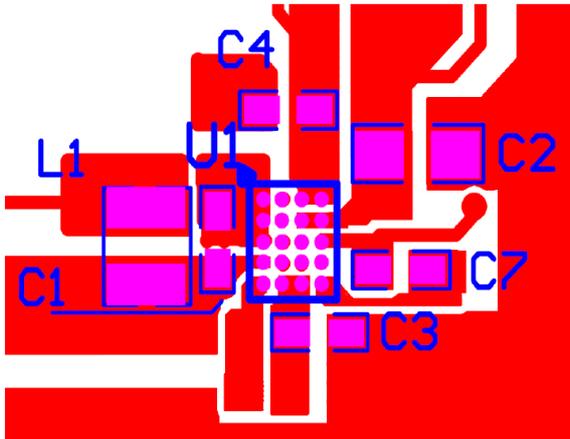


Figure 30. ISL98607EIAZ Recommended PCB Layout

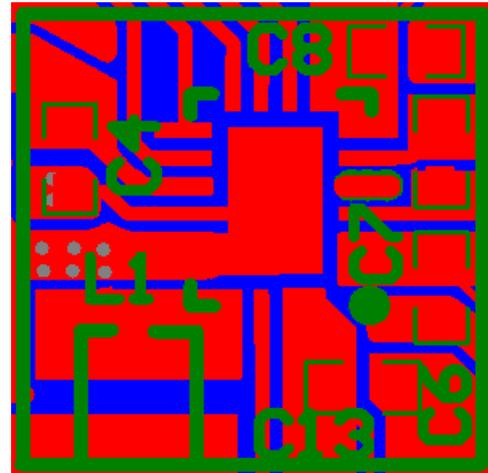


Figure 31. ISL98607IRTZ Recommended PCB Layout

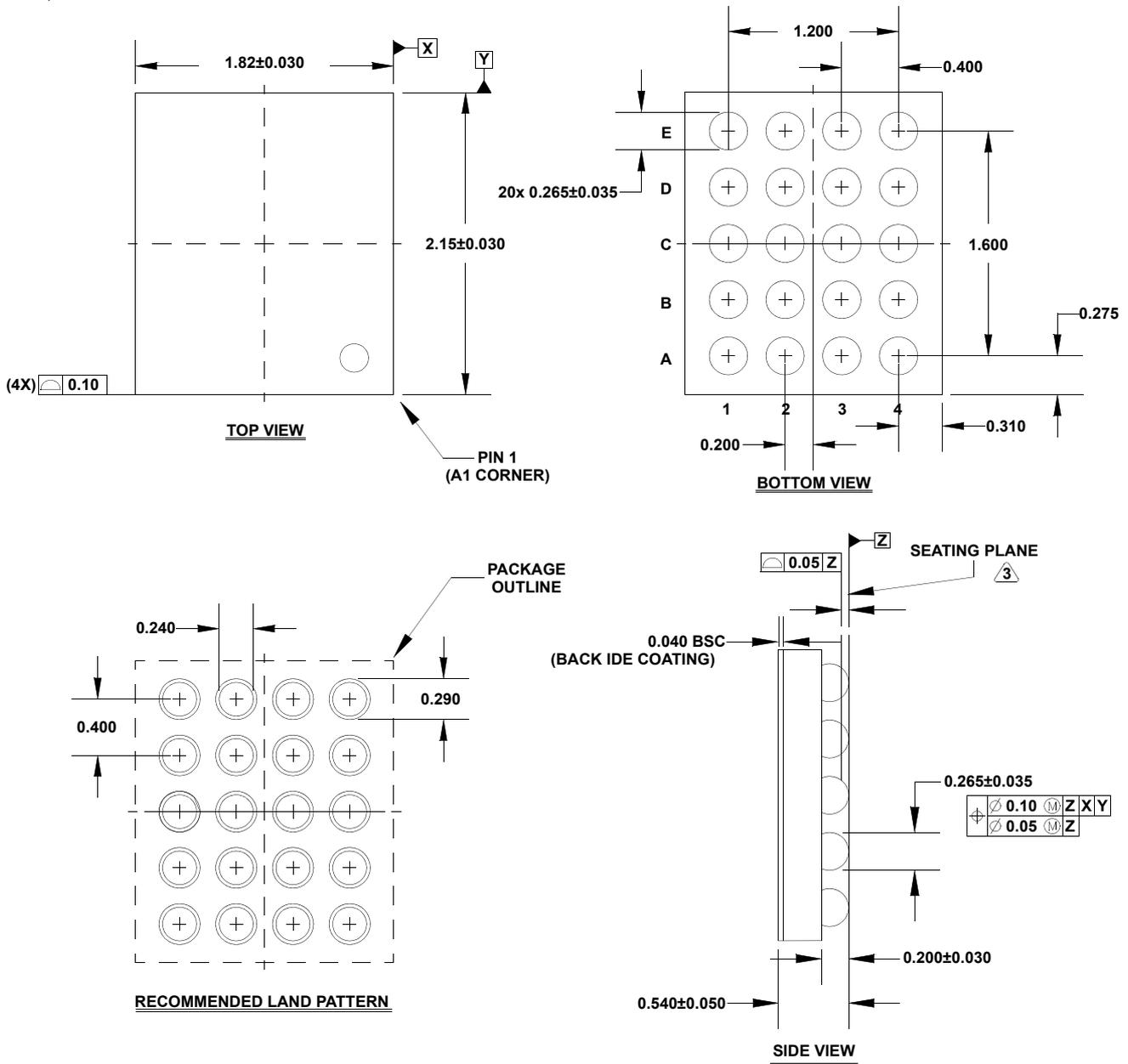
## 6. Revision History

Rev.	Date	Description
1.00	Jun.3.19	Applied new template and formatting. Added Related Literature section. Added ISL98607IRTZ information throughout datasheet. Updated disclaimer.
0.00	Mar.8.13	Initial release

# 7. Package Outline Drawings

For the most recent package outline drawing, see [W4x5.20E](#).

W4x5.20E  
 20 Ball Wafer Level Chip Scale Package (WLCSP) (BSC)  
 Rev 1, 1/13

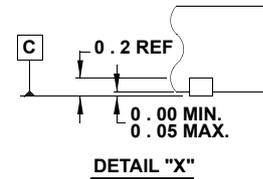
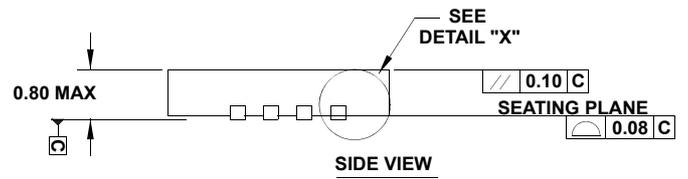
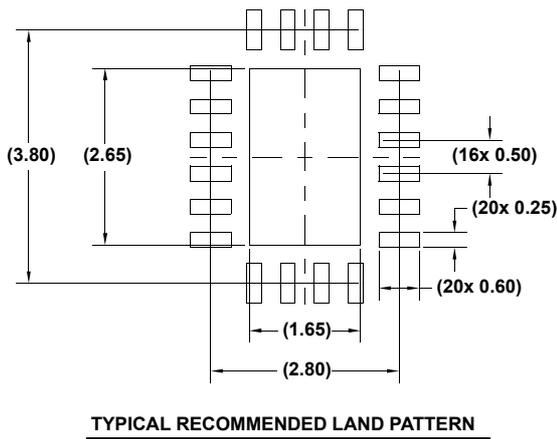
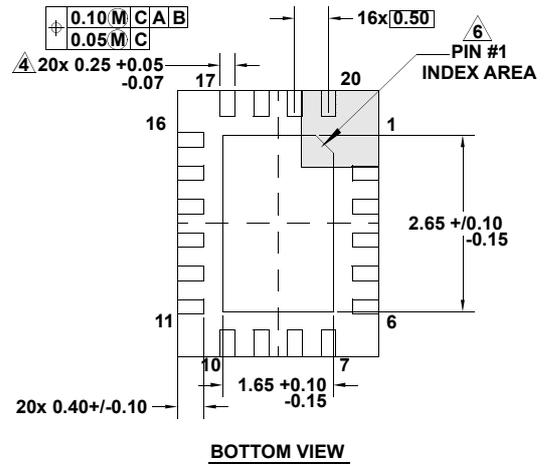
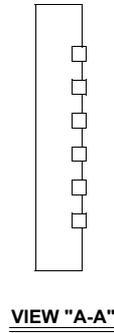
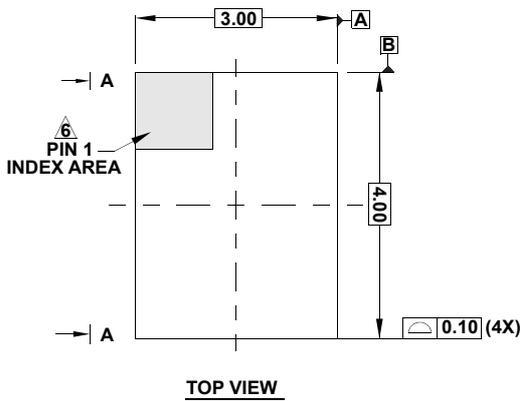


**NOTES:**

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. There shall be a minimum clearance of 0.10mm between the edge of the bump and the body edge.

L20.3x4A  
 20 Lead Thin Quad Flat No-Lead Plastic Package  
 Rev 0, 6/10

For the most recent package outline drawing, see [L20.3x4A](#).



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220VEGD-NJI.

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