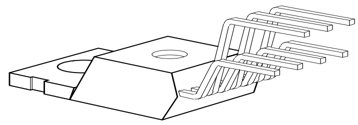
SIEMENS

5-V Low-Drop Voltage Regulator TLE 4267

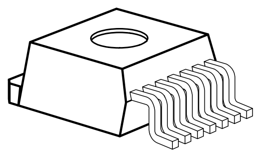
Bipolar IC

Features

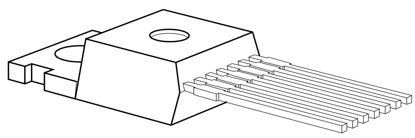
- Output voltage tolerance ≤ ± 2 %
- Low-drop voltage
- Very low standby current consumption
- Input voltage up to 40 V
- Overvoltage protection up to 60 V (≤ 400 ms)
- Reset function down to 1 V output voltage
- ESD protection up to 2000 V
- Adjustable reset time
- On/off logic
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Wide temperature range
- Suitable for use in automotive electronics



P-TO220-7-3



P-TO220-7-180



P-TO220-7-230

Type	Ordering Code	Package
TLE 4267	Q67000-A9153	P-TO220-7-3
TLE 4267 G	Q67006-A9169	P-TO220-7-180 (SMD)
TLE 4267 S	Q67000-A9246	P-TO220-7-230

Functional Description

TLE 4267 is a 5-V low-drop voltage regulator in a TO220-7 package. It supplies an output current of > 400 mA. The IC is shortcircuit-proof and incorporates temperature protection that disables the IC at overtemperature.

Application

The IC regulates an input voltage V_I in the range 5.5 V < V_I < 40 V to V_{Qrated} = 5.0 V. A reset signal is generated for an output voltage V_Q of < 4.5 V. The reset delay can be set with an external capacitor. The device has two logic inputs. It is turned-ON by a voltage of > 4 V on E2 by the ignition for example. It remains active as a function of the voltage on E6, even if the voltage on E2 goes Low. This makes it possible to implement a self-holding circuit without external components. When the device is turned-OFF, the output voltage drops to 0 V and current consumption tends towards 0 µA.

Design Notes for External Components

The input capacitor C_I is necessary for compensation line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with C_I. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values of ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range.

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturating of the power element.

A comparator in the reset-generator block compares a reference that is independent of the input voltage to the scaled-down output voltage. If this reaches a value of 4.5 V, the reset-delay capacitor is discharged and then the reset output is set Low. As the output voltage increases again, the reset-delay capacitor is charged with constant current from V_Q = 4.5 V onwards. When the capacitor voltage reaches the upper switching threshold, reset goes High again. The reset delay can be set within wide range by selection of the external capacitor.

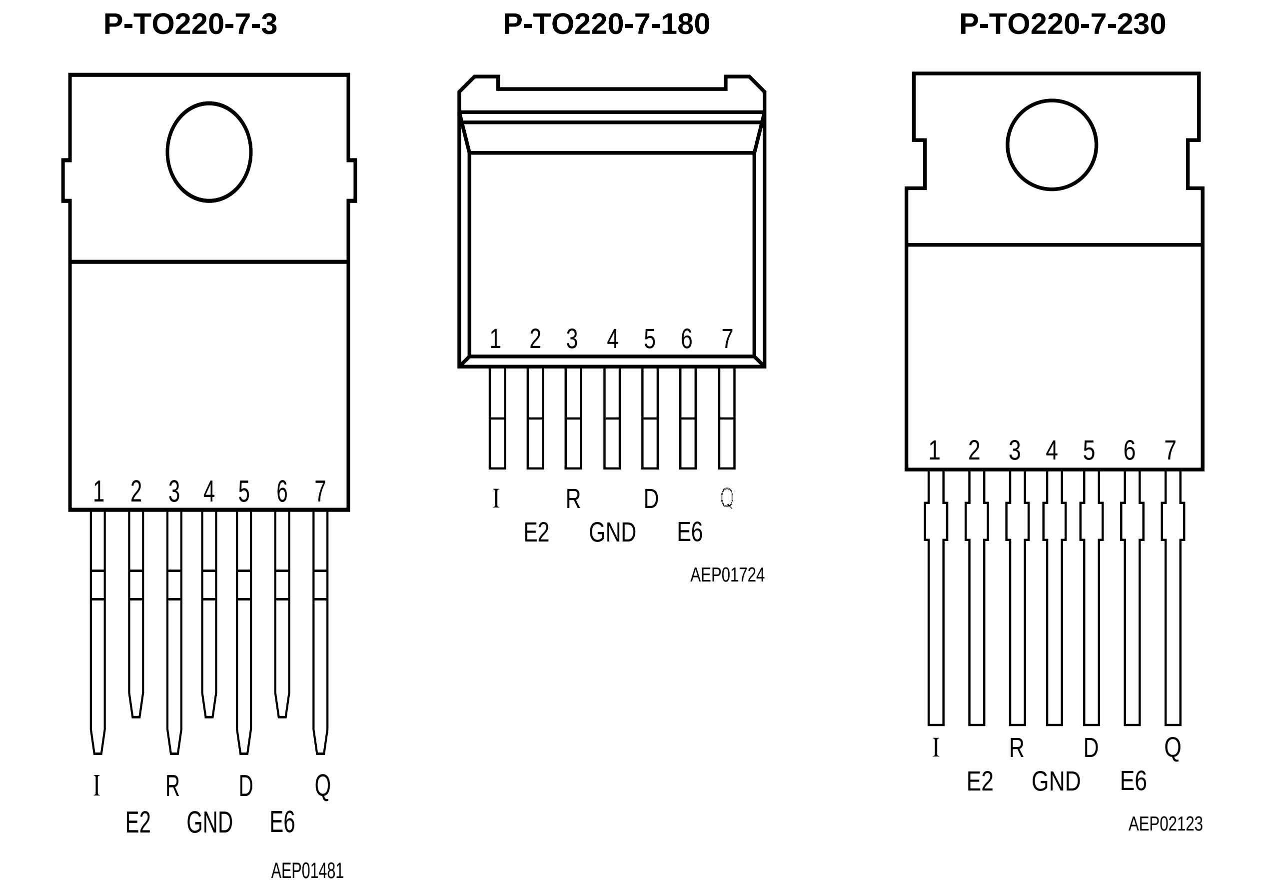
With the integrated turn-ON/turn-OFF logic it is simple to implement delayed turn-OFF without external components.

Truth Table for Turn-ON/Turn-OFF Logic

Pin 2	Pin 6	V_Q	Remarks
L	X	OFF	Initial state, pin 6 internally pulled up
H	X	ON	Regulator switched on via pin 2, by ignition for example
H	L	ON	Pin 6 clamped active to ground by controller while pin 2 is still high
X	L	ON	Previous state remains, even ignition is shut off: self-holding state
L	L	ON	Ignition shut off while regulator is in self-holding state
L	H	OFF	Regulator shut down by releasing of pin 6 while pin 2 remains Low, final state. No active clamping required by external self-holding circuit (µC) to keep regulator shut off.

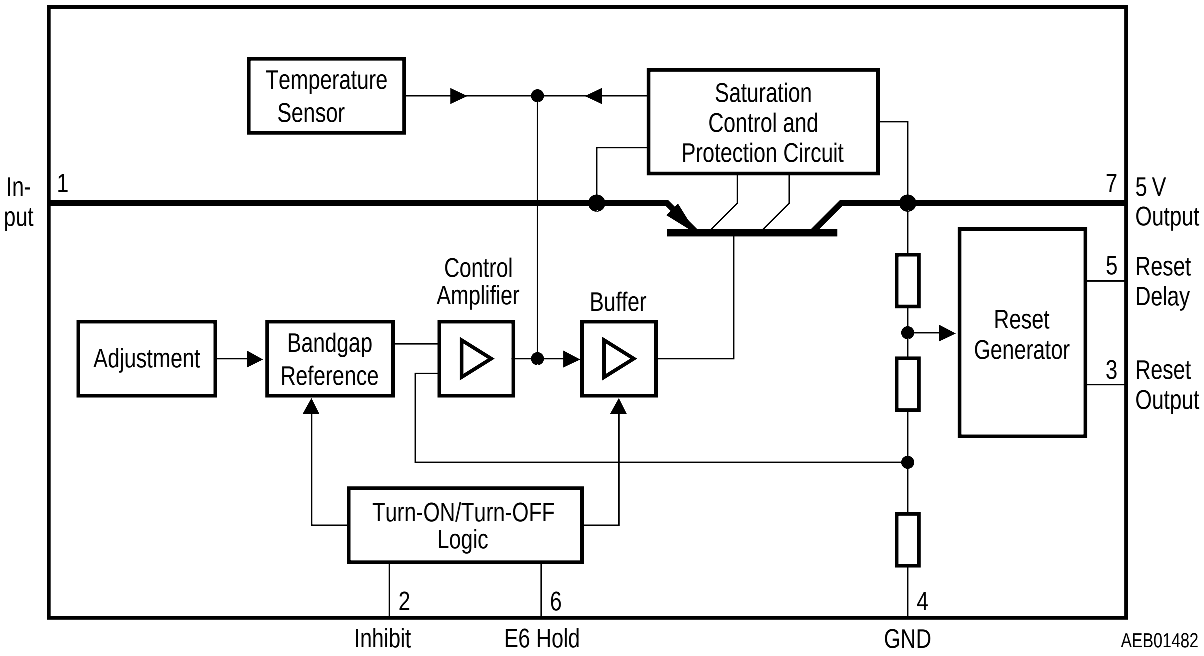
Pin 2: (Inhibit, E2) Enable function, active High
Pin 6: (Hold, E6) Hold and release function, active Low

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	I	**Input;** block to ground directly at the IC by a ceramic capacitor
2	E2	**Inhibit;** device is turned-ON by High signal on this pin; internal pulldown resistor of 100 kΩ
3	R	**Reset Output;** open-collector output internally connected to the output via a resistor of 30 kΩ
4	GND	**Ground;** connected to rear of chip
5	D	**Reset Delay;** connect with capacitor to GND for setting delay
6	E6	**Hold;** see truth table above for function; this input is connected to output voltage across pullup resistor of 50 kΩ
7	Q	**5-V Output;** block to GND with 22-µF capacitor, ESR < 3 Ω



Block Diagram

Absolute Maximum Ratings

T_J = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input					
Voltage	V_I	– 42	42	V	–
Voltage	V_I	–	60	V	$t \leq$ 400 ms
Current	I_I	–	–	–	Limited internally
Reset Output					
Voltage	V_R	– 0.3	7	V	–
Current	I_R	–	–	–	Limited internally
Reset Delay					
Voltage	V_d	– 0.3	42	V	–

Absolute Maximum Ratings (cont'd)

T_J = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Current	I_d	–	–	–	–
Output					
Voltage	V_Q	– 0.3	7	V	–
Current	I_Q	–	–	–	Limited internally
Inhibit					
Voltage	V_{E2}	– 42	42	V	
Current	I_{E2}	– 5	5	mA	$t \leq$ 400 ms
Hold					
Voltage	V_{E6}	– 0.3	7	V	–
Current	I_{E6}	–	–	mA	Limited internally
GND					
Current	I_{GND}	– 0.5	–	A	–
Temperatures					
Junction temperature	T_J	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input voltage	V_I	5.5	40	V	see diagram
Junction temperature	T_J	– 40	150	°C	–
Thermal Resistance					
Junction ambient	R_{thja}	–	70	K/W	–
Junction-case	R_{thjc}	–	6	K/W	–
Junction-case	R_{thjc}	–	2	K/W	t < 1 ms

Characteristics

V_I = 13.5 V; – 40 °C < T_J < 125 °C; V_{E2} > 4 V (unless specified otherwise)

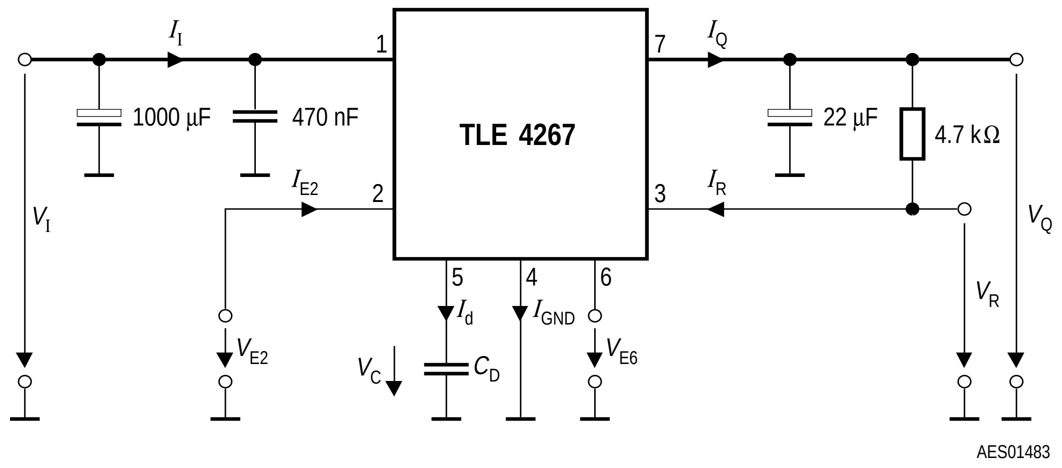
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage	V_Q	4.9	5	5.1	V	5 mA ≤ I_Q ≤ 400 mA 6 V ≤ V_I ≤ 26 V
Output voltage	V_Q	4.9	5	5.1	V	5 mA ≤ I_Q ≤ 150 mA 6 V ≤ V_I ≤ 40 V
Output-current limiting	I_Q	500	–	–	mA	T_J = 25 °C
Current consumption $I_q = I_I - I_Q$	I_q	–	–	50	µA	Regulator-OFF
Current consumption $I_q = I_I - I_Q$	I_q	–	1.0	10	µA	T_J = 25 °C IC turned off
Current consumption $I_q = I_I - I_Q$	I_q	–	1.3	4	mA	I_Q = 5 mA IC turned on
Current consumption $I_q = I_I - I_Q$	I_q	–	–	60	mA	I_Q = 400 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	–	80	mA	I_Q = 400 mA V_I = 5 V
Drop voltage	V_{Dr}	–	0.3	0.6	V	I_Q = 400 mA[1)]
Load regulation	ΔV_Q	–	–	50	mV	5 mA ≤ I_Q ≤ 400 mA
Supply-voltage regulation	ΔV_Q	–	15	25	mV	V_I = 6 to 36 V; I_Q = 5 mA
Supply-voltage rejection	SVR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 V_{pp}
Longterm stability	ΔV_Q	–	0	–	mV	1000 h

1) Drop voltage = $V_I - V_Q$ (measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V)

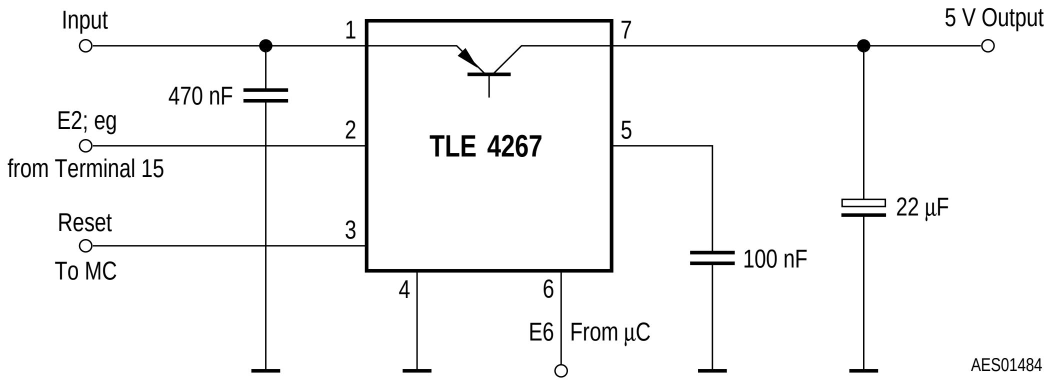
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reset Generator						
Switching threshold	V_{rt}	4.2	4.5	4.8	V	–
Reset High level	–	4.5	–	–	V	$R_{ext} = \infty$
Saturation voltage	V_R	–	0.1	0.4	V	R_R = 4.7 kΩ [1)]
Pullup	R_R	–	30	–	kΩ	–
Saturation voltage	$V_{D,sat}$	–	50	100	mV	$V_Q < V_{RT}$
Charge current	I_d	8	15	25	µA	V_D = 1.5 V
Delay switching threshold	V_{dt}	2.6	3	3.3	V	–
Delay	t_d	–	20	–	ms	C_d = 100 nF
Switching threshold	V_{st}	–	0.43	–	V	–
Delay	t_t	–	2	–	µs	C_d = 100 nF
Inhibit						
Turn-ON voltage	V_{E2}	–	3	4	V	IC turned-ON
Turn-OFF voltage	V_{E2}	2	–	–	V	IC turned-OFF
Pulldown	R_{E2}	50	100	200	kΩ	–
Hysteresis	ΔV_{E2}	0.2	0.5	0.8	V	–
Input current	I_{E2}	–	35	100	µA	V_{IP2} = 4 V
Holding voltage	V_{E6}	30	35	40	%	Referred to V_Q
Turn-OFF voltage	V_{E6}	60	70	80	%	Referred to V_Q
Pullup	R_{E6}	20	50	100	kΩ	–
Overvoltage Protection						
Turn-OFF voltage	$V_{i,ov}$	42	44	46	V	–
Turn-ON hysteresis	$\Delta V_{i,ov}$	2	–	6	V	–

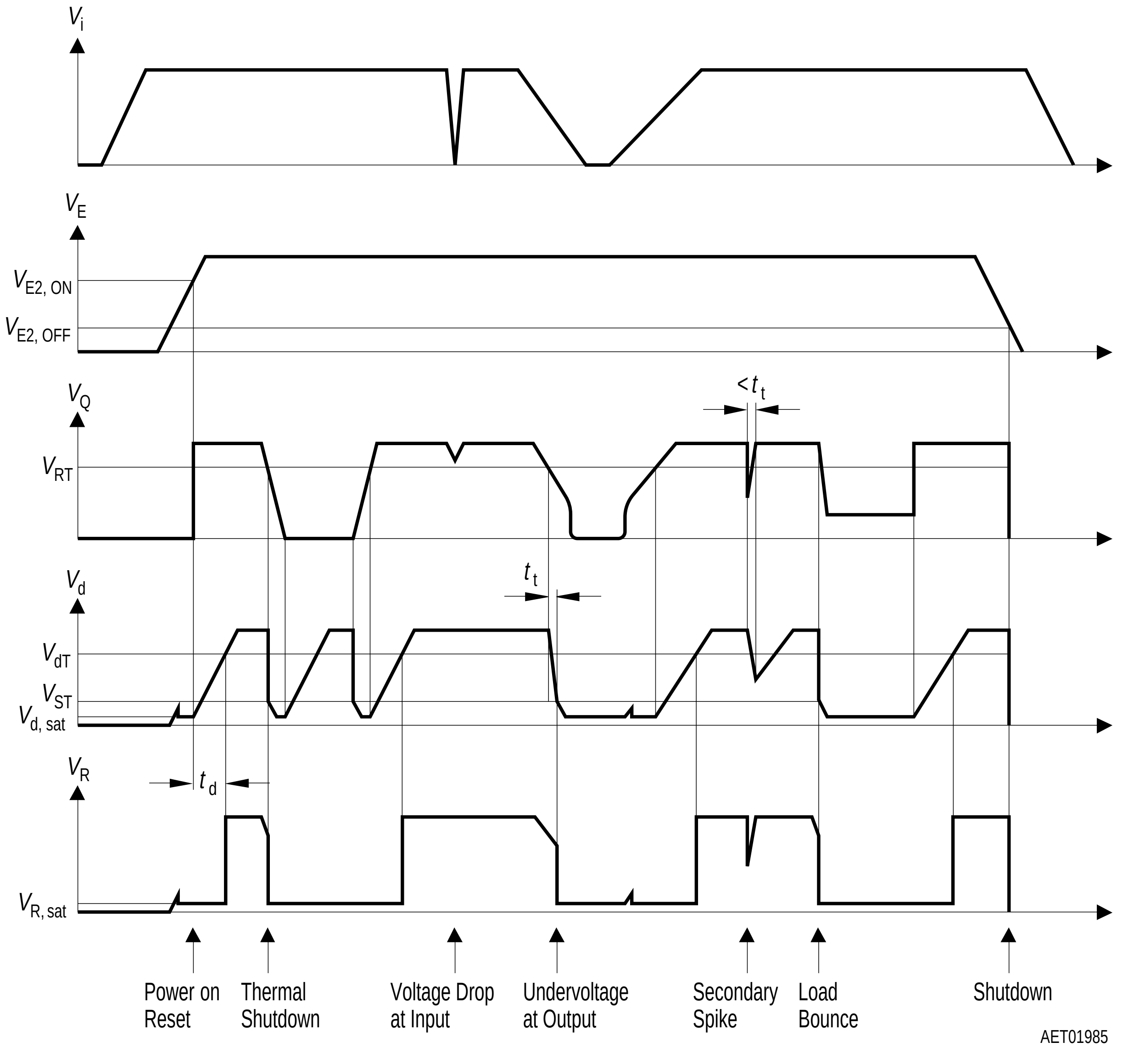
1) The reset output is Low between V_Q = 1 V and V_{RT}



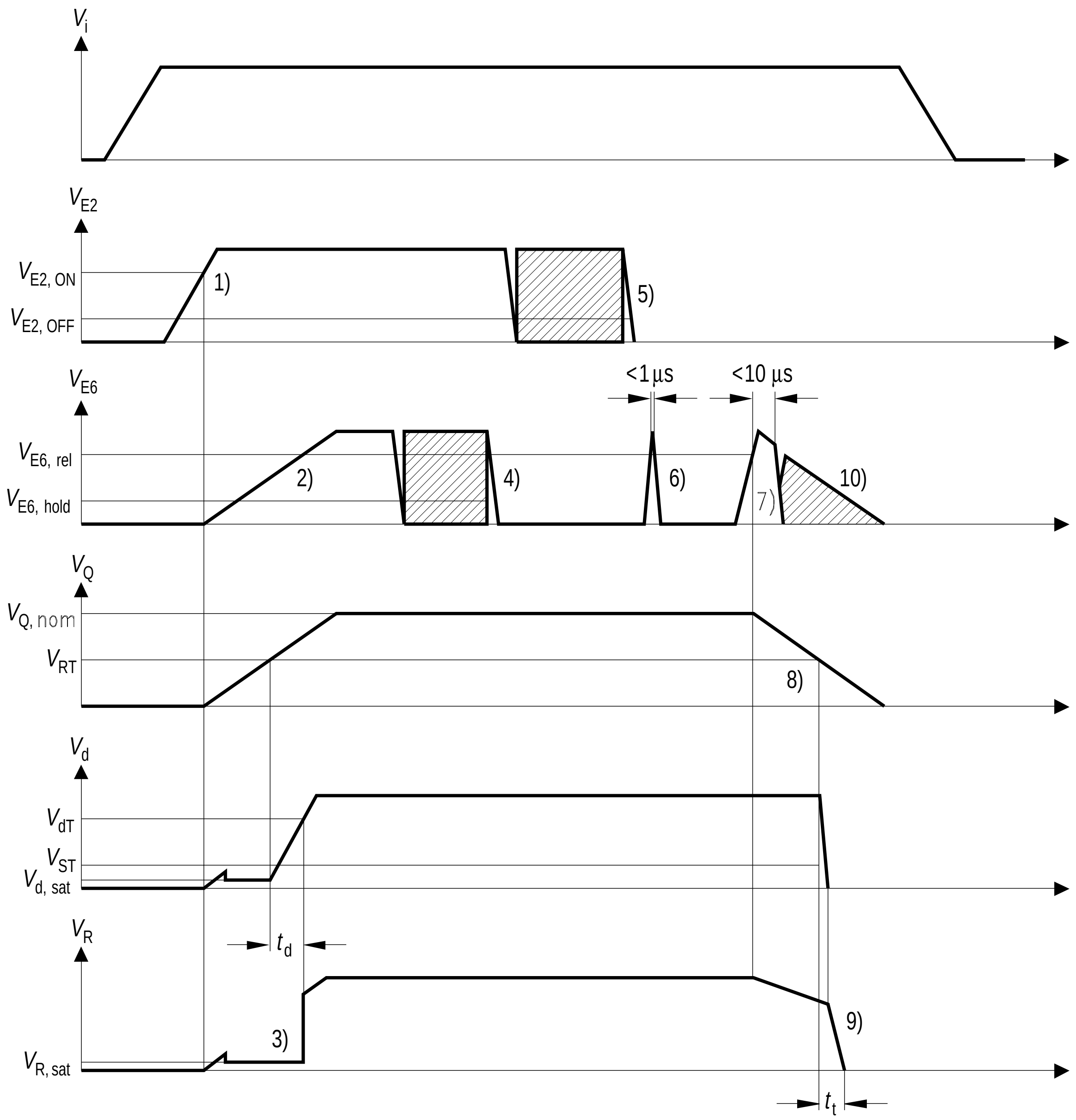
Test Circuit



Application Circuit



Time Response



1) Enable active
2) Hold inactive, pulled up by V_Q
3) Power-ON reset
4) Hold active, clamped to GND by external µC
5) Enable inactive, clamped by int. pull-down resistor
6) Pulse width smaller than 1 µs
7) Hold inactive, released by µC
8) Voltage controller shutdown
9) Output-low reset
10) No switch on via V_{E6} possible after E6 was released to $V_{E6} > V_{E6, rel}$ for more than 4 µs

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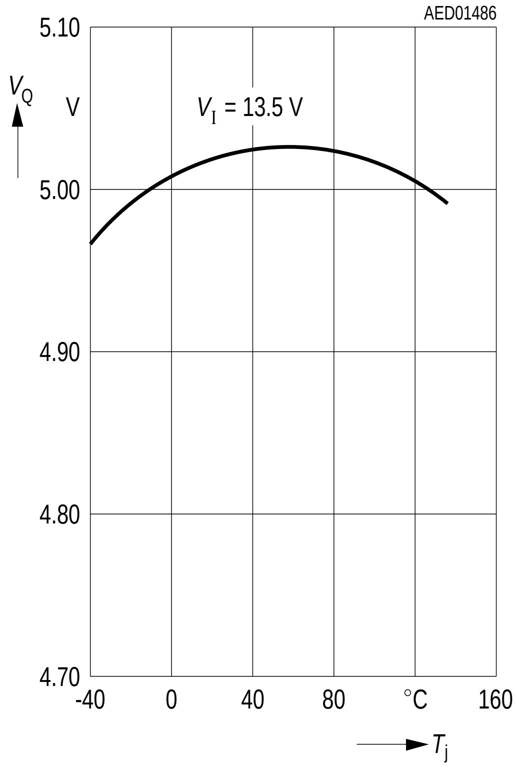
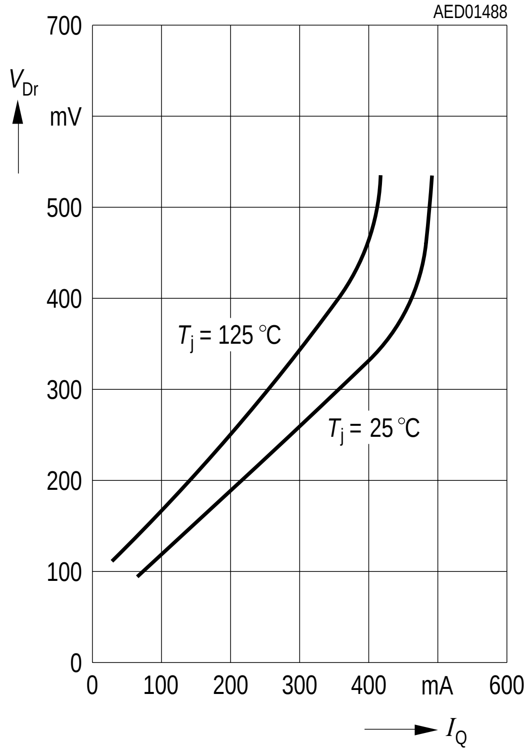
Enable and Hold Behaviour

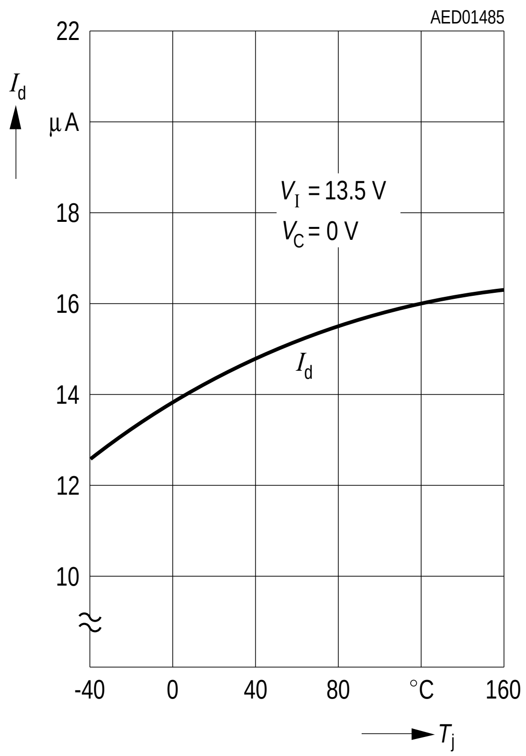
Output Voltage V_Q versus Temperature T_j



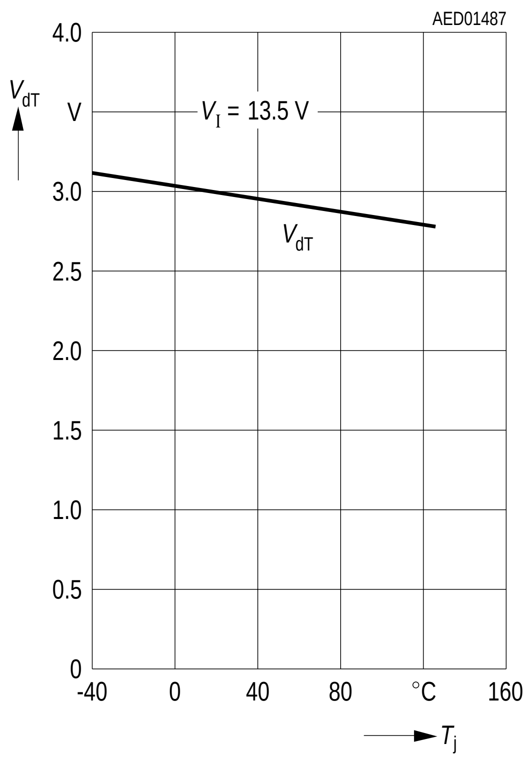
Drop Voltage V_{Dr} versus Output Current I_Q



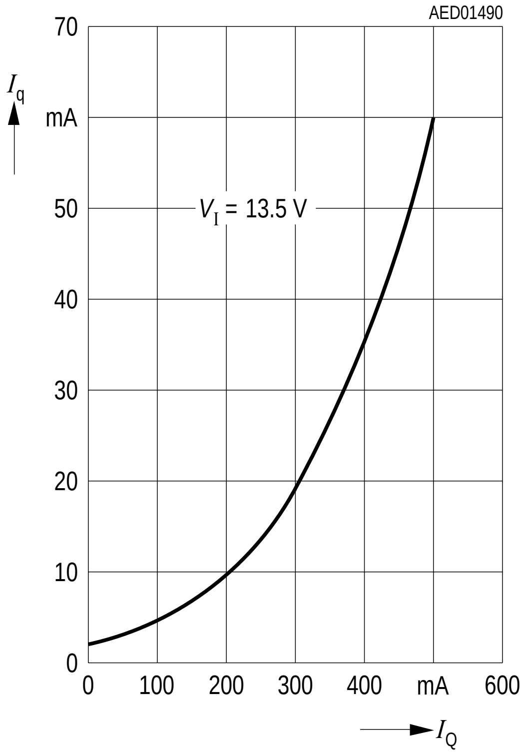
Charge Current I_d versus Temperature T_j



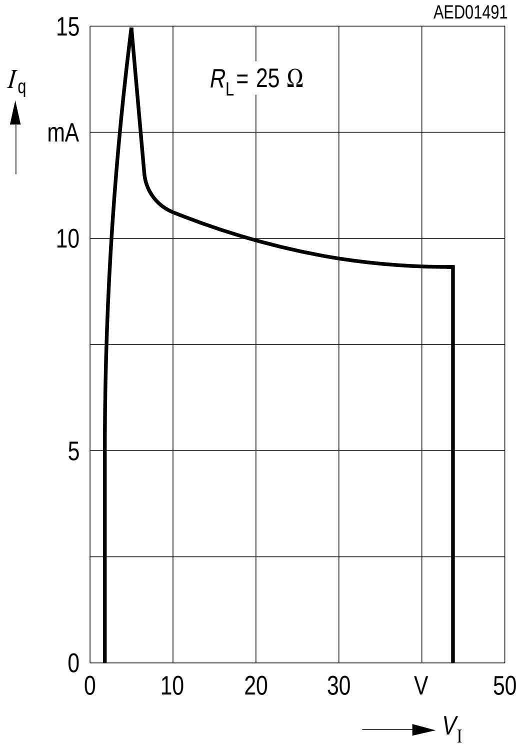
Delay Switching Threshold V_{dT} versus Temperature T_j



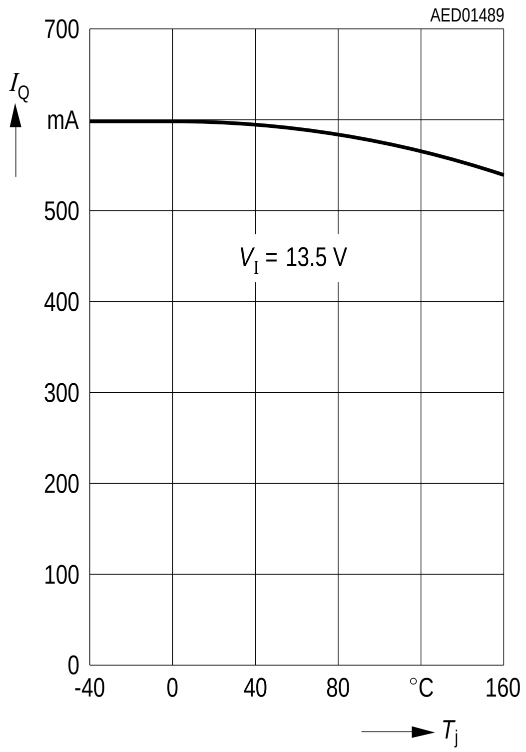
Current Consumption I_q versus Output Current I_Q



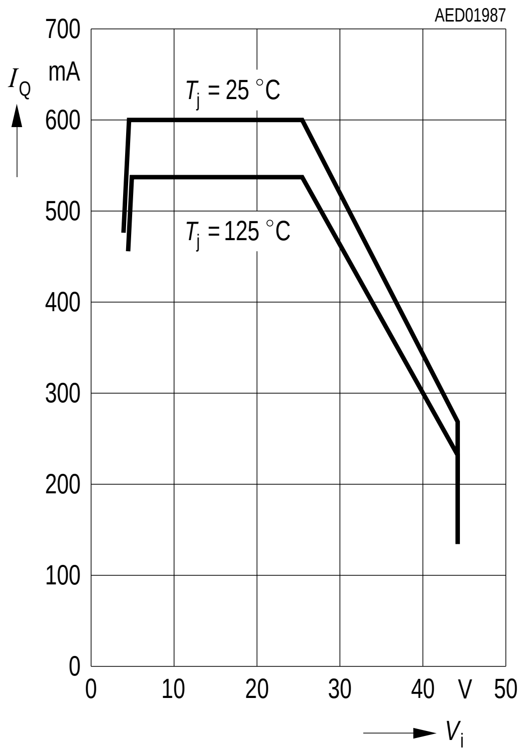
Current Consumption I_q versus Input Voltage V_I



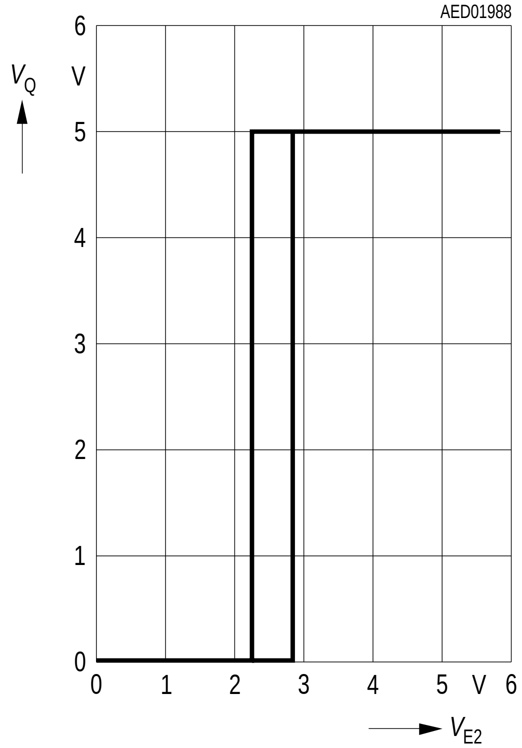
Output Current I_Q versus Temperature T_j



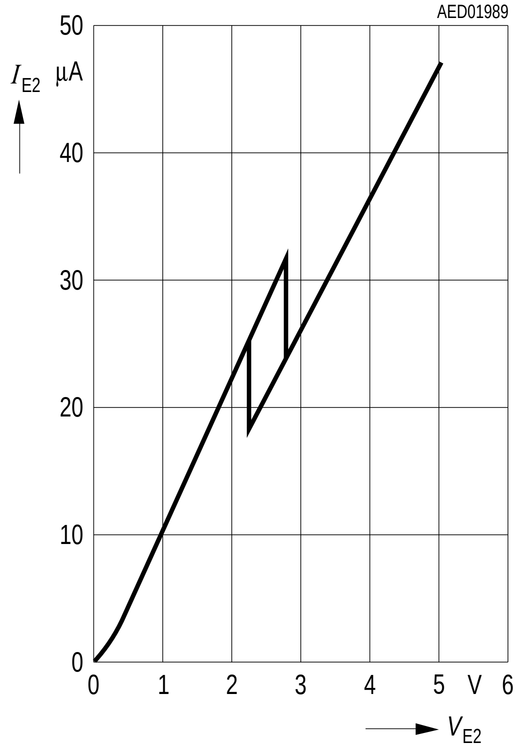
Output Current I_Q versus Input Voltage V_I



Output Voltage V_Q versus Inhibit Voltage V_{E2}

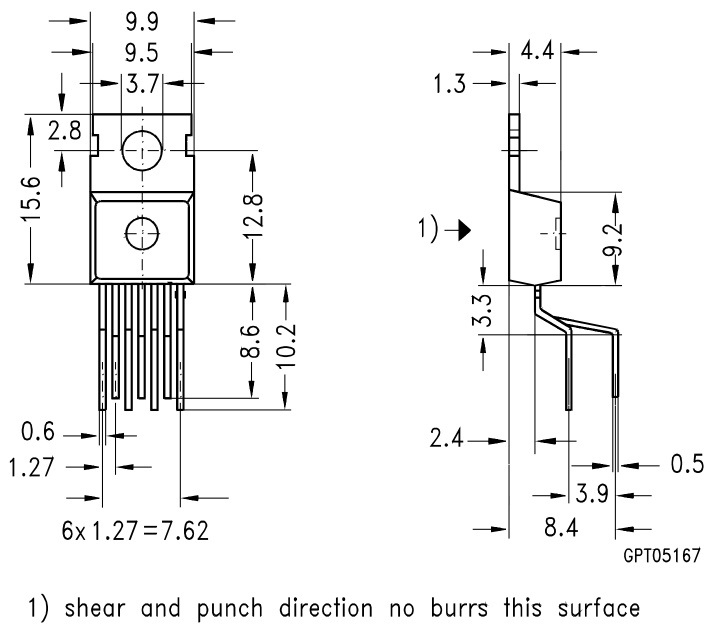


Inhibit Current I_{E2} versus Inhibit Voltage V_{E2}



Package Outlines

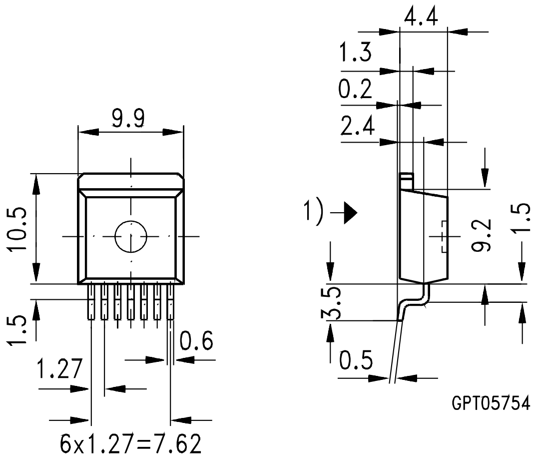
P-TO220-7-3
(Plastic Transistor Single Outline)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

Dimensions in mm

P-TO220-7-180
(Plastic Transistor Single Outline)



1) shear and punch direction no burrs this surface

Sorts of Packing
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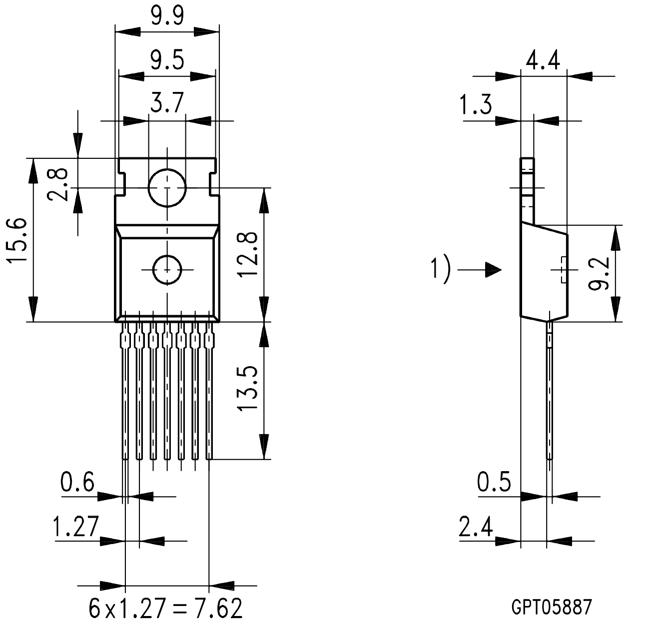
SMD = Surface Mounted Device

Dimensions in mm

P-TO220-7-230
(Plastic Transistor Single Outline)



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Dimensions in mm