SUPPLEMENT

Am29F010 Known Good Die

1 Megabit (128 K x 8-Bit)

CMOS 5.0 Volt-only, Uniform Sector Flash Memory—Die Revision 1

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — 5.0 V ± 10% for read, erase, and program operations
  - — Simplifies system-level power requirements
- **High performance**
  - — 90 or 120 ns maximum access time
- **Low power consumption**
  - — 30 mA max active read current
  - — 50 mA max program/erase current
  - — <25 µA typical standby current
- **Flexible sector architecture**
  - — Eight uniform sectors
  - — Any combination of sectors can be erased
  - — Supports full chip erase
- **Sector protection**
  - — Hardware-based feature that disables/re-enables program and erase operations in any combination of sectors
  - — Sector protection/unprotection can be implemented using standard PROM programming equipment
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically pre-programs and erases the chip or any combination of designated sector
  - — Embedded Program algorithm automatically programs and verifies data at specified address
- **Minimum 100,000 program/erase cycles guaranteed**
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash
  - — Superior inadvertent write protection
- **Data Polling and Toggle Bits**
  - — Provides a software method of detecting program or erase cycle completion
- **Tested to datasheet specifications at temperature**
- **Quality and reliability levels equivalent to standard packaged components**

1/13/98

Publication# **21116** Rev: **B** Amendment/**0**
Issue Date: **January 1998**

GENERAL DESCRIPTION

The Am29F010 in Known Good Die (KGD) form is a 1 Mbit, 5.0 Volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29F010 Features

The Am29F010 device is organized as eight uniform sectors of 16 Kbytes each for flexible erase capability. This device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. A power supply providing 12.0 Volt V_{PP} is not required for program or erase operations.

The Am29F010 in KGD form offers access times of 90 ns and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This invokes the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This invokes the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is erased when shipped from the factory.

The **hardware data protection** measures include a low V_{CC} detector automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory, and is implemented using standard EPROM programmers.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

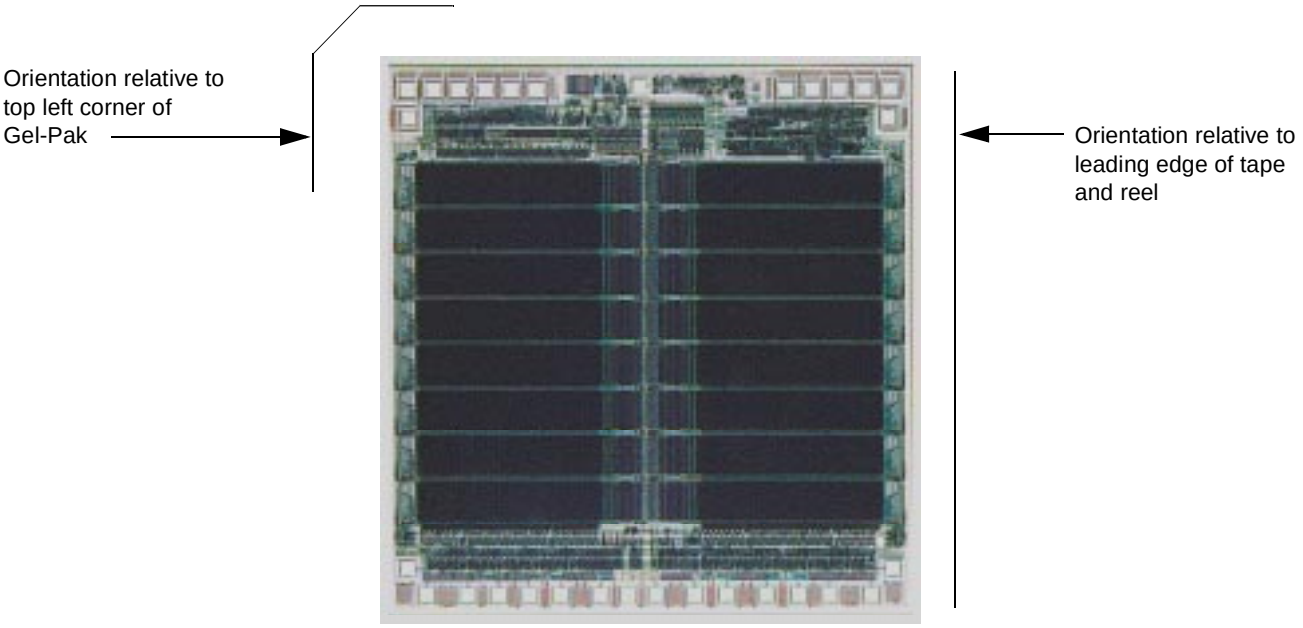
ELECTRICAL SPECIFICATIONS

Refer to the Am29F010 data sheet, publication number 16736, for full electrical specifications for the Am29F010 in KGD form.

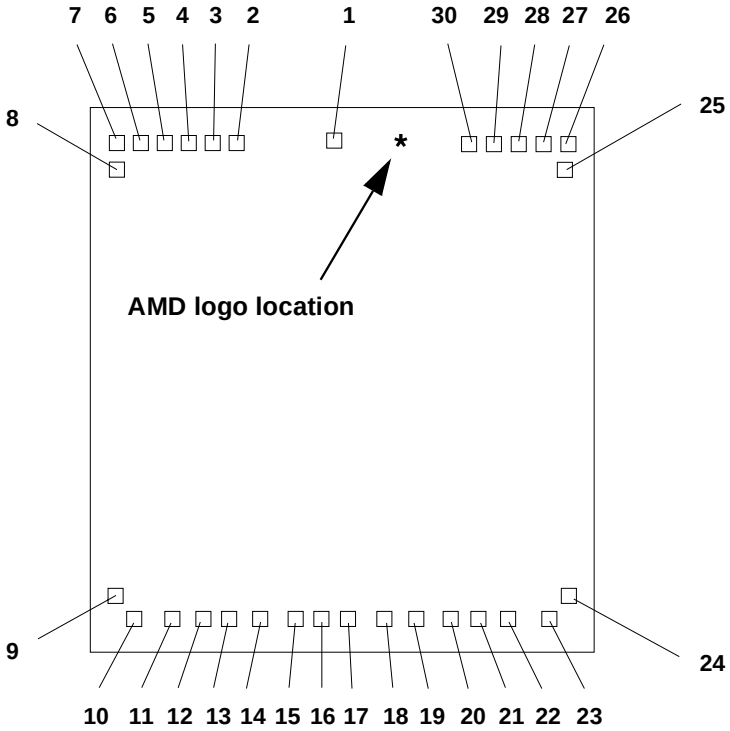
PRODUCT SELECTOR GUIDE

Family Part Number	Am29F010 KGD	
Speed Option (V_{CC} = 5.0 V ± 10%)	**-90**	**-120**
Max Access Time, t_{ACC} (ns)	90	120
Max CE# Access, t_{CE} (ns)	90	120
Max OE# Access, t_{OE} (ns)	35	50

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTION

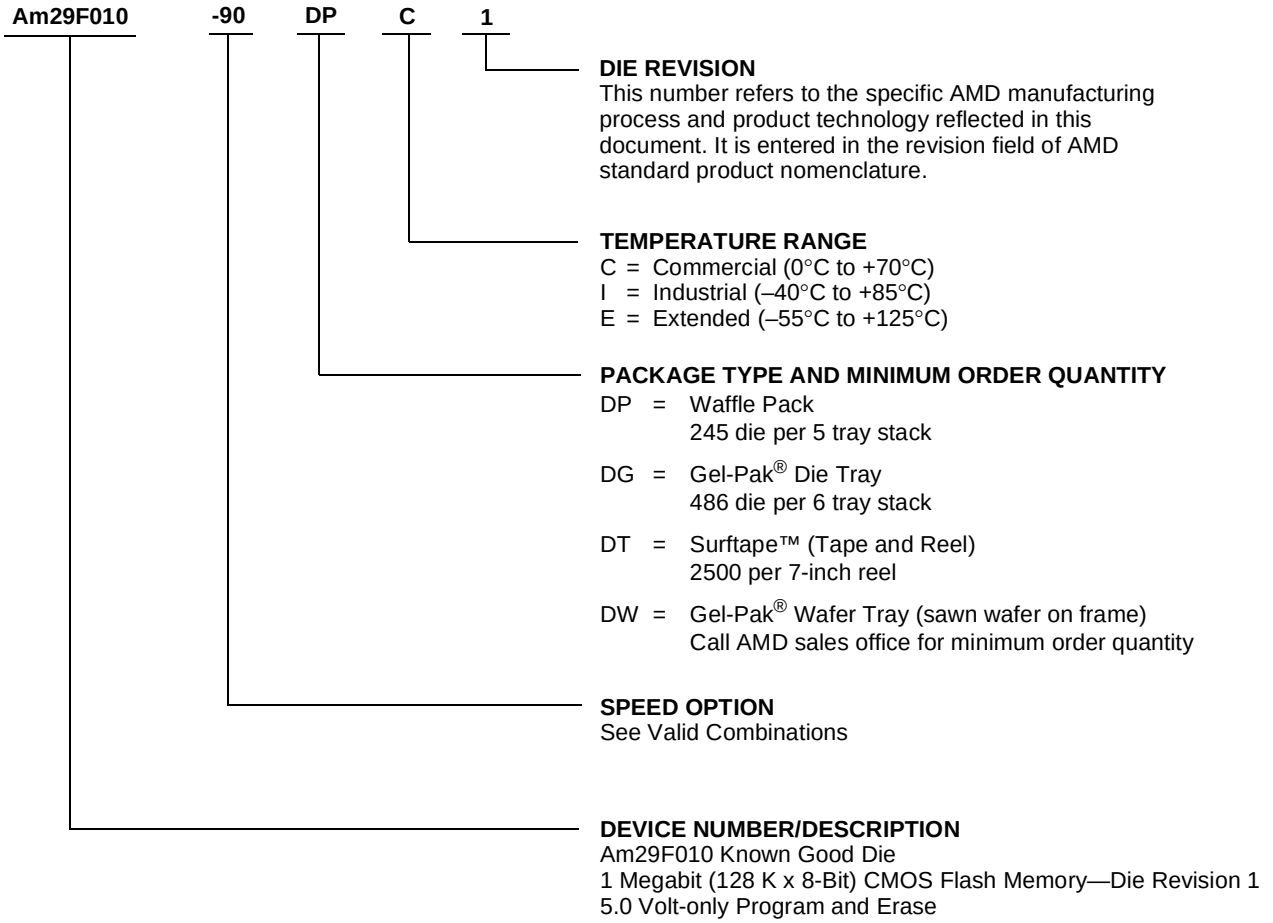
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.00	0.00
2	A16	–33.20	–1.30	–0.84	–0.03
3	A15	–41.60	–1.30	–1.06	–0.03
4	A12	–49.90	–1.30	–1.27	–0.03
5	A7	–58.30	–1.30	–1.48	–0.03
6	A6	–66.60	–1.30	–1.69	–0.03
7	A5	–75.00	–1.30	–1.91	–0.03
8	A4	–74.40	–10.50	–1.89	–0.27
9	A3	–75.60	–158.20	–1.92	–4.02
10	A2	–69.40	–166.80	–1.76	–4.24
11	A1	–56.10	–166.80	–1.42	–4.24
12	A0	–46.10	–166.80	–1.17	–4.24
13	D0	–36.30	–166.90	–0.92	–4.24
14	D1	–25.90	–166.90	–0.66	–4.24
15	D2	–13.30	–166.90	–0.34	–4.24
16	V_{SS}	–4.30	–166.90	–0.11	–4.24
17	D3	4.70	–166.90	0.12	–4.24
18	D4	17.30	–166.90	0.44	–4.24
19	D5	27.60	–166.90	0.70	–4.24
20	D6	40.20	–166.90	1.02	–4.24
21	D7	50.60	–166.90	1.29	–4.24
22	CE#	60.60	–166.80	1.54	–4.24
23	A10	74.00	–166.80	1.88	–4.24
24	OE#	81.40	–158.20	2.07	–4.02
25	A11	80.20	–10.40	2.04	–0.26
26	A9	80.80	–1.30	2.05	–0.03
27	A8	72.40	–1.30	1.84	–0.03
28	A13	64.10	–1.30	1.63	–0.03
29	A14	55.70	–1.30	1.41	–0.03
30	WE#	47.40	–1.30	1.20	–0.03

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

ORDERING INFORMATION

Standard Products

AMD KGD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
Am29F010-90	DPC 1, DPI 1, DPE 1, DGC 1, DGI 1, DGE 1, DTC 1, DTI 1, DTE 1, DWC 1, DWI 1, DWE 1
Am29F010-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29F010 product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

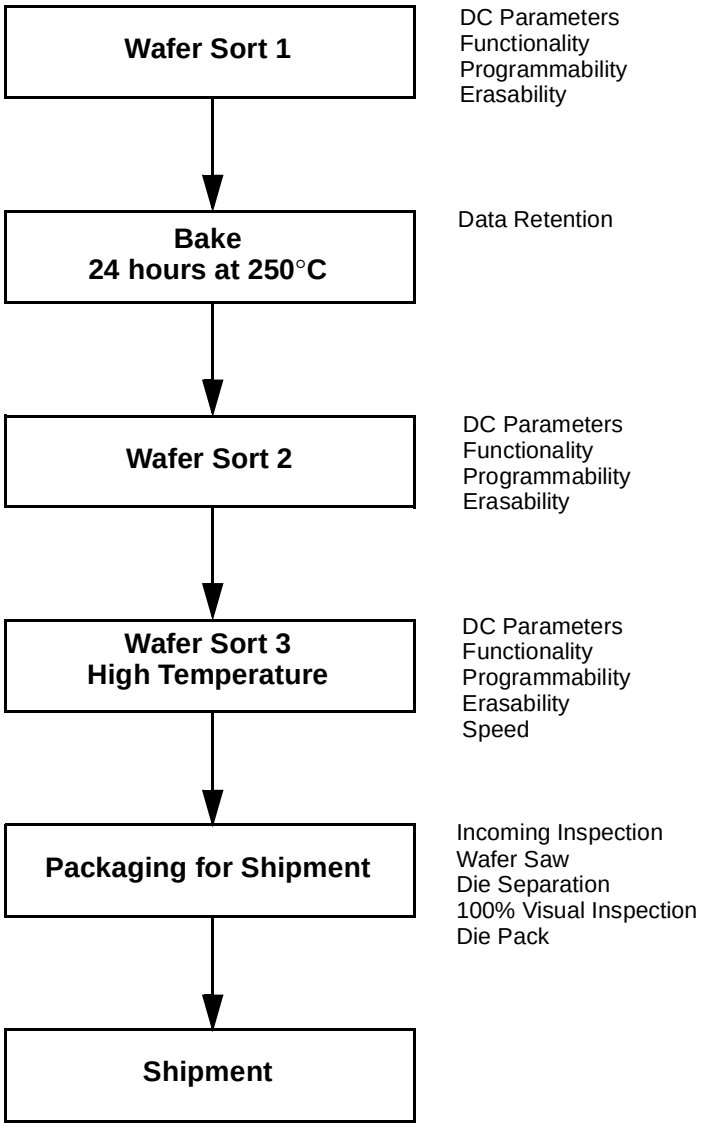


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die dimensions . . . . . 174 mils x 189 mils
4.42 mm x 4.80 mm

Die Thickness . . . . . ~20 mils or ~0.51 mm

Bond Pad Size . . . . . 4.47 mils x 4.47 mils
113.48 µm x 113.48 µm

Pad Area Free of Passivation . . . . . .19.98 $mils^2$
12,878 μm^2

Pads Per Die 30

Bond Pad Metalization . . . . . Al/Si/Cu

Die Backside . . . . . No metal,
may be grounded (optional)

Passivation. . . . . Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . .4.5 V to 5.5 V

Junction Temperature Under Bias . . T_J (max) = 130°C
For Read-only . . . . . T_J (max) = 140°C

Operating Temperature . . . Commercial 0°C to +70°C
Industrial –40°C to +85°C
Extended –55°C to +125°C

MANUFACTURING INFORMATION

Manufacturing and Test. . . . . Fab 14, Austin, TX

Manufacturing ID. 98108AK

Preparation for Shipment . . . . . .Penang, Malaysia

Fabrication Process CS19AFDS

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to AMD Products under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

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REVISION SUMMARY FOR AM29F010 KNOWN GOOD DIE

Formatted to match current template. Updated Distinctive Characteristics and General Description sections using the current main data sheet.