EPSON

S1D13506F00A

Color LCD/CRT/TV Controller

■DESCRIPTION

The S1D13506 is a color LCD/CRT/TV graphics controller interfacing to a wide range of CPUs and display devices. The S1D13506 architecture is designed to meet the low cost, low power requirements of the embedded markets, such as Mobile Communications, Hand-Held PC's, and Office Automation.

The S1D13506 supports multiple CPUs, all LCD panel types, CRT, TV, and additionally provides a number of differentiating features. Products requiring digital camera input can take advantage of the directly supported WINNOV VideumCam™ digital interface. The EPSON Independent Simultaneous Display (EISD) capability allows the user to configure two different images on two different displays, while the SviwelView™, Hardware Cursor, Ink Layer, and BitBLT engine offer substantial performance benefits. These features, combined with the S1D13506's Operating System independence, make it an ideal display solution for a wide variety of applications.

■FEATURES

◆ Memory Interface

- 16-bit DRAM interface:
  - EDO-DRAM up to 40MHz data rate (80M Bytes/s).
  - FPM-DRAM up to 25MHz data rate (50M Bytes/s).
- Memory size options:
  - 512K bytes using one 256Kx16 device.
  - 2M bytes using one 1Mx16 device.
- A configuration register can be programmed to enhance performance by tailoring the memory control output timing to the DRAM device.
- The complete 2M byte display buffer address space is directly and contiguously available through the 21-bit address bus.

◆ CPU Interface

- Supports the following interfaces:
  - Epson S1C33 (16-bit interface to 32-bit microprocessor).
  - Hitachi SH-4 bus interface.
  - Hitachi SH-3 bus interface.
  - MIPS/ISA.
  - Motorola MC68000 (16-bit interface to 16/32-bit microprocessor/microcontroller).
  - Motorola MC68030 (16-bit interface to 16/32-bit microprocessor/microcontroller).
  - Motorola PowerPC MPC82x (16-bit interface to 32-bit microprocessor).
  - MPU bus interface with programmable READY.
  - NEC MIPS VR41xx.
  - PC Card (PCMCIA).
  - Philips MIPS PR31500/31700.
  - Toshiba MIPS TX39xx.
  - StrongARM (PC Card).
- One-stage write buffer for minimum wait-state CPU writes.
- Registers are memory-mapped – the M/R# pin selects between display buffer and register address space.

◆ Display Support

- 4/8-bit monochrome or 4/8/16-bit color LCD interface for single-panel, single-drive displays.
- 8-bit monochrome or 8/16-bit color LCD interface for dual-panel, dual-drive displays.
- Direct support for 9/12-bit TFT/D-TFD, 18-bit TFT/D-TFD is supported up to 64K colors.
- Direct support for CRT up to 64K colors using Embedded RAMDAC.
- Direct support for NTSC/PAL TV output using Embedded RAMDAC.

◆ Display Modes

- 4/8/15/16 bit-per-pixel (bpp) color depths.
- Up to 64 shades of gray on monochrome passive LCD panels using Frame Rate Modulation (FRM) and Dithering.
- Up to 32K/64K colors in 15/16 bpp modes on color passive LCD panels using dithering.
- Up to 64K colors on TFT/D-TFD, CRT and TV.
- 4/8 bit-per-pixel color depths are mapped using three 256x4 Look-Up Tables (LUT) allowing 16/256 out of a possible 4096 colors.
- Separate LUTs for LCD and CRT/TV.

- 15/16 bit-per-pixel color depths are mapped directly, bypassing the LUT.
- Example Resolutions:
  320 x 240 at a color depth of 16 bpp.
  640 x 240 at a color depth of 16 bpp.
  640 x 480 at a color depth of 16 bpp.
  800 x 600 at a color depth of 16 bpp.

◆ Display Features

- SwivelView™: 90°, 180°, 270° hardware rotation of display image.
- EPSON Independent Simultaneous Display (EISD): displays independent images on different displays (CRT or TV and passive or TFT/D-TFD panel).
- Virtual Display Support: displays images larger than the panel size through the use of panning and scrolling.
- Hardware Cursor/Ink Layer: separate 64x64x2 hardware cursor or 2-bit ink layer for both LCD and CRT/TV.
- Double Buffering/Multi-pages: for smooth animation and instantaneous screen update.

◆ Clock Source

- Memory clock can be derived from CLKI or BUSCLK pin. It can be internally divided by 2.
- Pixel clock can be derived from CLKI, CLKI2, or BUSCLK pin. It can be internally divided by 2, 3 or 4.
- Bus clock can be BUSCLK or (BUSCLK)/2, i.e. a 2x clock may be used.

◆ Acceleration

- 2D Engine including the following 2 ROP BitBlts:
  - Write BLT.
  - Move BLT.
  - Solid Fill.
  - Pattern Fill.
  - Transparent Write BLT.
  - Transparent Move BLT.
  - Read BLT.
  - Color Expansion.
  - Move BLT with Color Expansion.

◆ MediaPlug Interface

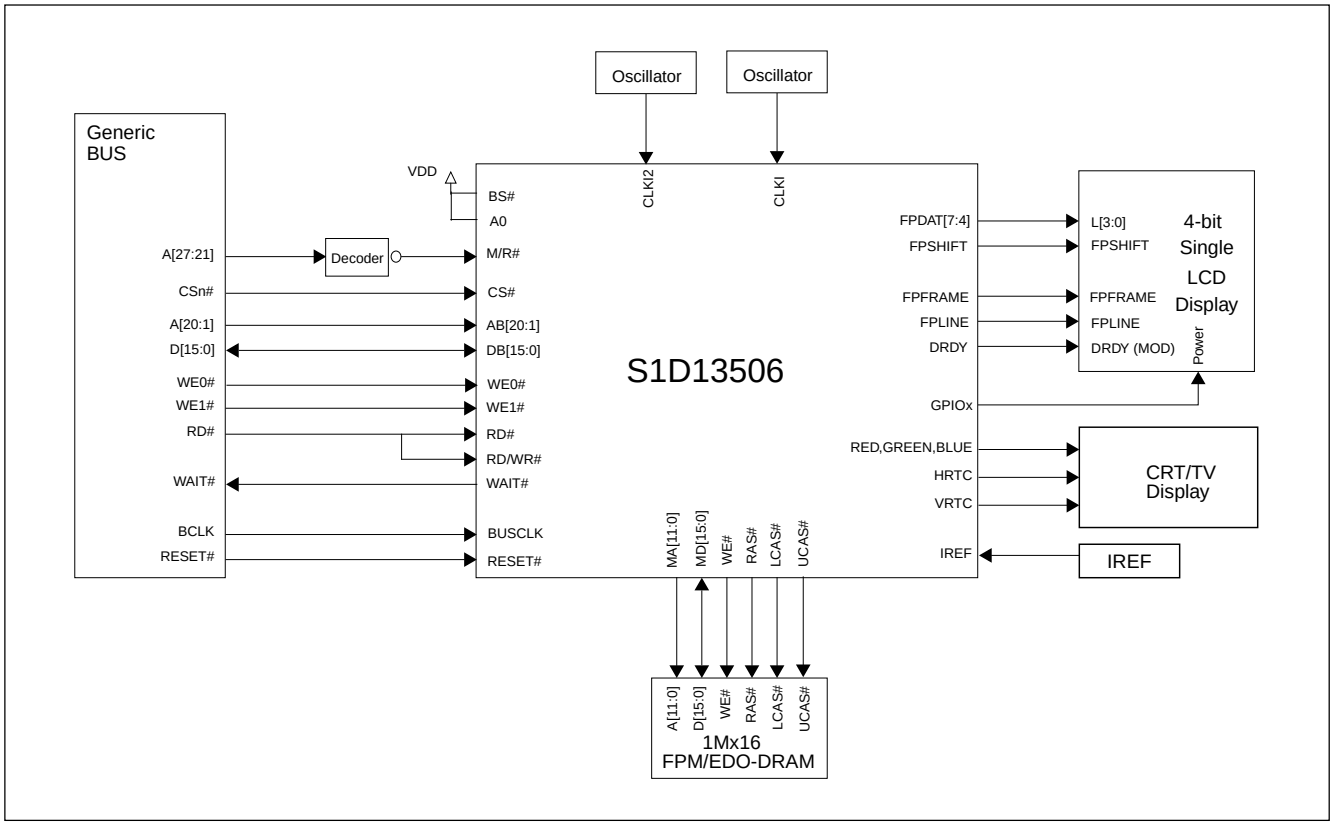
- Built-in WINNOV MediaPlug interface.
- VideumCam support at resolution of 320x240x256 color at 30fps.

◆ Miscellaneous

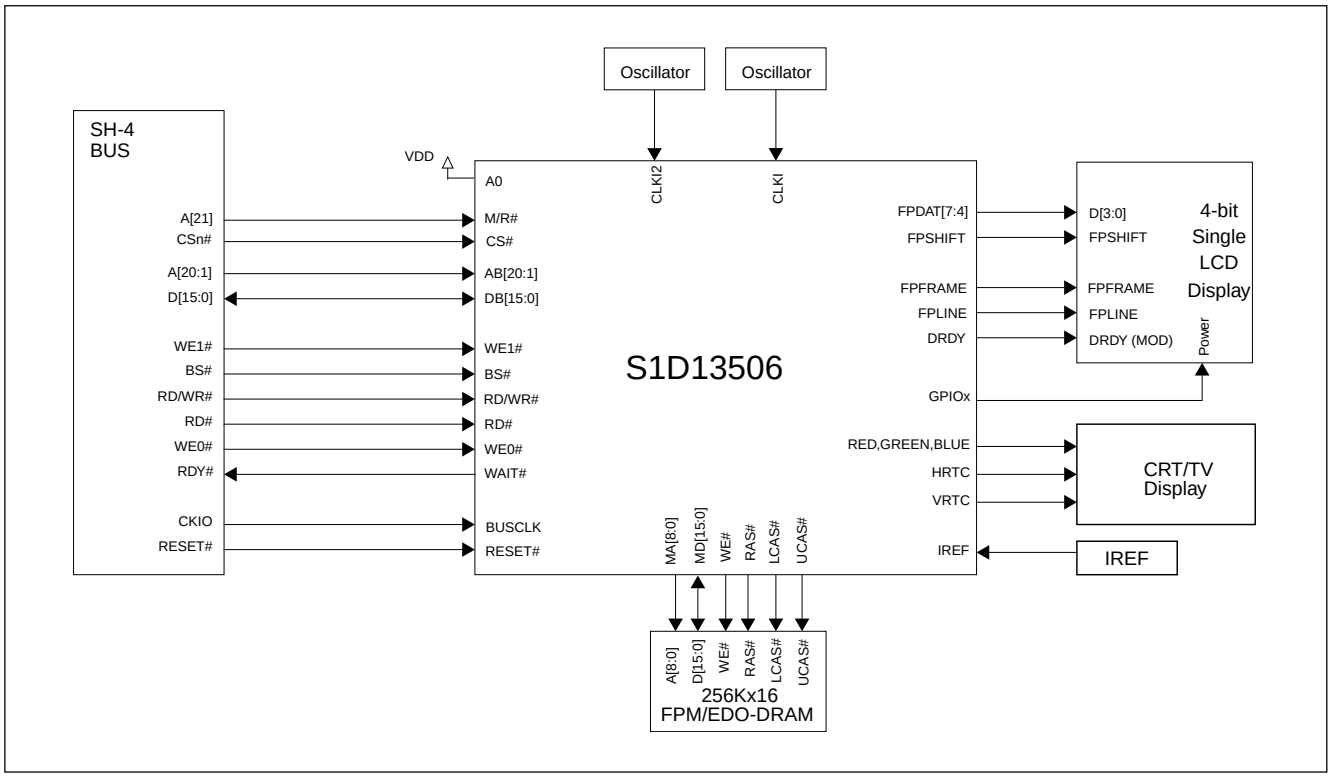
- The memory data bus, MD[15:0], is used to configure the chip at power-on.
- Three General Purpose Input/Output pins, GPIO[3:1], are available if upper Memory Address pins are not required for asymmetric DRAM support.
- Power save mode is initiated by software.
- Operating voltage from 2.7 volts to 5.5 volts.
- 128-pin QFP15 surface mount package.

■ Typical System Implementation Diagrams

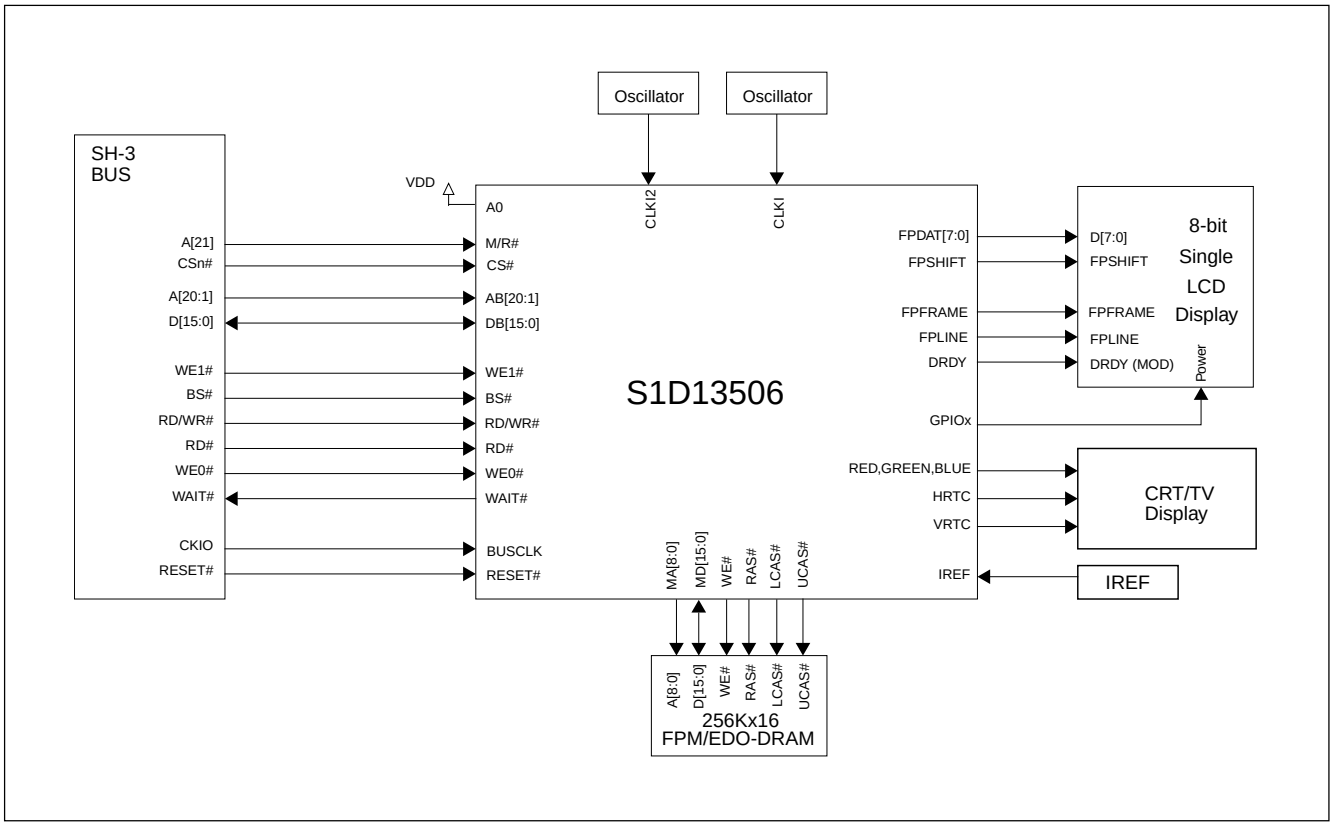
For the pin mapping of each system implementation, see Table “CPU Interface Pin Mapping” on page 21.



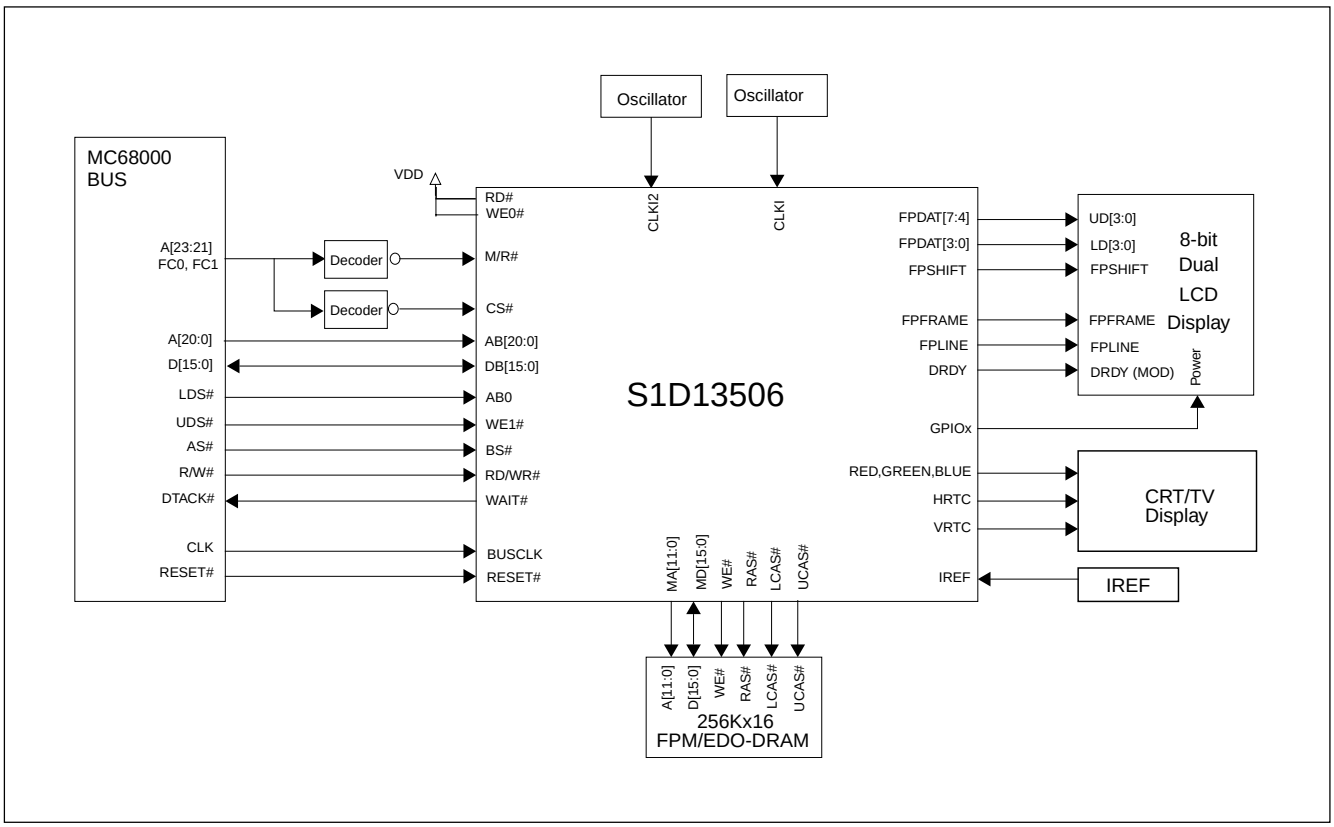
Typical System Diagram (Generic Bus)



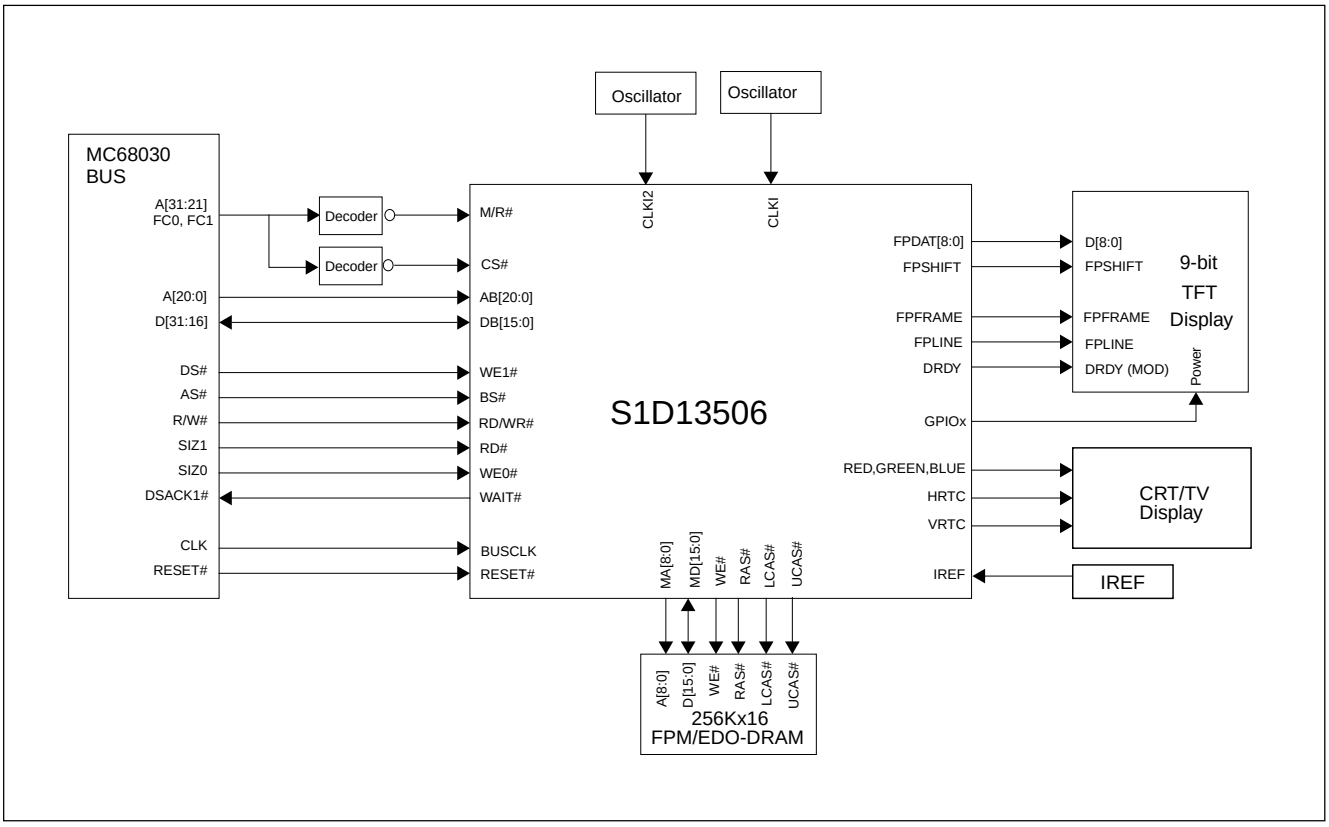
Typical System Diagram (Hitachi SH-4 Bus)



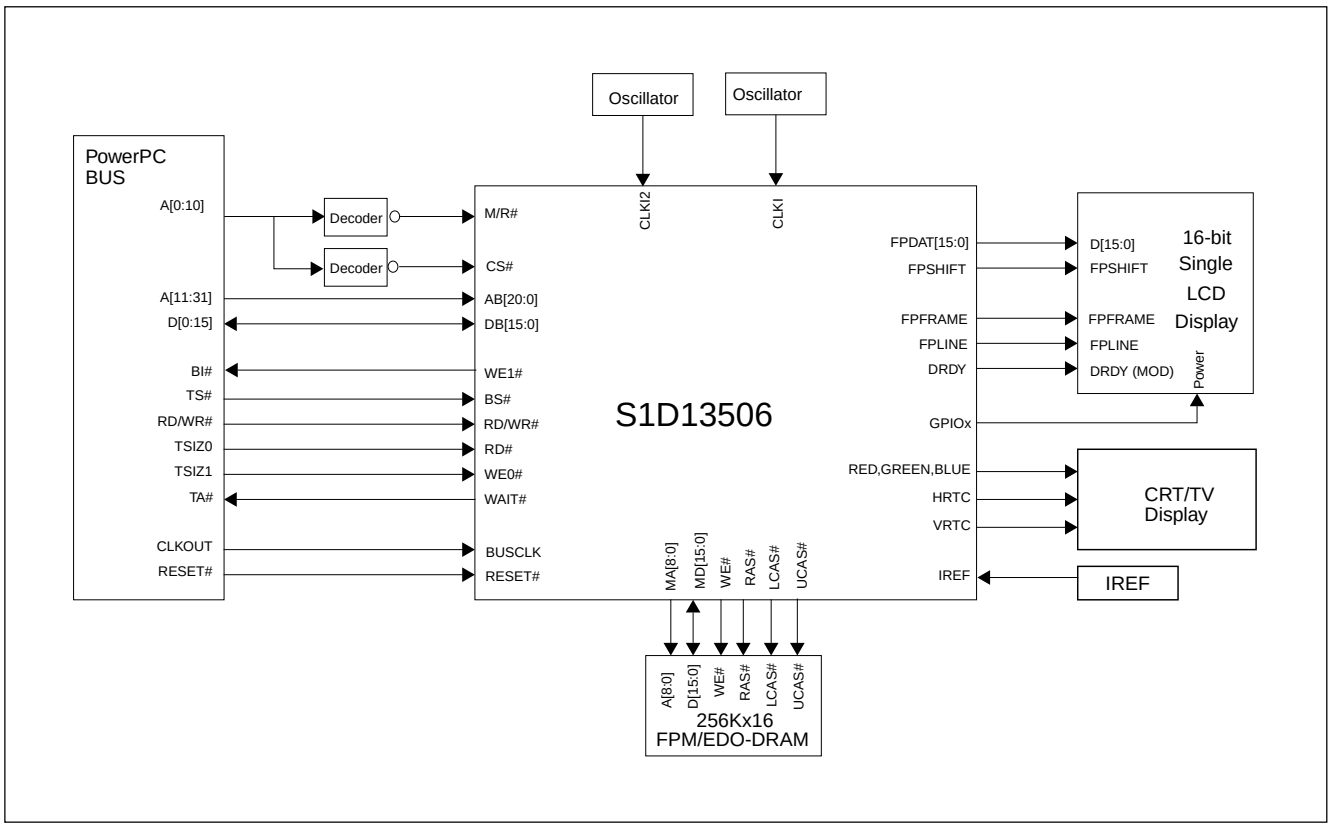
Typical System Diagram (Hitachi SH-3 Bus)



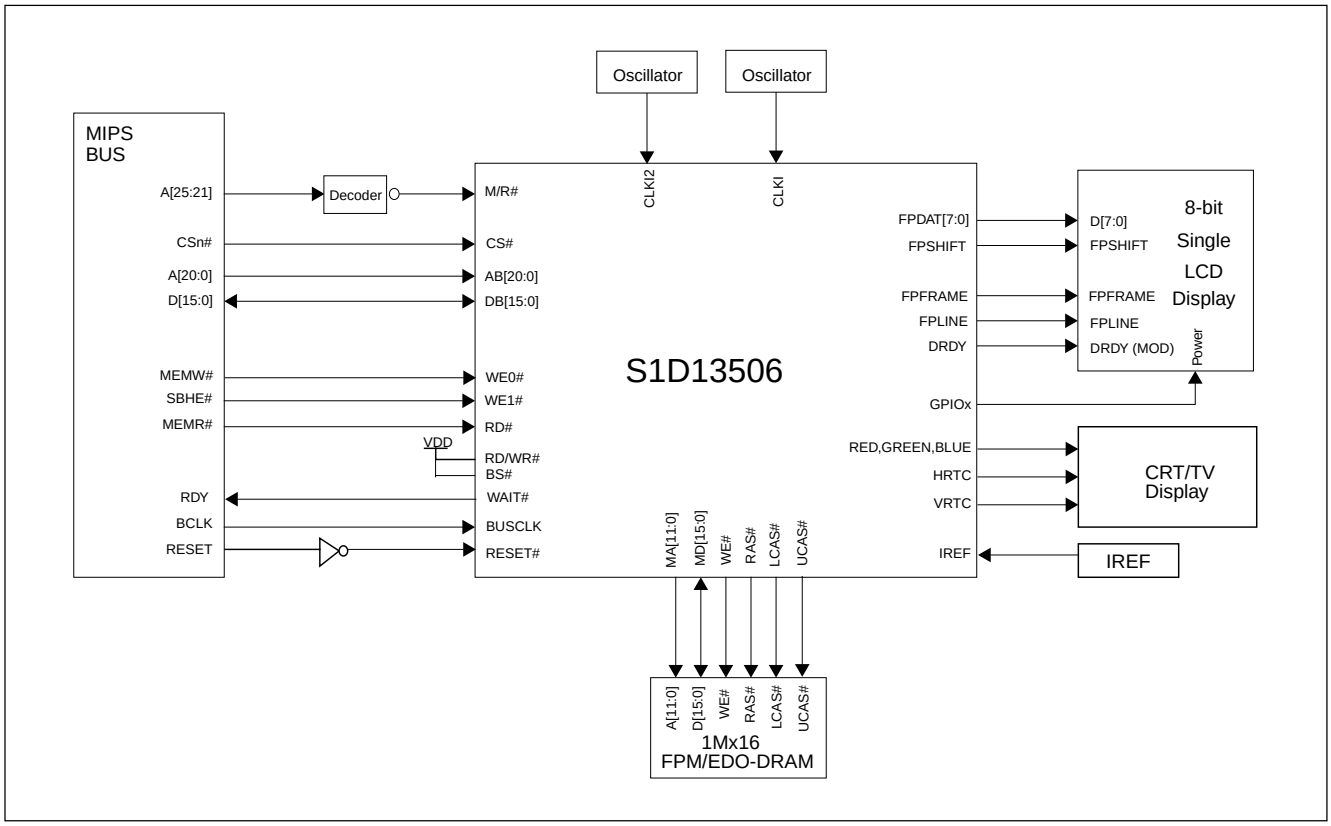
Typical System Diagram (MC68K Bus 1)



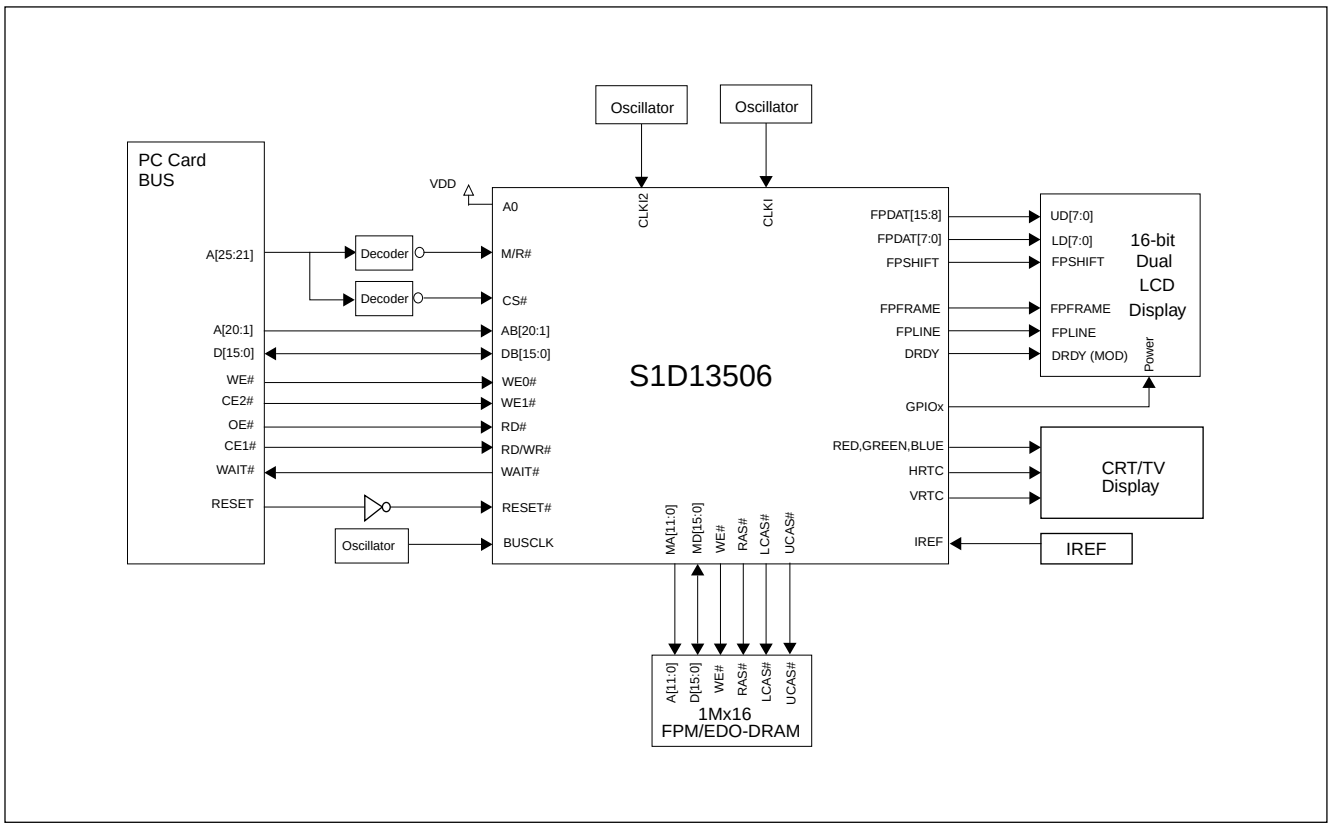
Typical System Diagram (MC68K Bus 2, Motorola 32-Bit 68030)



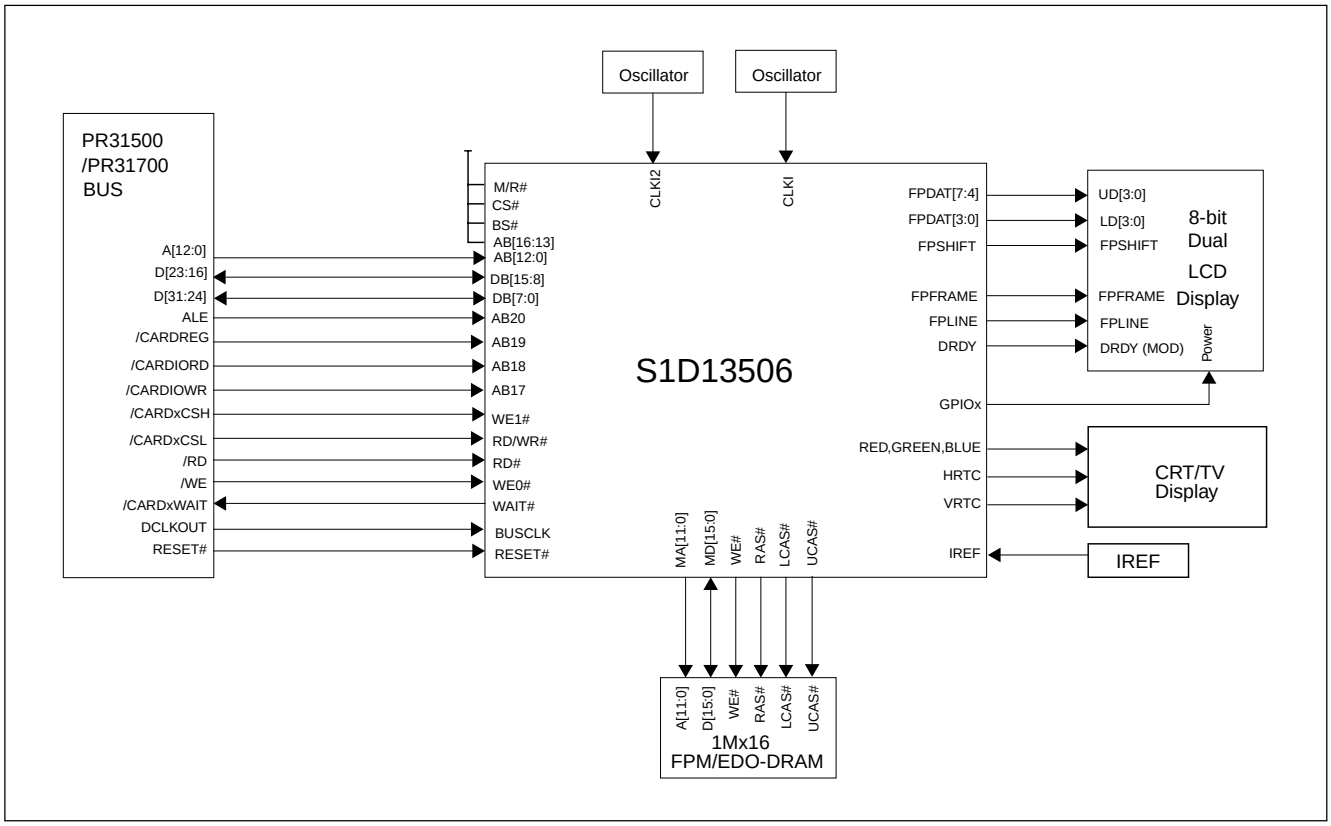
Typical System Diagram (Motorola PowerPC Bus)



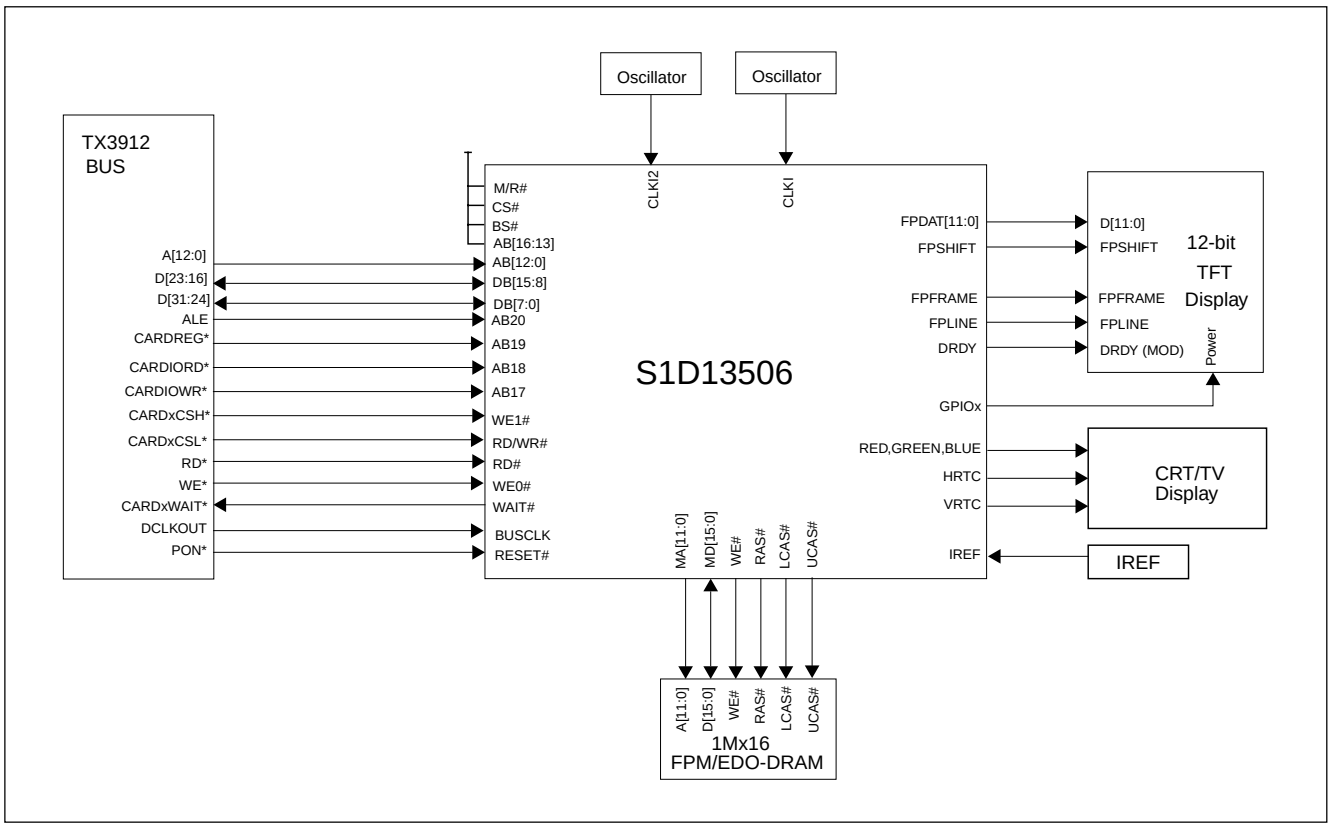
Typical System Diagram (NECVR41xx MIPS Bus)



Typical System Diagram (PC Card Bus)



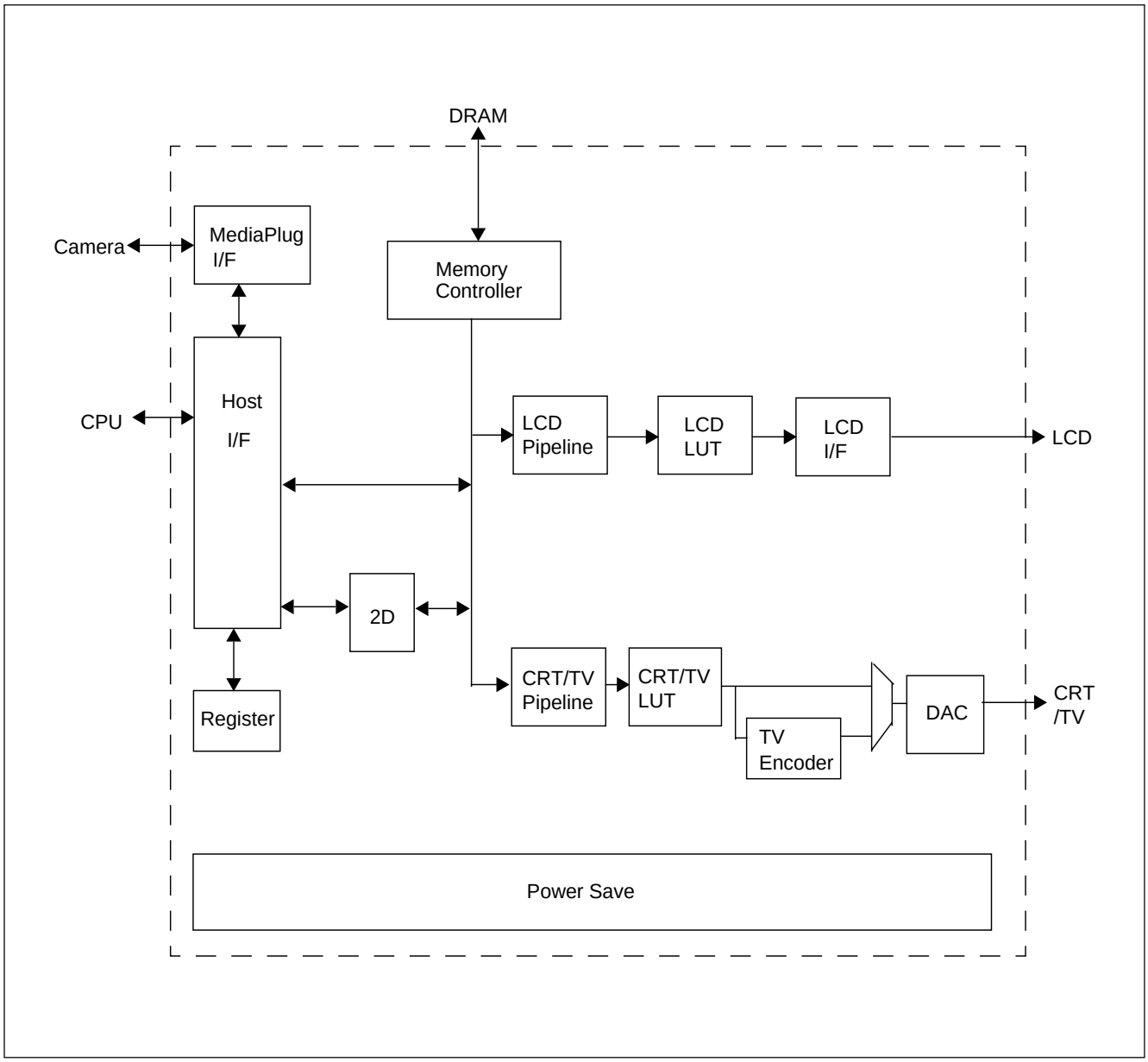
Typical System Diagram (Philips MIPS PR31500/PR31700 Bus)



Typical System Diagram (Toshiba MIPS TX3912 Bus)

■ Internal Description

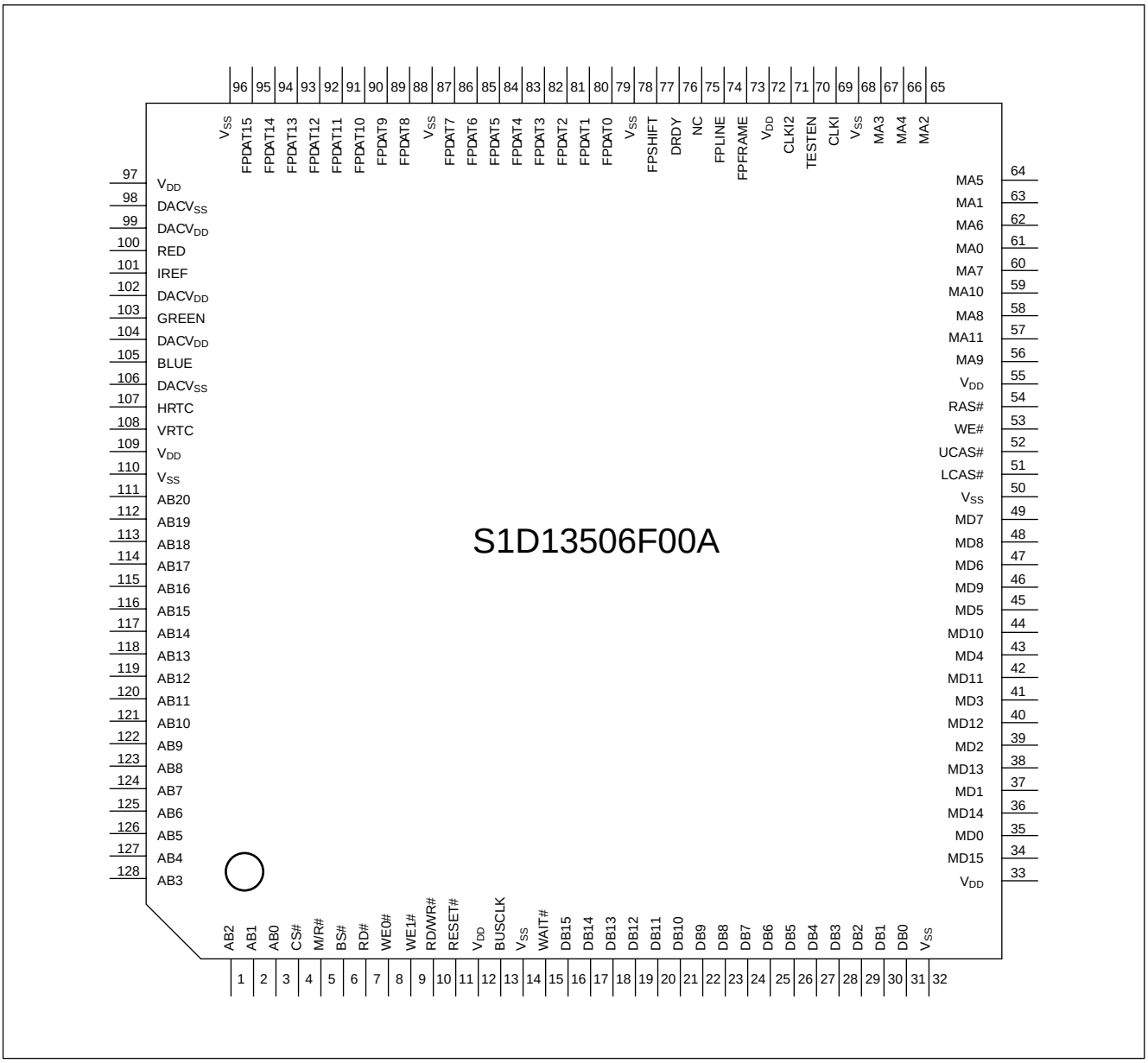
◆ Block Diagram Showing Pipelines



S1D13506 Block Diagram

■ Pins

◆ Pinout Diagram



Pinout Diagram

128-pin QFP15 surface mount package

◆ Pin Description

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
A	=	Analog
P	=	Power pin
C	=	CMOS level input
CD	=	CMOS level input with pull down resistor (Typ. values of 50kΩ/90kΩ at 5V/3.3V respectively)
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA at 5V)
TSx	=	Tri-state CMOS output driver, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA at 5V), x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA at 5V)
TSu	=	TSx with pull up resistor (Typ. values of 100kΩ/180kΩ at 5V/3.3V respectively)
TSxD	=	TSx with pull down resistor, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA at 5V) (Typ. values of 100kΩ/180kΩ at 5V/3.3V)
CNx	=	CMOS low-noise output driver, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA at 5V)
CNxU	=	CNx with pull up resistor, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA at 5V)
CNxD	=	CNx with pull down resistor, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA at 5V)

● Host Bus Interface

Host Bus Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
AB0	I	3	CS	Hi-Z	• For SH-3/SH-4 Bus, this pin must be connected to V_{SS} or V_{DD}. • For MC68K Bus 1, this pin inputs the lower data strobe (LDS#). • For MC68K Bus 2, this pin inputs system address bit 0 (A0). • For Generic Bus, this pin must be connected to V_{SS} or V_{DD}. • For MIPS/ISA Bus, this pin inputs system address bit 0 (SA0). • For Philips PR31500/31700 Bus, this pin inputs system address bit 0 (A0). • For Toshiba TX3912 Bus, this pin inputs system address bit 0 (A0). • For PowerPC Bus, this pin inputs system address bit 31 (A31). • For PC Card (PCMCIA) Bus, this pin must be connected to V_{SS} or V_{DD}. See Table “CPU Interface Pin Mapping” on page 21 for summary. See the respective ACTiming diagram for detailed functionality
AB[12:1]	I	119-128, 1, 2	C	Hi-Z	• For PowerPC Bus, these pins input the system address bits 19 through 30 (A[19:30]). • For all other busses, these pins input the system address bits 12 through 1 (A[12:1]). See Table “CPU Interface Pin Mapping” on page 21 for summary. See the respective AC Timing diagram for detailed functionality.

Host Bus Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
AB[16:13]	I	115-118	C	Hi-Z	• For Philips PR31500/31700 Bus, these pins are connected to V_{DD}. • For ToshibaTX3912 Bus, these pins are connected to V_{DD}. • For PowerPC Bus, these pins input the system address bits 15 through 18 (A[15:18]). • For all other busses, these pins input the system address bits 16 through 13 (A[16:13]). See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
AB17	I	114	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the IO write command (/CARDIOWR). • For ToshibaTX3912 Bus, this pin inputs the IO write command (CARDIOWR*). • For PowerPC Bus, this pin inputs the system address bit 14 (A14). • For all other busses, this pin inputs the system address bit 17 (A17). See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
AB18	I	113	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the IO read command (/CARDIORD). • For ToshibaTX3912 Bus, this pin inputs the IO read command (CARDIORD*). • For PowerPC Bus, this pin inputs the system address bit 13 (A13). • For all other busses, this pin inputs the system address bit 18 (A18). See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
AB19	I	112	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the card control register access (/CARDREG). • For ToshibaTX3912 Bus, this pin inputs the card control register access (CARDREG*). • For PowerPC Bus, this pin inputs the system address bit 12 (A12). • For all other busses, this pin inputs the system address bit 19 (A19). See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
AB20	I	111	C	Hi-Z	• For the MIPS/ISA Bus, this pin inputs system address bit 20. Note that for the ISA Bus, the unlatched LA20 must first be latched before input to AB20. • For Philips PR31500/31700 Bus, this pin inputs the address latch enable (ALE). • For ToshibaTX3912 Bus, this pin inputs the address latch enable (ALE). • For PowerPC Bus, this pin inputs the system address bit 11 (A11). • For all other busses, this pin inputs the system address bit 20 (A20). See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.

Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
DB[15:0]	IO	16-31	C/ TS2	Hi-Z	These pins are the system data bus For 8-bit bus modes, unused data pins should be tied to V_{DD}. • For SH-3/SH-4 Bus, these pins are connected to D[15:0]. • For MC68K Bus 1, these pins are connected to D[15:0]. • For MC68K Bus 2, these pins are connected to D[31:16] for 32-bit devices (eg. MC68030) or D[15:0] for 16-bit devices (eg. MC68340). • For Generic Bus, these pins are connected to D[15:0]. • For MIPS/ISA Bus, these pins are connected to SD[15:0]. • For Philips PR31500/31700 Bus, pins DB[15:8] are connected to D[23:16] and pins DB[7:0] are connected to D[31:24]. • For ToshibaTX3912 Bus, pins DB[15:8] are connected to D[23:16] and pins DB[7:0] are connected to D[31:24]. • For PowerPC Bus, these pins are connected to D[0:15]. • For PC Card (PCMCIA) Bus, these pins are connected to D[15:0]. See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
WE1#	IO	9	CS/ TS2	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K Bus 1, this pin inputs the upper data strobe (UDS#). • For MC68K Bus 2, this pin inputs the data strobe (DS#). • For Generic Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MIPS/ISA Bus, this pin inputs the system byte high enable signal (SBHE#). • For Philips PR31500/31700 Bus, this pin inputs the odd byte access enable signal (/CARDxCSH). • For ToshibaTX3912 Bus, this pin inputs the odd byte access enable signal (CARDxCSH*). • For PowerPC Bus, this pin outputs the burst inhibit signal (BI#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 2 signal (-CE2). See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
M/R#	I	5	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For ToshibaTX3912 Bus, this pin is connected to V_{DD}. • For all other busses, this input pin is used to select between the display buffer and register address spaces of the S1D13506. M/R# is set high to access the display buffer and low to access the registers. See *Register Mapping*. See Table "CPU Interface Pin Mapping" on page 21.
CS#	I	4	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For ToshibaTX3912 Bus, this pin is connected to V_{DD}. • For all other busses, this is the Chip Select input. See Table "CPU Interface Pin Mapping" on page 21. See the respective AC Timing diagram for detailed functionality.

Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
BUSCLK	I	13	C	Hi-Z	This pin inputs the system bus clock. It is possible to apply a 2x clock and divide it by 2 internally - see MD12 in Summary of Configuration Options • For SH-3/SH-4 Bus, this pin is connected to CKIO. • For MC68K Bus 1, this pin is connected to CLK. • For MC68K Bus 2, this pin is connected to CLK. • For Generic Bus, this pin is connected to BCLK. • For MIPS/ISA Bus, this pin is connected to CLK. • For Philips PR31500/31700 Bus, this pin is connected to DCLKOUT. • For ToshibaTX3912 Bus, this pin is connected to DCLKOUT • For PowerPC Bus, this pin is connected to CLKOUT. • For PC Card (PCMCIA) Bus, this pin is connected to the input clock (CLKI). See Table “CPU Interface Pin Mapping” on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
BS#	I	6	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the bus start signal (BS#). • For MC68K Bus 1, this pin inputs the address strobe (AS#). • For MC68K Bus 2, this pin inputs the address strobe (AS#). • For Generic Bus, this pin is connected to V_{DD}. • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For ToshibaTX3912 Bus, this pin is connected to V_{DD}. • For PowerPC Bus, this pin inputs the Transfer Start signal (TS#). • For PC Card (PCMCIA) Bus, this pin is connected to V_{DD}. See Table “CPU Interface Pin Mapping” on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
RD/WR#	I	10	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read write signal (RD/WR#).The S1D13506 needs this signal for early decode of the bus cycle • For MC68K Bus 1, this pin inputs the read write signal (R/W#). • For MC68K Bus 2, this pin inputs the read write signal (R/W#). • For Generic Bus, this pin inputs the read command for the upper data byte (RD1#). • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin inputs the even byte access enable signal (/CARDxCSL). • For ToshibaTX3912 Bus, this pin inputs the even byte access enable signal (CARDxCSL*). • For PowerPC Bus, this pin inputs the read write signal (RD/WR#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 1 signal (-CE1). See Table “CPU Interface Pin Mapping” on page 21 for summary. See the respective AC Timing diagram for detailed functionality.

Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
RD#	I	7	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read signal (RD#). • For MC68K Bus 1, this pin is connected to V_{DD}. • For MC68K Bus 2, this pin inputs the bus size bit 1 (SIZ1). • For Generic Bus, this pin inputs the read command for the lower data byte (RD0#). • For MIPS/ISA Bus, this pin inputs the memory read signal (MEMR#). • For Philips PR31500/31700 Bus, this pin inputs the memory read command (/RD). • For ToshibaTX3912 Bus, this pin inputs the memory read command (RD*). • For PowerPC Bus, this pin inputs the transfer size 0 signal (TSIZ0). • For PC Card (PCMCIA) Bus, this pin inputs the output enable signal (-OE). See Table “CPU Interface Pin Mapping” on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
WE0#	I	8	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K Bus 1, this pin must be connected to V_{DD} • For MC68K Bus 2, this pin inputs the bus size bit 0 (SIZ0). • For Generic Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MIPS/ISA Bus, this pin inputs the memory write signal (MEMW#). • For Philips PR31500/31700 Bus, this pin inputs the memory write command (/WE). • For ToshibaTX3912 Bus, this pin inputs the memory write command (WE*). • For PowerPC Bus, this pin inputs the Transfer Size 1 signal (TSIZ1). • For PC Card (PCMCIA) Bus, this pin inputs the write enable signal (-WE). See Table “CPU Interface Pin Mapping” on page 21 for summary. See the respective AC Timing diagram for detailed functionality.

Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
WAIT#	O	15	TS2	Hi-Z*a or 1*b or 0*c	The active polarity of the WAIT# output is configurable; the state of MD5 on the rising edge of RESET# defines the active polarity of WAIT# - see *"Summary of Configuration Options."* • For SH-3 Bus, this pin outputs the wait request signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For SH-4 Bus, this pin outputs the ready signal (RDY#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 1, this pin outputs the data transfer acknowledge signal (DTACK#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#); MD5 must be pulled high during reset by an external pull-up resistor. • For Generic Bus, this pin outputs the wait signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For MIPS/ISA Bus, this pin outputs the IO channel ready signal (IOCHRDY); MD5 must be pulled low during reset by the internal pull-down resistor. • For Philips PR31500/31700 Bus, this pin outputs the wait state signal (/CARDxWAIT). MD5 must be pulled low during reset by the internal pull-down resistor. • For Toshiba TX3912 Bus, this pin outputs the wait state signal (CARDxWAIT*). MD5 must be pulled low during reset by the internal pull-down resistor. • For PowerPC Bus, this pin outputs the transfer acknowledge signal (TA#); MD5 must be pulled high during reset by an external pull-up resistor. • For PC Card (PCMCIA) Bus, this pin outputs the wait signal (-WAIT); MD5 must be pulled low during reset by the internal pull-down resistor. See Table "CPU Interface Pin Mapping" on page 21 for summary. See the respective AC Timing diagram for detailed functionality.
RESET#	I	11	CS	0	Active low input that clears all internal registers and forces all outputs to their inactive states. Note that active high RESET signals must be inverted before input to this pin.

* a When the MD configuration at RESET# is set such that WAIT# can be tristated.
  b When the MD configuration at RESET# is set such that WAIT# is always driven and active low.
  c When the MD configuration at RESET# is set such that WAIT# is always driven and active high.

● Memory Interface

Memory Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
LCAS#	O	51	CO1	1	• For dual-CAS# DRAM, this is the column address strobe for the lower byte (LCAS#). • For single-CAS DRAM, this is the column address strobe (CAS#). See Table “Memory Interface Pin Mapping” on page 22 for summary.
UCAS#	O	52	CO1	1	This is a multi-purpose pin: • For dual-CAS# DRAM, this is the column address strobe for the upper byte (UCAS#). • For single-CAS# DRAM, this is the write enable signal for the upper byte (UWE#). See Table “Memory Interface Pin Mapping” on page 22 for summary.
WE#	O	53	CO1	1	• For dual-CAS# DRAM, this is the write enable signal (WE#). • For single-CAS# DRAM, this is the write enable signal for the lower byte (LWE#). See Table “Memory Interface Pin Mapping” on page 22 for summary.
RAS#	O	54	CO1	1	Row address strobe.
MD[15:0]	IO	34, 36, 38, 40, 42, 44, 46, 48, 49, 47, 45, 43, 41, 39, 37, 35	C/ TS1D	Hi-Z (pull 0)	Bi-directional memory data bus. During reset, these pins are inputs and their states at the rising edge of RESET# are used to configure the chip - see “Summary of Configuration Options” on page 22. Internal pull-down resistors (Typ. values of 100kΩ at 5V/3.3V respectively) pull the reset states to 0. External pull-up resistors can be used to pull the reset states to 1.
MA[8:0]	O	58, 60, 62, 64, 66, 67, 65, 63, 61	CO1	0	Multiplexed memory address.
MA9	IO	56	C/TS1	0*a or Hi-Z*b	This is a multi-purpose pin: • For 2M byte DRAM, this is memory address bit 9 (MA9). • For asymmetrical 512K byte DRAM, this is memory address bit 9 (MA9). • For symmetrical 512K byte DRAM, this pin can be used as general purpose IO pin 3 (GPIO3). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table “Memory Interface Pin Mapping” on page 22 for summary.

Memory Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
MA10	IO	59	C/TS1	0*c or Hi-Z*d	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 10 (MA10). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 1 (GPIO1). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table “Memory Interface Pin Mapping” on page 22 for summary.
MA11	IO	57	C/TS1	0*e or Hi-Z*f or 1*g	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 11 (MA11). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 2 (GPIO2). • Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table “Memory Interface Pin Mapping” on page 22 for summary. This pin can also be configured as the MediaPlug power pin VMPEPWR - see Table “MA11, MA10, MA9, and DRDY Pin Mapping” on page 23 for details

* a When the MD configuration at RESET# is set such that MA9 is used as MA9.
  b When the MD configuration at RESET# is set such that MA9 is used as GPIO3.
  c When the MD configuration at RESET# is set such that MA10 is used as MA10.
  d When the MD configuration at RESET# is set such that MA10 is used as GPIO1.
  e When the MD configuration at RESET# is set such that MA11 is used as MA11.
  f When the MD configuration at RESET# is set such that MA11 is used as GPIO2.
  g When the MD configuration at RESET# is set such that MA11 is used as VMPEPWR.

● LCD Interface

LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPDAT[8:0]	O	88, 86-79	CN3	0	Panel data bus. Not all pins are used for some panels - see Table “LCD Interface Pin Mapping” on page 22 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table “MediaPlug Interface Pin Mapping” on page 23 for details.
FPDAT9	O	89	CN3D	0*a or Hi-Z*b	Panel data bus. Not all pins are used for some panels - see Table “LCD Interface Pin Mapping” on page 22 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table “MediaPlug Interface Pin Mapping” on page 23 for details.
FPDAT[13:10]	IO	93-90	C/ TS3U	0*c or Hi-Z*d	Panel data bus. Not all pins are used for some panels - see Table “LCD Interface Pin Mapping” on page 22 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table “MediaPlug Interface Pin Mapping” on page 23 for details.
FPDAT[15:14]	O	95,94	CN3	0	Panel data bus. Not all pins are used for some panels - see Table “LCD Interface Pin Mapping” on page 22 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table “MediaPlug Interface Pin Mapping” on page 23 for details.
FPFRAME	O	73	CN3	0	Frame pulse
FPLINE	O	74	CN3	0	Line pulse
FPSHIFT	O	77	CO3	0	Shift clock
DRDY	O	76	CO3	0*e or 1*f	This is a multi-purpose pin: • For TFT/D-TFD panels this is the display enable output (DRDY). • For passive LCD with Format 1 interface this is the 2nd Shift Clock (FPSHIFT2). • For all other LCD panels this is the LCD backplane bias signal (MOD). See Table “LCD Interface Pin Mapping” on page 22 and REG[030h] for details. This pin can also be configured as the MediaPlug power pin VMPEPWR - see Table “MA11, MA10, MA9, and DRDY Pin Mapping” on page 23 for details.

* a When the MD configuration at RESET# is set such that FPDAT9 is used as FPDAT9.
  b When the MD configuration at RESET# is set such that FPDAT9 is used as VMPRCTL.
  c When the MD configuration at RESET# is set such that FPDAT[13:10] is used as FPDAT[13:10].
  d When the MD configuration at RESET# is set such that FPDAT[13:10] is used as VMPD[3:0].
  e When the MD configuration at RESET# is set such that DRDY is used as DRDY (MOD).
  f When the MD configuration at RESET# is set such that DRDY is used as VMPEPWR.

● CRT Interface

CRT Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
HRTC	O	107	CN3	0	Horizontal retrace signal for CRT
VRTC	O	108	CN3	0	Vertical retrace signal for CRT
RED	O	100	A	no output current	Analog output for CRT color Red / S-Video Luminance
GREEN	O	103	A	no output current	Analog output for CRT color Green / Composite Video Out
BLUE	O	105	A	no output current	Analog output for CRT color Blue / S-Video Chrominance
IREF	I	101	A	–	Current reference for DAC. This pin must be connected to V_{SS} if the DAC is not needed.

● Miscellaneous

Miscellaneous Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
CLKI	I	69	C	–	Selectable input clock. Can be used for the internal pixel clock (PCLK), memory clock (MCLK), and MediaPlug Clock.
CLKI2	I	71	C	–	Selectable input clock. Can be used for the internal pixel clock (PCLK) and MediaPlug Clock.
TESTEN	I	70	CD	–	Test Enable. This pin should be connected to V_{SS} for normal operation.
V_{DD}	P	12, 33, 55, 72, 97, 109	P	–	V_{DD}
$DACV_{DD}$	P	99, 102, 104	P	–	DAC V_{DD}
V_{SS}	P	14, 32, 50, 68, 78, 87, 96, 110	P	–	V_{SS}
$DACV_{SS}$	P	98, 106	P	–	DAC V_{SS}
NC	-	75		–	Not connected

◆ Summary of Configuration Options

Summary of Power-On/Reset Options

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">value of this pin at rising edge of RESET# is used to configure:(1/0)</th></tr>
<tr><th>1</th><th>0</th></tr>
<tr><td>MD0</td><td colspan="2">Not used, value of this pin at rising edge of RESET# can be read at REG[00Ch] bit 0</td></tr>
<tr><td>MD11, MD[3:1]</td><td colspan="2">Select Host Bus Interface as follows :

MD11 MD3 MD2 MD1 Host Bus
0 0 0 0 SH-4/SH-3 Bus interface
0 0 0 1 MC68K Bus 1
0 0 1 0 MC68K Bus 2
0 0 1 1 Generic
0 1 0 0 Reserved
0 1 0 1 MIPS/ISA
0 1 1 0 PowerPC
0 1 1 1 PC Card (PCMCIA)
1 1 1 1 Philips PR31500/PR31700 / Toshiba TX3912</td></tr>
<tr><td>MD4</td><td>Little Endian</td><td>Big Endian</td></tr>
<tr><td>MD5</td><td>WAIT# is active high (1 = insert wait state)</td><td>WAIT# is active low (0 = insert wait state)</td></tr>
<tr><td>MD[7:6]</td><td colspan="2">Memory Address/GPIO configuration:
(See Table “MA11, MA10, MA9, and DRDY Pin Mapping” on page 23)
00 = symmetrical 256K 16 DRAM. MA[8:0] = DRAM address. MA[11:9] can be used as GPIO2,1,3 pins .
01 = symmetrical 1M 16 DRAM. MA[9:0] = DRAM address. MA[11:10] can be used as GPIO2,1 pins.
10 = asymmetrical 256K 16 DRAM. MA[9:0] = DRAM address. MA[11:10] can be used as GPIO2,1 pins.
11 = asymmetrical 1M 16 DRAM. MA[11:0] = DRAM address.</td></tr>
<tr><td>MD8</td><td colspan="2">Not used, value of this pin at rising edge of RESET# can be read at REG[00Dh] bit 0</td></tr>
<tr><td>MD9</td><td colspan="2">Not used, value of this pin at rising edge of RESET# can be read at REG[00Dh] bit 1</td></tr>
<tr><td>MD10</td><td colspan="2">Not Used, value of this pin at rising edge of RESET# can be read at REG[00Dh] bit 2</td></tr>
<tr><td>MD11</td><td>Alternate Host Bus Interface Selected</td><td>Primary Host Bus Interface Selected</td></tr>
<tr><td>MD12</td><td>BUSCLK input divided by 2</td><td>BUSCLK input not divided</td></tr>
<tr><td>MD13</td><td>Configure FPDAT[15:8] for MediaPlug I/F. External latches required to support 16-bit passive panels.</td><td>Support 16-bit passive panels directly</td></tr>
<tr><td>MD14</td><td>DRDY or MA11 is configured as MediaPlug power down pin (VMPEPWR). (See Table “MA11, MA10, MA9, and DRDY Pin Mapping” on page 23)</td><td>DRDY is configured as a normal LCD I/F output pin. MA11 is configur ed as either a memory address or GPIO2. (See Table “MA11, MA10, MA9, and DRDY Pin Mapping” on page 23)</td></tr>
<tr><td>MD15</td><td>WAIT# is always driven</td><td>WAIT# is tristated when the chip is not accessed by the host</td></tr>
</table>

◆ Multiple Function Pin Mapping

CPU Interface Pin Mapping

S1D13506 Pin Names	Generic	Hitachi SH-4/SH-3	MIPS/ISA	Motorola MC68K Bus 1	Motorola MC68K Bus 2	Motorola PowerPC	PC Card	Philips PR31500 /PR31700	Toshiba TX3912
AB20	A20	A20	LatchA20	A20	A20	A11	A20	ALE	ALE
AB19	A19	A19	SA19	A19	A19	A12	A19	/CARDREG	CARDREG*
AB18	A18	A18	SA18	A18	A18	A13	A18	/CARDIORD	CARDIORD*
AB17	A17	A17	SA17	A17	A17	A14	A17	/CARDIOWR	CARDIOWR*
AB[16:13]	A[16:13]	A[16:13]	SA[16:13]	A[16:13]	A[16:13]	A[15:18]	A[16:13]	Connected to V_{DD}	Connected to V_{DD}
AB[12:1]	A[12:1]	A[12:1]	SA[12:1]	A[12:1]	A[12:1]	A[19:30]	A[12:1]	A[12:1]	A[12:1]
AB0	Connected to V_{DD}*1	Connected to V_{DD}*1	SA0	LDS#	A0	A31	Connected to V_{DD}*1	A0	A0
DB[15:8]	D[15:0]	D[15:8]	SD[15:0]	D[15:8]	D[31:24]	D[0:7]	D[15:0]	D[23:16]	D[23:16]
DB[7:0]	D[7:0]	D[7:0]	SD[7:0]	D[7:0]	D[23:16]	D[8:15]	D[7:0]	D[31:24]	D[31:24]
WE1#	WE1#	WE1#	SBHE#	UDS#	DS#	$\overline{BI}$	CE2#	/CARDxCSH	CARDxCSH*
M/R#	External Decode							Connected to V_{DD}	Connected to V_{DD}
CS#	External Decode							Connected to V_{DD}	Connected to V_{DD}
BUSCLK	BCLK	CKIO	CLK	CLK	CLK	CLKOUT	External Oscillator*2	DCLKOUT	DCLKOUT
BS#	Connected to V_{DD}	BS#	Connected to V_{DD}	AS#	AS#	$\overline{TS}$	Connected to V_{DD}	Connected to V_{DD}	Connected to V_{DD}
RD/WR#	RD1#	RD/WR#	Connected to V_{DD}	R/W#	R/W#	$\overline{RD/WR}$	CE1#	/CARDxCSL	CARDxCSL*
RD#	RD0#	RD#	MEMR#	Connected to V_{DD}	SIZ1	TSIZ0	OE#	/RD	RD*
WE0#	WE0#	WE0#	MEMW#	Connected to V_{DD}	SIZ0	TSIZ1	WE#	/WE	WE*
WAIT#	WAIT#	RDY# /WAIT#	IOCHRDY	DTACK#	DSACK1 #	$\overline{TA}$	WAIT#	/CARDxWAIT	CARDxWAIT*
RESET#	RESET#	RESET#	Inverted RESET	RESET#	RESET#	RESET#	Inverted RESET	RESET#	PON*

Note: All GPIO pins default to input on reset and unless programmed otherwise, must be connected to either V_{SS} or IOV_{DD} if not used.

*1: AB0 is not used internally for these busses and must be connected to either V_{SS} or V_{DD}.

*2: For further information on interfacing the S1D13506 to the PC Card bus, see Interfacing to the PC Card Bus, document number X25B-G-005-xx

Memory Interface Pin Mapping

S1D13506 Pin Names	FPM/EDO-DRAM							
	Sym 256Kx16		Asym 256Kx16		Sym 1Mx16		Asym 1Mx16	
	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#
MD[15:0]	D[15:0]							
MA[8:0]	A[8:0]							
MA9*1	GPIO3*2		A9				A9	
MA10*1	GPIO1[2]						A10	
MA11*1	GPIO2[2]						A11	
UCAS#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#
LCAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#
WE#	WE#	LWE#	WE#	LWE#	WE#	LWE#	WE#	LWE#
RAS#	RAS#							

*1 For MA9, MA10, and MA11 functionality see Table “MA11, MA10, MA9, and DRDY Pin Mapping” on page 23.

*2 All GPIO pins default to input on reset and unless programmed otherwise, should be connected to either V_{SS} or IOV_{DD} if not used.

LCD Interface Pin Mapping

S1D13506 Pin Names	Monochrome Passive Panel			Color Passive Panel						Color TFT/D-TFD Panel		
	Single		Dual	Single	Single Format 1	Single Format 2	Single	Dual				
	4-bit	8-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	8-bit	16-bit	9-bit	12-bit	18-bit
FPFRAME	FPFRAME											
FPLINE	FPLINE											
FPSHIFT	FPSHIFT											
DRDY	MOD				FPSHIFT2	MOD				DRDY		
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	D0	LD0	LD0	R2	R3	R5
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	D1	LD1	LD1	R1	R2	R4
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	D2	LD2	LD2	R0	R1	R3
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	D3	LD3	LD3	G2	G3	G5
FPDAT4	D0	D4	UD0	D0	D4	D4	D4	UD0	UD0	G1	G2	G4
FPDAT5	D1	D5	UD1	D1	D5	D5	D5	UD1	UD1	G0	G1	G3
FPDAT6	D2	D6	UD2	D2	D6	D6	D6	UD2	UD2	B2	B3	B5
FPDAT7	D3	D7	UD3	D3	D7	D7	D7	UD3	UD3	B1	B2	B4
FPDAT8	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D8	driven 0	LD4	B0	B1	B3
FPDAT9	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D9	driven 0	LD5	driven 0	R0	R2
FPDAT10	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D10	driven 0	LD6	driven 0	driven 0	R1
FPDAT11	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D11	driven 0	LD7	driven 0	G0	G2
FPDAT12	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D12	driven 0	UD4	driven 0	driven 0	G1
FPDAT13	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D13	driven 0	UD5	driven 0	driven 0	G0
FPDAT14	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D14	driven 0	UD6	driven 0	B0	B2
FPDAT15	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D15	driven 0	UD7	driven 0	driven 0	B1

Note: DRDY and FPDAT[15:8] may be used by the MediaPlug interface when the MediaPlug is enabled. For MediaPlug Interface pin mapping, see Table “MediaPlug Interface Pin Mapping.”

MA11, MA10, MA9, and DRDY Pin Mapping

MD14, MD7, MD6	MA11	MA10	MA9	DRDY
000	GPIO2	GPIO1	GPIO3	DRDY
001	GPIO2	GPIO1	MA9	DRDY
010	GPIO2	GPIO1	MA9	DRDY
011	MA11	MA10	MA9	DRDY
100	VMPEPWR	GPIO1	GPIO3	DRDY
101	VMPEPWR	GPIO1	MA9	DRDY
110	VMPEPWR	GPIO1	MA9	DRDY
111	MA11	MA10	MA9	VMPEPWR

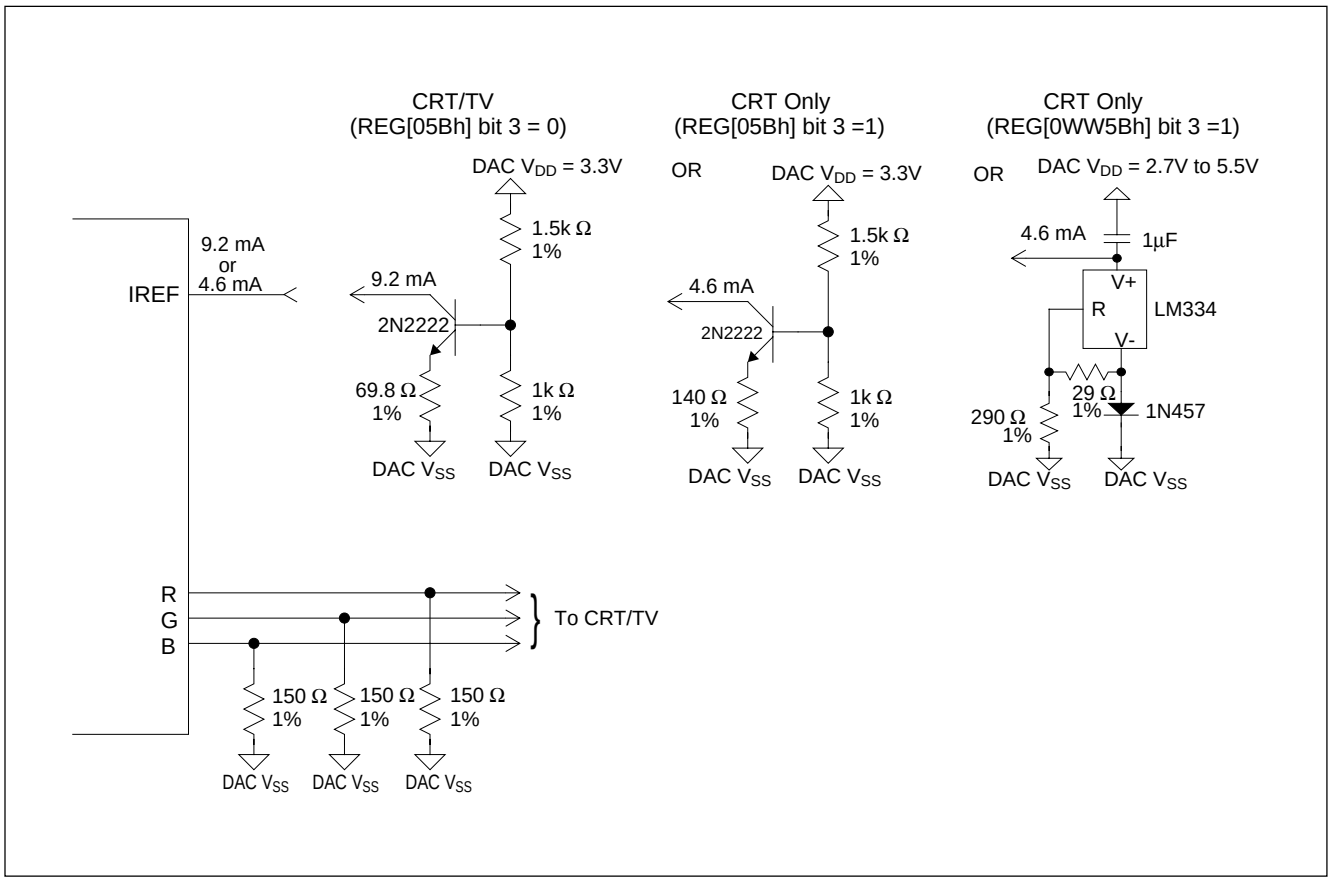
MediaPlug Interface Pin Mapping

S1D13506 Pin Names	IO Type	MediaPlug I/F (MD13=1 at RESET)
FPDAT8	O	VMPLCTL
FPDAT9	I	VMPRCTL
FPDAT10	IO	VMPD0
FPDAT11	IO	VMPD1
FPDAT12	IO	VMPD2
FPDAT13	IO	VMPD3
FPDAT14	O	VMPCLK
FPDAT15	O	VMPCLKN
DRDY or MA11*1	O	VMPEPWR

*1 Either DRDY or MA11 may be used for VMPEPWR (see Table “MA11, MA10, MA9, and DRDY Pin Mapping”). If DRDY is required by the LCD interface and MA11 is required by the DRAM interface then VMPEPWR is not available.

◆ CRT/TV Interface

The following figure shows external circuitry for the CRT/TV interface.



External Circuitry for CRT/TV Interface

Note: Example implementation only, individual characteristics of components may affect actual IREF current.

■ D.C. Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
DAC V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	˚C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max. at lead	˚C

Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	˚C

Electrical Characteristics for V_{DD} = 5.0V typical

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			400	uA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	V_{DD} = Min. I_{OL} = -4mA (Type1), -8mA (Type2) -12mA (Type3)	V_{DD} - 0.4			V
V_{OL}	Low Level Output Voltage	V_{DD} = Min. I_{OL} = 4mA (Type1), 8mA (Type2) 12mA (Type3)			0.4	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = Max.	3.5			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = Min.			1.0	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V			4.0	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.8			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.3			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	50	100	200	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Electrical Characteristics for V_{DD} = 3.3V typical

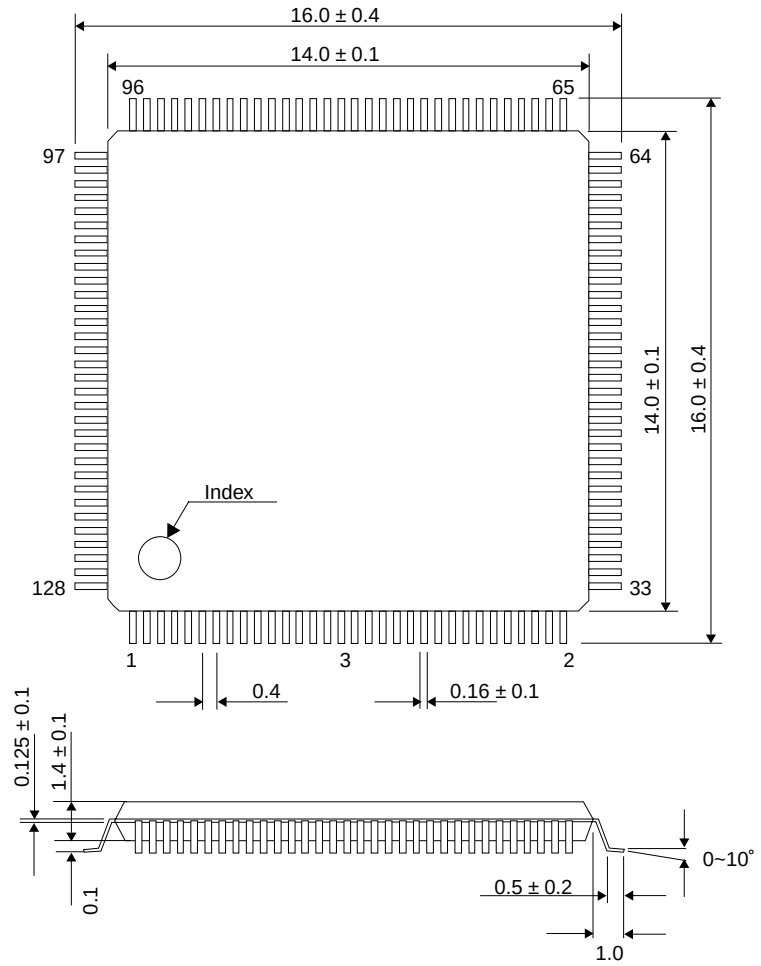
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			290	uA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	V_{DD} = Min. I_{OL} = -2mA (Type1), -4mA (Type2) -6mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	V_{DD} = Min. I_{OL} = 2mA (Type1), 4mA (Type2) 6mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = Max.	2.2			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = Min.			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V			2.4	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.6			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	90	180	360	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Electrical Characteristics for V_{DD} = 3.0V typical

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			260	uA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	V_{DD} = Min. I_{OL} = -1.8mA (Type1), -3.5mA (Type2) -5mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	V_{DD} = Min. I_{OL} = 1.8mA (Type1), 3.5mA (Type2) 5mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = Max.	2.0			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = Min.			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V			2.3	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.5			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	100	200	400	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

■ Mechanical Data

128-pin QFP15 surface mount package



Mechanical Drawing QFP15

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