Datasheet

FS501

18-bit ADC with two low noise OPAMPs

Fortune SEMICONDUCTOR CORPORATION

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Contents

1. Introduction to FS501 Chip

FS501 is a high resolution analog-to-digital converter (ADC) chip. The core of this chip is an 18-bit resolution ΔΣ ADC. Besides the ΔΣ ADC, FS501 consists of switching circuits, operational amplifier (op amp), digital filter, crystal oscillation circuits, digital control logic, and microprocessor interface. Under 5V working voltage, this chip consumes 1.2mA power.

FS501 contains two op amps and several programmable ADC direct inputs. The input signals of the ADC and the reference voltages are fully differential. This mechanism can measure the fully differential small signals. The application includes electronic scale and infrared ear thermometer.

The FS501 ADC contains two digital filters. One is an 18-b/5Hz high resolution output, and the other is a 12-b/325Hz resolution output.

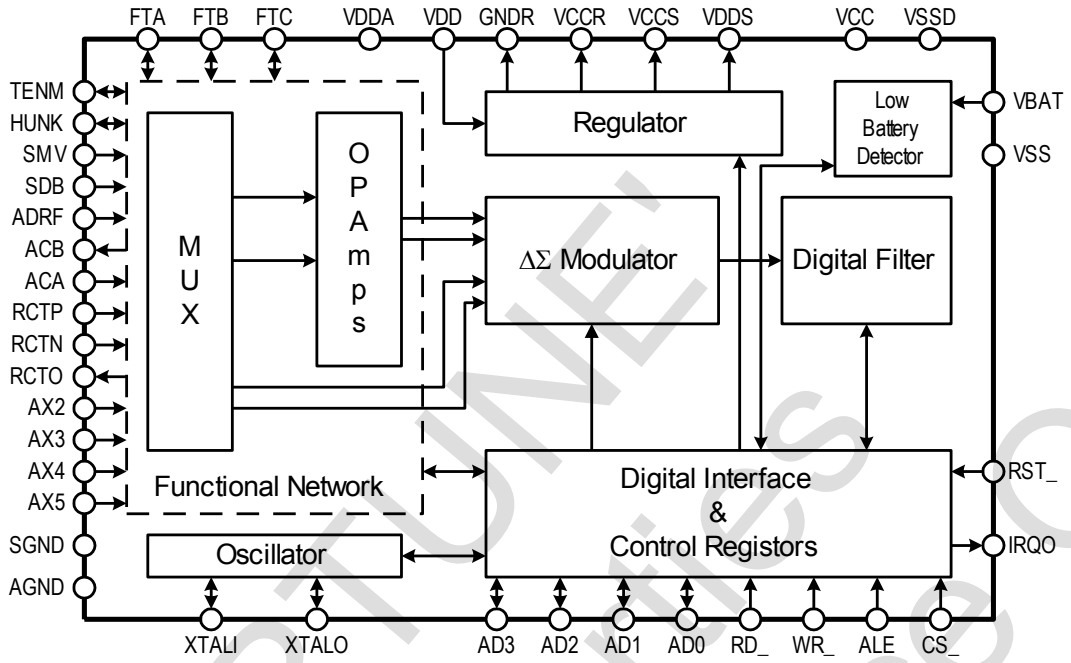
Table 1. FS501 IC Chip

IC Chip	Package	High Resolution 〔Bits/Hz〕	Low Resolution 〔Bits/Hz〕	Voltage Low Detector/ (Thermistor) Resistance Measuring
FS501F	LQFP44	18/5	12/325	√

Characteristics

- Embed High resolution ΔΣ ADC
- Five 18-bit high resolution outputs per second
- 325 12-bit outputs per second
- Embed two op amps
- Embed a voltage regulator, input: 5 V, outputs: 2.5 V and 4V
- Chip current is less than 1.2mA
- With power saving mode
- 50/60 Hz noise distortion
- Embed crystal oscillation circuits
- Standard 4-bit parallel port interface, can be directly connected to microprocessor I/O ports
- With four programmable ADC direct input channels

Block Diagram of FS501



2. Electrical Characteristics

•(VDD = 6V, VSS = 0V, T_A=+25℃, unless otherwise indicated)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Analog-to-Digital Converter					
Zero Input Reading	V_{IN}=0V, 500mV Scale	-1	0	1	Counts
Zero Reading Drift	V_{IN}=0V, 0℃<T_A<+70℃		0	1	μ V/℃
Linearity (Max. deviation from best straight line fit)	500mV Scale	-2	0	2	Counts
Input Common-Mode Rejection Ratio	V_{CM}=±1V, V_{IN}=0V, 500mV Scale			120	μ V/V
Input Common-Mode Voltage Range	V_{IN}=0V, 500mV Scale, ±12 Counts	-1		1	V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN}=0V, 500mV Scale		0	1	Counts
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	-V_{IN}=+V_{IN}=500.00mV	0	1	5	Counts
Input Leakage Current	V_{IN}=0V		1	10	pA
Scale Factor Temperature Coefficient	V_{IN}=500.00mV, 0℃<T_A<+70℃		7.5		ppm/℃
Current Consumption			660	800	μA

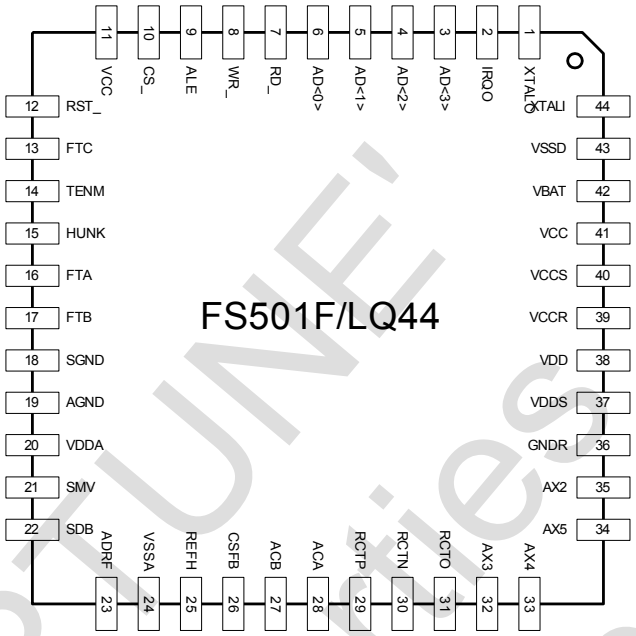
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Instrumentation Amplifier @ Gain = 30, Vref=0.5V, T_A=25℃					
Input Offset Voltage without AZ	Rs<100Ω		20		μV
Input Offset Voltage with AZ	Rs<100Ω		0	3	μV
Input Offset Drift without AZ	-20℃<T_A<+50℃		200		nV/℃
Input Offset Drift with AZ	-20℃<T_A<+50℃		20		nV/℃
Input Referred Noise	Rs=100 , 0.1Hz~1Hz		0.3	0.6	μVpp
Input Bias Current	[2]		100	300	pA
Current Consumption			180	220	μA
Regulator					
Analog Ground Source Capability	ΔV_O=-0.1V	15	20		μA
Analog Ground Sink Capability	ΔV_O=0.1V		3	5	mA
VBAT		5.5	9		V
Low Battery Detection Voltage		6.7	6.8	6.9	V
VDD Operating Current	V_{IN}=0, 500mV Scale		960		μA
Sleep Current			10	30	μA
Parasitic Capacitance			10	15	pF
Digital Output High	I_{OUT}=-1mA		5		V
Digital Output Low	I_{OUT}=1mA		25		mV
Digital Input High					V
Digital Input Low					V
Temperature Range					
Operating Temperature Range		-40	25	85	°C
Storage Temperature Range		-65	25	150	°C

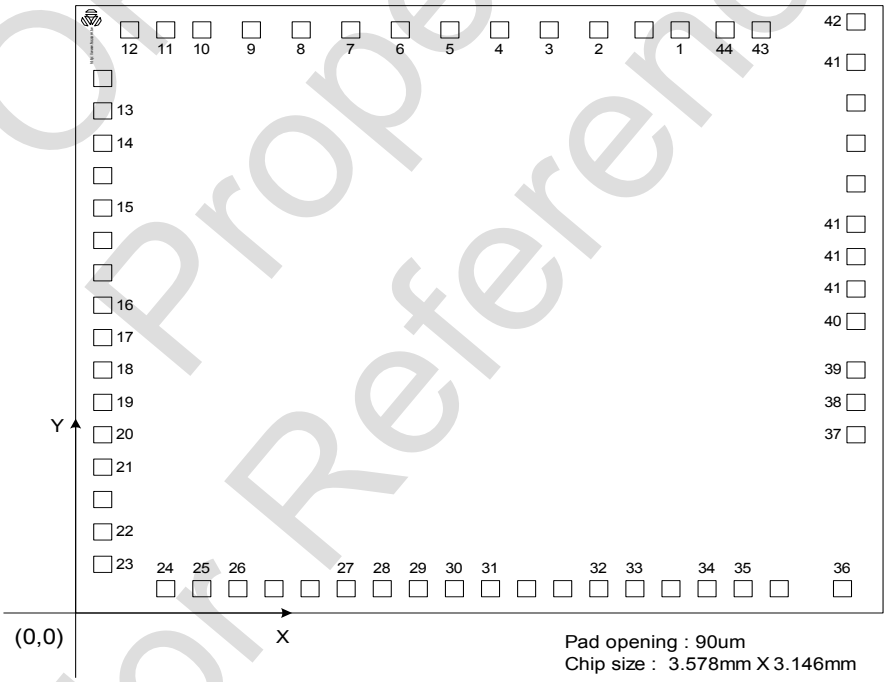
These parameters are guaranteed by design and are tested only by sampling while mass production.

While a voltage source with large output impedance is measured by an instrumentation amplifier having input bias current, an additional input offset voltage will be introduced. However, this offset voltage could be cancelled by mirrored offset cancellation technique.

3. Package and Terminal Assignments

Package and Terminal Assignment of LQFP44





Package： LQFP44 10*10

Dice size： 3.578*3.146 mm

Pad No.	Name	X[mm]	Y[mm]	Pad No.	Name	X[mm]	Y[mm]
1	XTALO	2.675	2.937	31	RCTO	1.828	0.209
2	IRQO	2.340	2.937	32	AX3	2.290	0.209
3	AD<3>	2.120	2.937	33	AX4	2.444	0.209
4	AD<2>	1.900	2.937	34	AX5	2.753	0.209
5	AD<1>	1.679	2.937	35	AX2	2.906	0.209
6	AD<0>	1.459	2.937	36	GNDR	3.282	0.209
7	RD_	1.255	2.937	37	VDDS	3.368	0.961
8	WR_	1.051	2.937	38	VDDS	3.368	1.110
9	ALE	0.847	2.937	39	VCCR	3.368	1.272
10	CS_	0.643	2.937	40	VCCS	3.368	1.503
11	VCC	0.496	2.937	41	VCC	3.368	1.674
12	RST_	0.349	2.937	41	VCC	3.368	1.845
13	FTC	0.209	2.468	41	VCC	3.368	2.016
14	TENM	0.209	2.313	41	VCC	3.368	2.761
15	HUNK	0.209	2.006	42	VBAT	3.368	2.952
16	FTA	0.209	1.544	43	VSSD	3.046	2.937
17	FTB	0.209	1.390	44	XTAL1	2.899	2.937
18	SGND	0.209	1.236				
19	AGND	0.209	1.082				
20	VDDA	0.209	0.935				
21	SMV	0.209	0.788				
22	SDB	0.209	0.480				
23	ADRF	0.209	0.325				
24	VSSA	0.449	0.209				
25	REFH	0.597	0.209				
26	CSFB	0.750	0.209				
27	ACB	1.213	0.209				
28	ACA	1.366	0.209				
29	RCTP	1.521	0.209				
30	RCTN	1.674	0.209				

Terminal Description

SOP 40	LQ 44	Attribute	Name	Function
1	18	AI	SGND	Signal Ground
2	19	API	AGND	Power Supply Ground for Analog Signal (+2.5 V)
3	20	API	VDDA	Power Supply VDD for Analog Signal（+5 V）
4	21	AIO	SMV	Input of Analog Signal
Na	22	AIO	SDB	Reference Resistance Bottom Input for the (Thermistor) Resistance Measuring
5	23	AI	ADRF	Input Reference Voltage of the ADC
6	24	API	VSSA	Power Supply VSS (0V) of the Analog Signal
7	25	AI	REFH	Reference Voltage Input of the Embedded Analog Power Source
8	26	AIO	CSFB	Current Source Feedback
9-10	27-28	AIO	ACB, ACA	ACBUF Op Amp Terminals
11-12	29-30	AIO	RCTP, RCTN	Inputs of RCTOP Op Amp
13	31	AIO	RCTO	Output of RCTOP Op Amp
14	32	AIO	AX3	Programmable Input Channel 3
Na	33	AIO	AX4	Programmable Input Channel 4
Na	34	AIO	AX5	Programmable Input Channel 5
15	35	AIO	AX2	Programmable Input Channel 2
16	36	APO	GNDR	Analog Ground Output of the Embedded Voltage Regulator (+2.5 V)
17	37	PO	VDDS	VDD Output Via Internal Switches
18	38	PI	VDD	VDD (+5V) Input for Voltage Regulator
19	39	DPO	VCCR	VCC (+5 V) Output from the Voltage Regulator
20	40	DPO	VCCS	VCC Output Via Internal Switches
21-22	41	DPI	VCC	Power Supply VCC (4~5V) for Digital Signal
Na	42	AI	VBAT	Input of Power Low Detector
23	Na	DO	OSCO	Crystal Oscillation Output. It can be used by the microprocessor directly.
24	43	DPI	VSSD	VSS (0V) for Digital Signal
25-26	44-1	DIO	XTALI, XTALO	Crystal Oscillator Inputs
27	2	DO	IRQO	Interrupt Output Signal for Measure Events
28-31	3-6	DIO	AD<3:0>	Data Input/Output of the Microprocessor Interface
32	7	DI	RD_	Read Terminal of the Microprocessor (Active Low Oriented)
33	8	DI	WR_	Write Terminal of the Microprocessor (Active Low Oriented)
34	9	DI	ALE	Address Latch Enable of the Microprocessor. When it is high, AD<3:0> is the address bus.
35	10	DI	CS_	Chip Select of the Microprocessor Interface (Active Low Oriented)
36	11	DPI	VCC	VCC (+4V) for Digital Signal
37	12	DI	RST_	Reset. It is low to reset all the internal registers to zero.
38	13	AIO	FTC	Terminal of the Pre RC Filter
Na	14-15	AIO	TENM, HUNK	Reference Resistance Terminals for the (Thermistor) Resistance Measuring
39-40	16-17	AIO	FTA, FTB	Terminals of the Pre RC Filter

Notations:

1. D stands for Digital.
2. A stands for Analog
3. P stands for Power.
4. stands for Output.
5. I stands for Input.
6. For example: DIO means “Digital Input/Output”

4. Microprocessor Interfaces

FS501 can be directly connected to any microprocessor by pins of CS_, WR_, RD_, ALE, AD<3>, AD<2>, AD<1>, AD<0>, and RQO. It can access the read/write of the control registers, handle interrupts, and access the measure registers.

Control Registers

The Control registers are to control the status of internal components, such as the status of the multiplexer, TAP of the digital filters, etc. All of them are 8-bit registers, and all of them are input/output ports that can be read and written by the microprocessor. When reset is activated (RST_= 0), all the control registers are rest to 0. The microprocessor can control the chip by setting the control registers, and read the values of the control registers to check the status of the chip.

Table 2. The Address of Control Registers and Interrupt Registers.

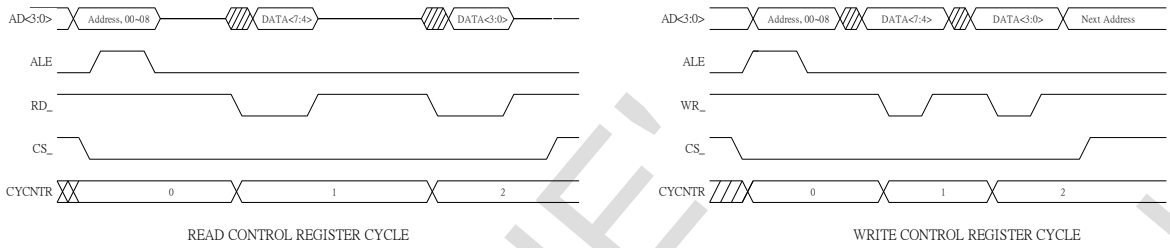
MSB									LSB
Address	Name	7	6	5	4	3	2	1	0
00	RGD<7:0>	0	0	HUNK	0	MODE<3:0>			
01	SIN<7:0>	SINH<3:0>				BPFTR	SINL<2:0>		
02	SRF<7:0>	0	0	SRFH<1:0>		FTR	SRFL<2:0>		
03	SCP<7:0>	SCMPH<3:0>				0	0	0	0
04	AFT<7:0>	1	RCTEN	ACDIV	ACEN	0	0	0	0
05	ADG<7:0>	ENAD	0	ADG<5:0>					
06	SETADC	ENVDS	ENVCS	CYS<1:0>		TPS2<1:0>		TPS1<1:0>	
07	MISC1<7:0>	0	FSDIV	1	ENOSCO_	ENXTL_	0	0	0
08	MISC2<7:0>	ENCP	0	0	LBO	0	0	ENGNDR_	ENLBS
09	INTRG<7:0>	0	0	INSTA<1>	INSTA<0>	0	0	INTEN<1>	INTEN<0>

Table 2 shows the control signals and the addresses of the control registers. There are 10 addresses, 00~09. The functions are briefly described in Table 3.

Table 3. Brief Description of the Function of FS501 Registers

Registers	Function	Refer to
MODE<3:0>	Selection of Thermistor or Voltage Measure	Section 7.1
RGD<5>	Selection of Thermistor Measure Switches	Table 8
SIN<7:0>	Input selection of the ADC and control signals of the pre filter.	Table 9 and Table 10
SRF<5:0>	Reference voltage selection of the ADC and control signals of the pre filter	Table 11 and Table 12
SCP<7:4>	Path selection of CMPH	Table 13
AFT<6:4>	Enable controls of the op amps	Fig. 8
ADG<5:0>	Input gain setting of the ADC	Section 8.2
ADG<7:6>	Job setting of the ADC	Section 8.6
SETADC<7:6>	ENVDS and ENVCS, programmable power supply setting.	Section 5.3
SETADC<5:4>	CYS<1:0>, ADC offset voltage elimination mode setting	Section 8.4
SETADC<3:0>	TPS2<1:0> and TPS1<1:0>, TPS2<1:0> and TPS1<1:0> are the high speed TAP and high resolution TAP setting of the digital filter.	Section 8.3
MISC1<6,4:3>	Setting of the clock generator	Table 7
MISC2<7>	ACBUF op amp switching mode	Section 7.3
MISC2<2>	If set, the CMPH signal will bypass ACBUF amplifier and directly output through ACA	Fig. 8
MISC2<4>, MISC2<0>	Setting of Power Low Detector	Section 5.4
MISC2<1>	ENGNDR_, the enable control of the output of internal power supply ground of the analog parts.	Section 5.2
INTRG<4>	Interrupt status register	Section 4.2
INTRG<0>	Enable control of IRQO	Section 4.2

The read/write timing sequences of all the control registers are shown in Fig. 1. The length of the data is 8-bit wide, therefore, it needs to read and write consecutively twice (MSB 4 bits first then LSB 4 bits). Otherwise, the activation of next ALE will reset the CYCNTR (cycle counter) and it will start from the MSB 4 bits of next instruction.



• *Fig. 1. The Read/Write Timing Diagram of the Control Registers*

Interrupt Process

If new data are converted by the ADC and are read by the interface of the microprocessor, that is new event occurred, this chip activates an interrupt signal through IRQO to the microprocessor to request for accessing.

When the microprocessor receives a negative edge-triggered interrupt signal, the measure register of FS501 has measured new data. The interrupt of the measured event is triggered by signal INTEN (as shown in Table 4).

• Table 4. Interrupt Status Register

INSTA	INSTA<1>	INSTA<0>
Event	High speed low resolution AD conversion	High resolution low speed AD conversion
INTEN	INTEN<1>	INTEN<0>
Function	Corresponding IRQO enable	Corresponding IRQO enable

When the microprocessor is reading data from the measure register, the corresponding interrupt bit is cleared to 0 to wait for next new measured data.

Interrupt status register, INSTA<0>, is a read-only register. Whereas interrupt enable register, INTEN<0>, is a read/write register. The read/write timing sequences of these two registers are the same as that of control registers (as shown in Fig. 1).

The interrupt procedures are as follows:

(1) When new data appear in the enabled measure register, IRQO is cleared to 0 and kept in 0.
(2) The microprocessor is activated by the negative edge of IRQO and then reads the contents of the interrupt status register.
(3) After the read of interrupt status register, IRQO is set to 1.
(4) Check IRQO. If it is not 1, the negative edge signal was not captured, and the microprocessor has to read the interrupt status register again.

When reading the interrupt register, the negative edge of the new interrupt signal may be lost. Step (4) may improve this problem. The value of the interrupt status register whether is refreshed or not is independent of interrupt enable register. The interrupt enable register only affects the IRQO output.

Measure Registers

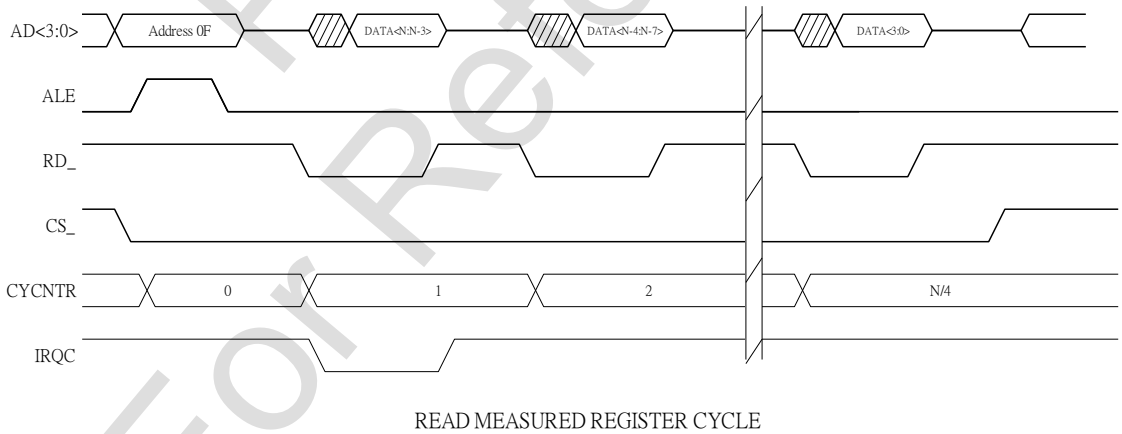
Table 5. Measure Register

Address	Name	Content	Register Length	Read Times
0E	SUM1<15:0>	Output of low resolution high speed ADC	16	4
0F	SUM1<23:0>	Output of low speed high resolution ADC	24	6

The measure register and the corresponding address of FS501 are shown in Table 5. It is an output for reading of the microprocessor.

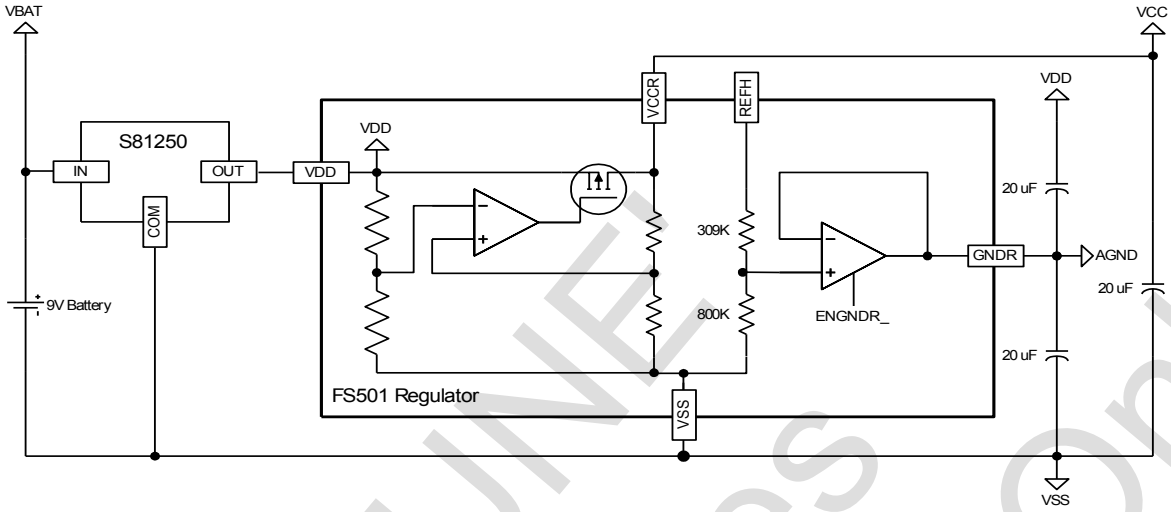
The read timing sequence of the measure register is shown in Fig. 2. The negative edge of IRQC will clear INSTA<0>. The read count for each read should be correct. Otherwise, the high ALE will clear CYCNTR (read/write cycle counter) to 0. The read count of the measure register is shown in the last column of Table 5.

When read the measure register, the low of RD_ should be longer than the sampling cycle of the ADC at the first read cycle. For other read cycles, the low of RD_ can be at least 2us. For example, the sampling rate of the ADC is 83.3kHz; then the first read cycle for reading the measure register should be greater than 12us.



● *Fig. 2. The Read Timing Sequence of Measure Register*

5. Voltage Regulator



• *Fig. 3. Block Diagram of FS501 Voltage Regulator*

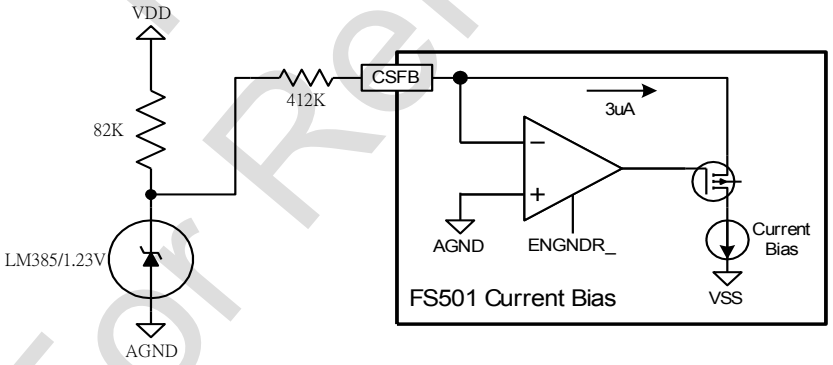
The block diagram of FS501 voltage regulator is shown in Fig. 3. In the circuit, we need a low cost voltage regulator, S81250, to regulate the battery voltage (more than 6.8V) to 6.4V VDD. The VDD power supply is used for: (1) analog circuit power supply, (2) as the reference voltage of the voltage regulator.

In Fig. 3, voltages VDD and REFH are used as reference voltages to generate VCCR, GNDR, and VSS for FS501. If VSS is set to 0V, then VCCR and GNDR will be regulated to 5V and 3.2V respectively.

Users can select the power supply source for FS501 by themselves, either generated internally or supplied externally. The power sources of analog circuits of FS501 are supported through terminals of VDDA, AGND, and VSSA. Therefore, we can directly connect the voltage regulator outputs of VCCR, GNDR, and VSS to terminals of VCC, AGND, and VSSA respectively. If the user can find stable power source externally, the power sources can be applied to terminals of VCC, AGND, and VSSA directly instead of internal power sources of VCCR and GNDR.

Most of the power consumption of the analog circuit is due to the static current. In FS501 the current of analog part is designed to be less than 1mA, and the current of digital part is less than 0.5mA .

Bias Current Source Generator



• *Fig. 4. FS501 Bias Current Source Generator*

The bias current source generator as shown in Fig. 4 generates the bias current for all the analog circuits of FS501. If the embedded op amp works, CSFB will be pulled to AGND by the feedback; there are 1.2V in resistor 412K, and 3uA bias current can be obtained. If the value of the 412K-resistor is reduced, the working current of the chip will be increased, and some of the specs can be improved.

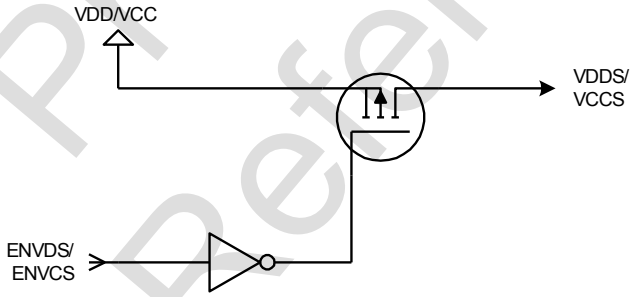
Power Saving Mode

In FS501 except VCCR generator, the user can use the control registers to turn off part of the circuits to reduce power consumption. The control signals related to power saving are shown in Table 6. If we turn off all the devices (circuits) but keep VCCR active, shown in Table 6, the total current of FS501 chip will be less than 10uA

Table 6. Setting of the Power Saving Mode

Register	Control Name	Power-Saving Setting	Power Consumption Circuit
AFT<6>	RCTEN	0	Op Amp
AFT<4>	ACEN	0	Op Amp
ADG<7>	ENAD	0	ADC
SETADC<7:6>	ENVDS, ENVCS	00	Switching Power Output
MISC1<4>	ENOSCO_	1	OSCO Output
MISC1<3>	ENXTL_	1	Crystal Oscillator
MISC2<1>	ENGNDR_	1	GNDR Voltage Regulator

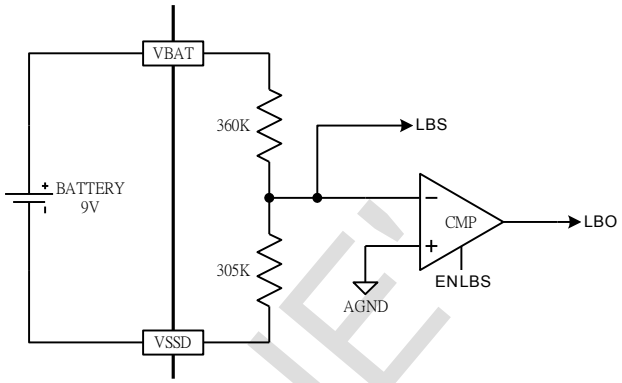
Switchable Power Output



• *Fig. 5. Switchable Power Output*

Terminals of VDDS and VCCS are the switchable power outputs of VDD and VCC respectively, and the circuit diagram is shown in Fig. 5. VDD/VCC is fed in the PMOS switch, and VDDS/VCCS is the output. The PMOS switch is controlled by ENVDS/ENVCS control signal. Signals 0 and 1 will turn on and turn off the PMOS switch respectively.

Power Low Detector



● *Fig. 6. Power Low Detector*

Power low detector is shown in Fig. 6. LBS is the dividing voltage of VBAT and is fed into the input of the power low detector. The output voltage, LBO, of the power low detector can detect whether the dividing voltage of VBAT is less than AGND. If it is less than AGND, LBO is high and the user has to replace the battery. Before reading LBO, we have to set ENLBS to Hi (high), and pull ENLBS to low after approximately 0.1ms; we can then read LBO.

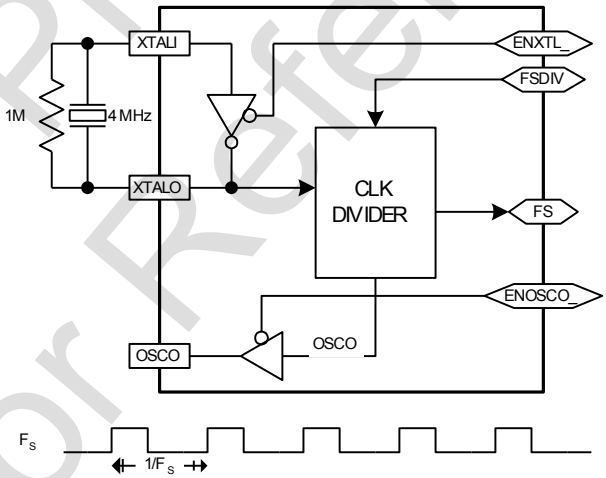
By the ADC multiplexer, the LBS voltage can be selected by the ADC, and by Equation 1 the LBS voltage can be found.

Equation 2 $$V_{BAT} \approx 2.2 \times V_{LBS}$$

In power saving mode, we can set ENGDR_ (MISC<1>) to high to turn off GNDR to save power consumption.

6. Clock Generator

Clock Generator



● *Fig. 7. Clock Generator*

The block diagram of the clock generator is shown in Fig. 7. We connect a 4MHz crystal oscillator to the clock generator to generate a 4MHz clock frequency. A frequency divider is used to divide the clock signal to generate a signal FS, and the ADC uses this FS signal to do data conversion. FS is controlled by ENXTAL_ and

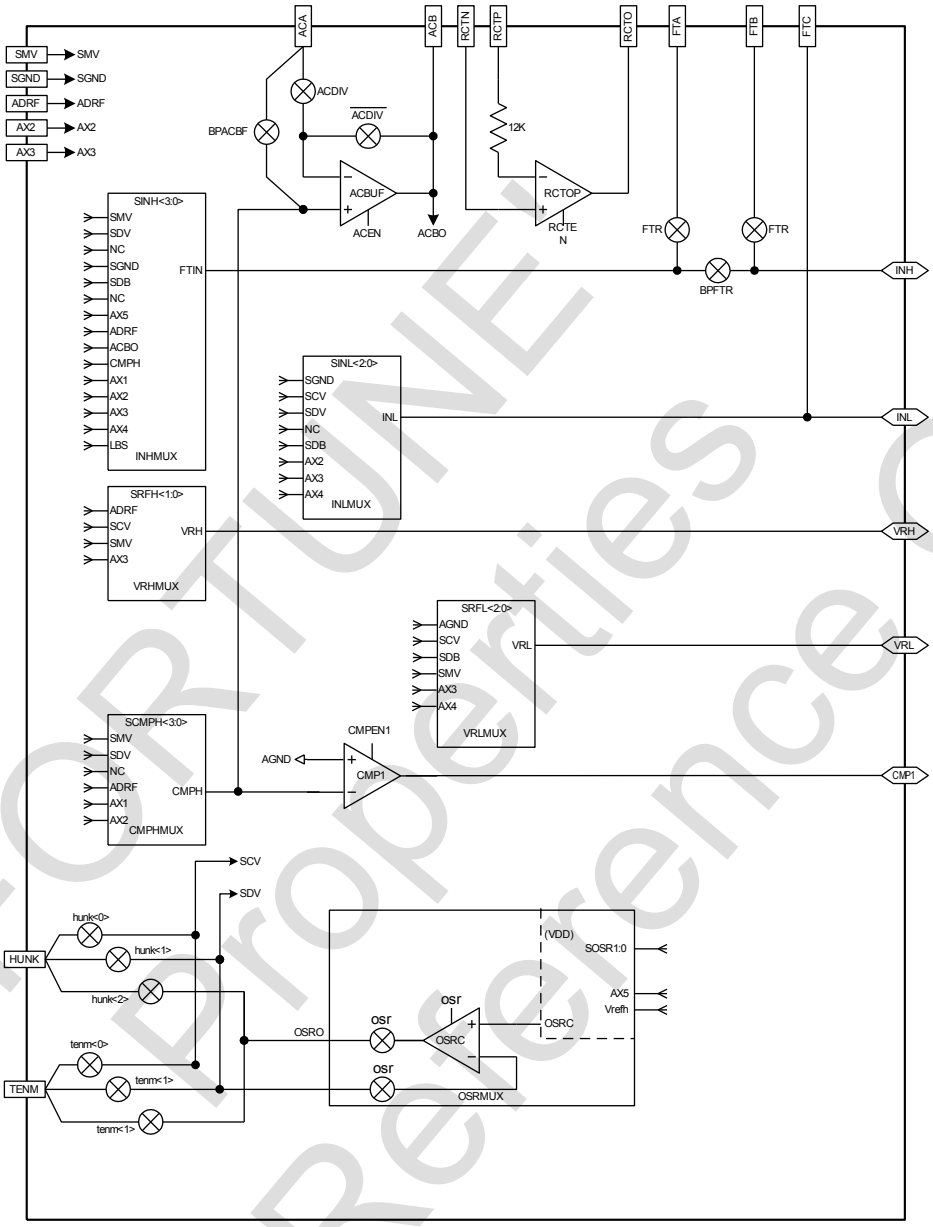
FSDIV; the truth table is shown in Table 7.

- Table 7. Truth Table of the FS Generation

ENXTAL_	FSDIV	F_S
L	L	166.67 kHz
L	H	83.33 kHz
H	X	0, (L)

When ENOSCO_=0, the output is a fixed 2.000 MHz square wave. When ENOSCO_=1, the output is 0, and can save VCC power consumption.

7. Function Network

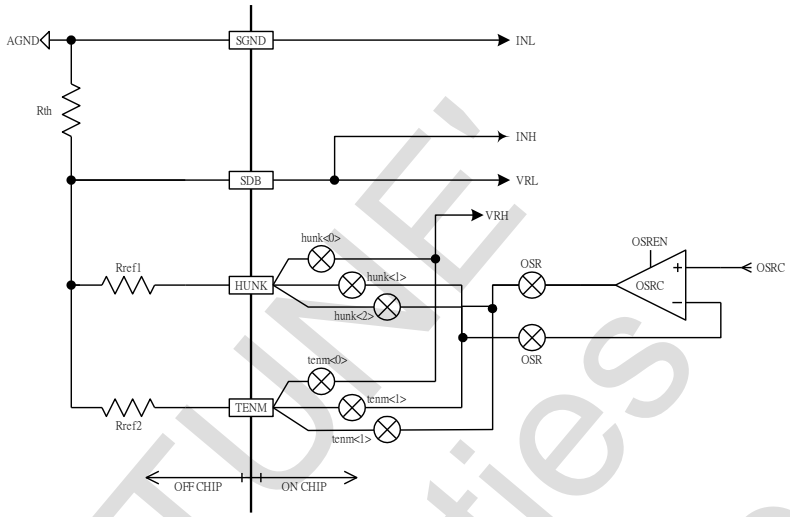


● *Fig. 8. Function Network of FS501*

The function network is shown in Fig. 8. There are multiplexers, op amps, and comparators. Control registers can set multiplexers, INHMUX, INLMUX, VRHMUX, VRLMUX, and SCMPHMUX, to select working channels. The op amps, ACBUF and RCTOP, can be used as the amplifier or input voltage buffer. OSRC is the embedded Ohm voltage source for resistance measuring. The comparator is to compare the input signal with AGND, and the output can be read through the register.

Measure Mode

FS501 has voltage measuring and resistance measuring modes, and the modes are controlled by 00F register MODE3:0. When MODE=0, it is in the voltage measuring mode. The measured voltage can be either directly fed from INHMUX to ADC, or fed through the ACBUF amplifier and then fed to the ADC.



• *Fig. 9. Resistance Measuring Circuit*

When MODE=1, it is in the resistance measuring mode. The circuit is shown in Fig. 9. Suppose that the reference resistance is R_{ref}, and the measured resistance to be R_{th}. The measuring equation is as follows.

Equation 3

$$R_{th} = R_{ref} \times \frac{V_{INH} - V_{INL}}{V_{VRH} - V_{VRL}} = G \times D_{out}$$

Where D_{out} is the ADC output, and thereafter the resistance can be measured. The control setting of the resistance measuring circuit is shown in Table 8.

• Table 8. Setup Table of the Resistance Measuring Circuit

Range Mode	MODE3:0	HUNK	hunk2:0	tenm1:0
HUNK	1001	1	111	00
TENM	1001	0	000	11

Multiplexer and Pre-filter

Multiplexers of INHMUX, INLMUX, VRHMUX, and VRLMUX can select the inputs of FTIN, INL, VRH, and VRL to the ADC. Where FTIN and INL are outputs. These two signals will go through a RC pre-filter and then are connected to the fully differential inputs, INH and INL, of the ADC. They can also bypass the RC filter by control of BPFTR and FTR, and are connected to the ADC directly. The control registers control all the selections. The control registers and the selections are shown in Tables 9, 10, 11, and 12.

Table 9. Setting of INH Multiplexer

Name	SMV	SGND	ADRF	ACBO	CMPH	AX2	AX3
SINH	0000	0011	0111	1000	1001	1011	1100

Table 10. Setting of INL Multiplexer

Name	SGND	AX2	AX3
SINL	000	101	110

Table 11. Setting of VRH Multiplexer

Name	ADRF	SMV	AX3
SRFH	00	10	11

Table 12. Setting of VRL Multiplexer

Name	AGND	SMV	AX3
SRFL	000	011	100

Multiplexer CMPH (CMPHMUX) can select signals to op amp ACBUF. The control registers and selections are shown in Table 13.

Table 13. Setting of CMPH Multiplexer

Name	SMV	ADRF	AX2	SGND	AGND	VRH	VRL
SCMPH	0000	0011	0101	1100	1101	1110	1111

Operation Amplifier (Op Amp)

1) ACBUF Op Amp

Op amp of ACBUF, control switch of ACDIV and the external resistors can form a gain loop.

Operation of ACBUF is controlled by register ACEN. When ACEN=0, the op amp is turned off and the output is in high impedance.

The gain of ACBUF is set by control register ACDIV. When ACDIV=0, the gain is 1. When ACDIV=1, the gain of the op amp is determined by the external resistance.

2) RCTOP Op Amp

RCTOP op amp is enabled by control register RCTEN. When RCTEN=0, the op amp is turned off to save power.

Ohm Voltage Source

The supplied voltages of the Ohm voltage source are shown in Table 14 and they are directly fed into the attenuating network. The output of the Ohm voltage source is controlled by SOSR1:0. The value of SOSR1:0 can be directly set by the control register.

When the output of the Ohm voltage source is VDD, the switch resistor in the loop will affect the voltage of the chip driving terminator. Therefore, the load affects the effective load voltage.

Because of the high gain op amp and negative feedback, outputs other than VDD will not be affected by the switch resistor. The effect of load in the circuit can be neglected, and the maximum supplied current is around ±1.2mA.

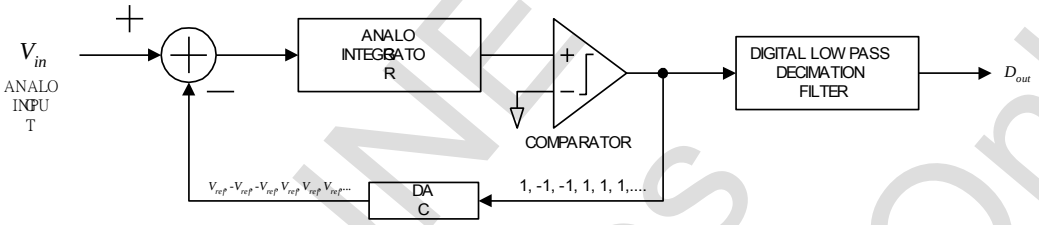
Table 14. Control Values of the Ohm Voltage Source

INPUT		OUTPUT
MODE3:0	SOSR1:0	OSRO
1001	00	high impedance
1001	01	AX5
1001	10	Vrfh
1001	11	VDD

8. Analog to Digital Converter (ADC)

The Operation of the Delta-Sigma (ΔΣ) Modulator ADC

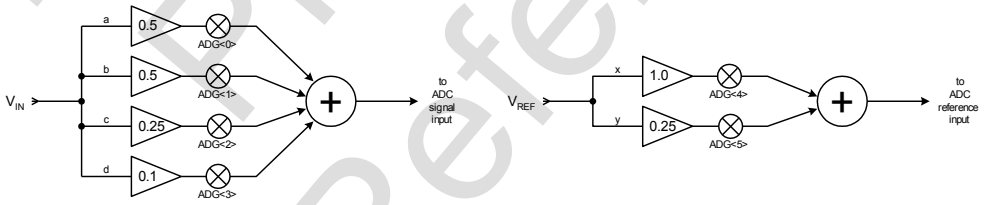
This high resolution ADC is designed by the technology of delta-sigma (ΔΣ) modulator. The continuous analog signals are sampled by a very high sampling rate that is much higher than the bandwidth of the input signal. The delta-sigma modulator converts the input signal to a series of 1-bit codes. These 1-bit codes are then fed to the digital filter to filter out the high frequency quantization noise to find high resolution digital outputs. It can be used in the high resolution digital multimeters. This kind of ADC quantizes one bit in the analog part, therefore, it has very good linearity. Because it is in a fully differential configuration, the common mode rejection ratio (CMRR) is very high and can reduce the common mode signals effectively.



● *Fig. 10. The Symbolic Diagram of the Delta-Sigma Analog-to-Digital Converter*

The symbolic diagram of the delta-sigma ADC is shown in Fig. 10. It consists of an analog subtractor, an integrator, a comparator, a 1-bit digital-to-analog converter (DAC), and a low-pass digital filter. The analog signals are continuously sampled and are subtracted by the expected voltage. The difference of the signals is fed into the integrator, and then the signal is compared with a reference voltage to find a digital output. This digital output is converted by the 1-bit DAC to become an analog signal ($+V_{ref}$ or $-V_{ref}$) and then negatively fed back into the integrator. Due to the infinitive DC gain of the integrator, if the change of the input signal is much slower than the sampling speed, the average voltage obtained by the delta-sigma modulator will be very close to the input signal. In some resolution they can be treated to be the same, therefore, the 1-bit output data from the comparator are equivalent to the $\pm V_{ref}$ analog signal values. The digital filter then decimates the 1-bit data to get a very high resolution digital code.

Gain Stage Setting



● *Fig. 11. Diagram of FS501Gain Stage Setting*

There are four different gain paths to the input of the FS501 ADC, and they are controlled by control register ADG<3:0>; the block diagram is shown in Fig. 11. Two different gain paths control the input reference voltage, and they are controlled by control register ADG<5:4>. The gains shown here are not accurate. The accurate gains can be found by careful calibration.

By proper selection of the gain paths, this ADC can be applied to the optimum dynamic range for all the measuring applications. Table 15 shows values of ADG<5:0> for three frequently used applications.

Table 15. FS501 ADC Typical Gain Setting

	First Scale	Second Scale	Third Scale
ADG<5:0>	01_0011	11_0111	11_1000
Reference Voltage Gain（G_{REFi}）	×1.0	×1.25	×1.25
Input Voltage Gain（G_{SIGi}）	×1.0	×1.25	×0.1

The transfer function for each scale is as follows,

Equation 4 $$D_x = \frac{G_{SIG_i}}{G_{REF_i}} \times \frac{v_x}{v_{re}}$$

The gains for the reference voltages and input voltages shown in Table 15 are approximate values. The accurate gains for the reference voltages and input voltages can be found by careful calibration.

Digital Filter

In Fig. 10, the 1-bit output of the comparator should be fed to the digital low pass filter to do decimation to find the high resolution multiple-bit digital output. The transfer function of the FS501 digital filter is:

Equation 5

$$\left|H(f)\right| = \frac{1}{N^2}\left(\frac{\sin(N\pi f / f_S)}{\sin(\pi f / f_S)}\right)^2$$

Where N is TAP of the digital filter.

Suppose the sampling rate of the ADC is 166KHz, the TAP of the digital filter is 16600. We can find the frequency response diagram of the digital filter as shown in Fig. 12. The first zero is at:

Equation 6

$$f_{Z1} = \frac{f_S}{N} = \frac{166000\ \text{Hz}}{16600} = 10\ \text{Hz}$$

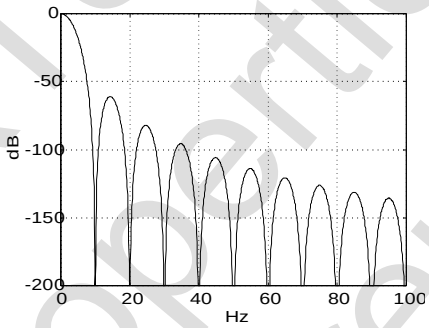


Fig. 12. The Frequency Response Diagram of FS501 Digital Filter

The zero points fall at multiples of 10Hz. The digital filter will filter out all the signals near the zero points. From Fig. 12, we can find that the noises at 50Hz and 60Hz are suppressed very well. If the sampling rate is 83KHz and the TAP of the filter is 16600, the first zero-frequency is at 5Hz.

There are two programmable TAP digital filters in FS970x, and they are COMB1 and COMB2; the outputs are SUM1 and SUM2 respectively. The TAP of COMB1 is higher than that of COMB2; therefore COMB1 is used for high resolution measuring, and COMB2 is used for low resolution but high speed measuring.

The TAP's of COMB1 and COMB2 are programmable, and can be set by TPS1 and TPS2 respectively; they are shown in Table 16. The first zero-frequency is computed by taking 83.3 kHz as sampling frequency and applies Equation 5. At TPS1=TPS2=11, the resolutions of high speed and low speed are 18-bit and 12-bit respectively. The resolutions for other conditions are according to the actual measuring.

Table 16. TAP Setting of the Comb Digital Filter and the First Zero Frequency [FS=83.3 kHz]

	COMB1（TPS1）		COMB2（TPS2）	
TPSX<1:0>	TAP（N）	First Zero Frequency（Hz）	Tap（N）	First Zero Frequency（Hz）
11	16384	5	256	325
10	8192	10	128	650
01	4096	20	64	1300
00	2048	40	32	2600

Reading and Calculating of Digital-to-Analog Converter

Due to the manufacture process drift, there is an offset voltage in the FS501 ADC such that an offset value is existed in the ADC output. In order to eliminate the offset value, FS501 provides three operation modes, which can be set by CYS <1:0> of control register SETADC. The SUM1 output and calculation are different in different operation modes, and they are described in the following subsection.

8.4.1 ADC Output SUM1

Set CYS<1:0>=00, the ADC inputs are short circuited, and we can find the negative offset voltage of the ADC from SUM1.

Set CYS<1:0>=11, as described by Equation 3 and we can find the equivalent voltage of the input signal from SUM1.

Set CYS<1:0>=01, and the SUM1 output is the value of an ideal ADC. The transfer function is Equation 1. This mode is suitable for high resolution measurement.

When CYS<1:0>≠01, the output rate of SUM1 is the first zero frequency, f_{Z1}, of COMB1 as described in Equation 6. When CYS<1:0> =01, the output rate equals $f_{Z1}/2$.

The Conversion of the Digital Codes and Equivalent Voltage

The output of the FS501 ADC is SUM1<23:0>, which is a 24-bit 2's complement number. SUM1<23> is the sign bit; 0 represents a positive number, and 1 represents a negative number. The decimal point lies in between SUM1<22> and SUM1<21>.

If SUM1<23:0>=0010_1000_0000_0000_0000_0000, the equivalent floating point number is:

$$\begin{aligned} \text{SUM1} &= 00.10\_1000\_0000\_0000\_0000\_0000 \\ &= 1\times 2^{-1} + 0\times 2^{-2} + 1\times 2^{-3} + 0\times 2^{-4} + 0\times 2^{-5} + ...+ 0\times 2^{-22} \\ &= 0.5 + 0.125 = 0.625 \end{aligned}$$

Equation 7

If SUM1<23:0>=1101_1111_1111_1111_1111_1111, the equivalent floating point number is:

$$\begin{aligned} \text{SUM1} &= 11.01\_1111\_1111\_1111\_1111\_1111 \\ &= -(00.10\_0000\_0000\_0000\_0000\_0001) \\ &= -(1\times 2^{-1} + 0\times 2^{-2} + 0\times 2^{-3} + 0\times 2^{-4} + ...+ 1\times 2^{-22} \\ &= -0.5000002384 \end{aligned}$$

From Equation 1, if gain $G^{'}$ equals 1 and reference voltage V_{ref}=1.00000V, the value of SUM1, 0010_1000_0000_0000_0000_0000, can be used to calculate the measured voltage as:

$$v_x = \frac{V_{ref}}{G^{'}} \times D_x = \frac{1.00000\ \text{V}}{1} \times 0.625 = 0.62500\ \text{V}\ 。$$

If SUM1=1101_1111_1111_1111_1111_1111, the measured voltage can be calculated:

$$v_x = \frac{V_{ref}}{G^{'}} \times D_x = \frac{1.00000\ \text{V}}{1} \times -0.5000002384 = -0.50000\ \text{V}\ 。$$

However, due to the manufacture process drift $G^{'}$ is not exactly equal to 1, and there will be around $\pm 1\%$ offset. Similarly the reference voltage source and resistors may affect the reference voltage V_{ref}, and make V_{ref} not to be exact 1.00000V. Therefore, we have to calibrate the ADC.

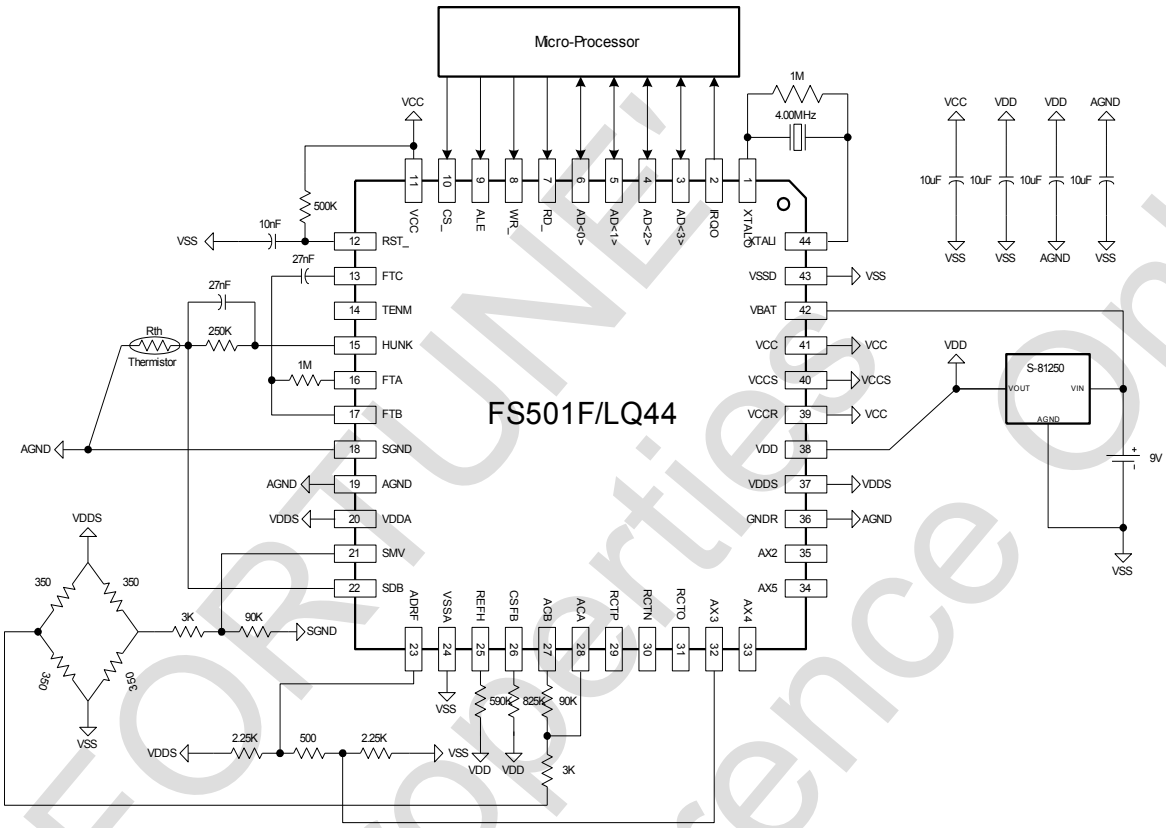
Other Control Setting

ENAD(ADG<7>) is the enable control signal for the ADC. It is 1 to enable the ADC; it is 0 to turn off the ADC and can save power.

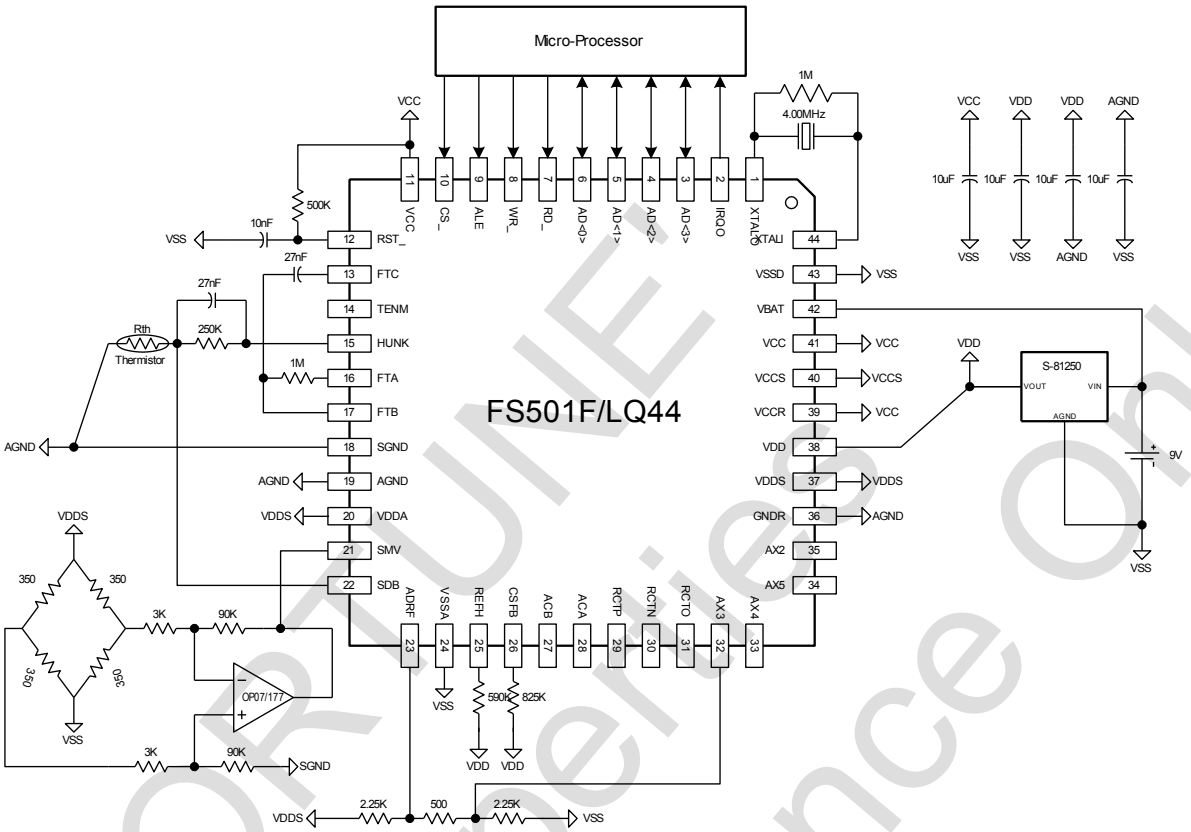
CPVR(ADG<6>) is the enhancement mode for resistance measuring. It is set to 1 to improve the linearity when measuring resistance.

9. Application Information

Application Circuit of Electronics Scale (Using Internal OP)

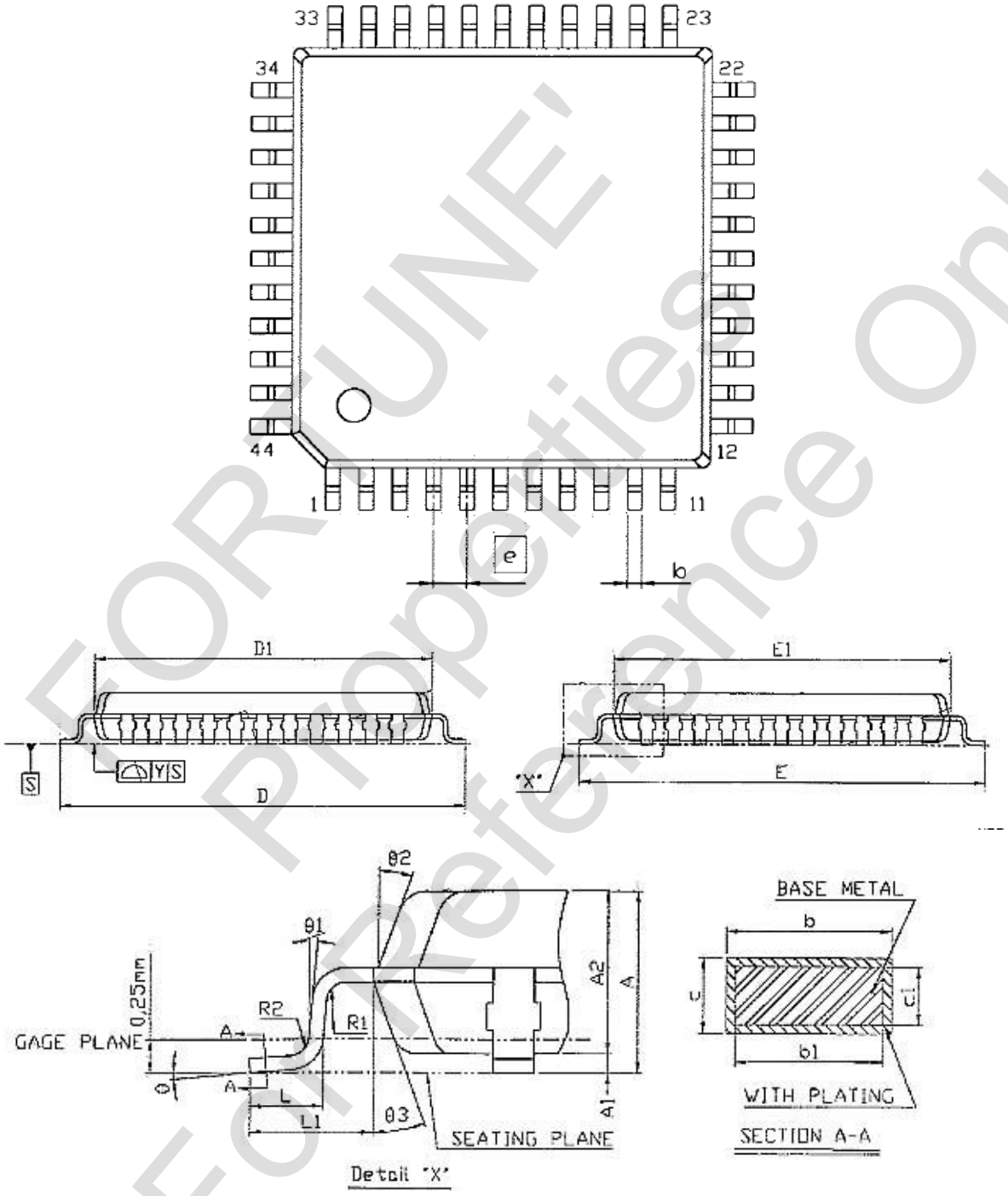


Application Circuit of Electronics Scale (Using External OP)



10. IC Dimension

Max. Rated Value



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.30	0.37	0.45	12	15	18
b1	0.30	0.35	0.40	12	14	16
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	12.00 BSC			472 BSC		
D1	10.00 BSC			394 BSC		
E	12.00 BSC			472 BSC		
E1	10.00 BSC			394 BSC		
e	0.80 BSC			31.5 BSC		
L	0.45	0.60	0.75	10	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

11. Ordering Information

Product Number	Description	Package Type
FS501F		Die form (44 pins)
FS501F		44-pin LQFP (Not Pb free package)
FS501F-PCD	44-pin LQFP Pb free package part number.	44-pin LQFP (Pb free package)

12. Revision History

Version	Date	Page	Description
3.8	2004/04/16	30	Reformat and correct the contents Add ordering information.
3.9	2005/08/02	32	Correct 1 low noise OPAMP to two low noise OPAMPs. Revise ordering information. Add Pb free package part number. Add Revision History.
4.0	2006/12/21	All	Revise datasheet format
4.1	2014/05/22	2	Revised company address