GENERAL DESCRIPTION

OB3396 is a primary side regulation off-line LED lighting controller which can achieve accurate LED current. It significantly simplifies LED lighting system design by eliminating the secondary side feedback circuitry. Proprietary Constant Voltage (CV) and Constant Current (CC) control is integrated as shown in the figure below.

The LED current (CC control) can be adjusted externally by the resistor Rs at SOURCE pin. Device operates in PFM in CC mode as well at large load condition and it operates in PWM with frequency reduction at light/medium load.

OB3396 offers comprehensive protection coverage with auto-recovery features including Cycle-by-Cycle current limiting, VDD OVP, VDD clamp and UVLO. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

OB3396 is offered in DIP8 package.

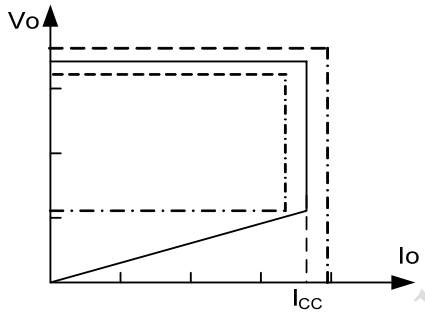


Fig.1. Typical CC/CV Curve

FEATURES

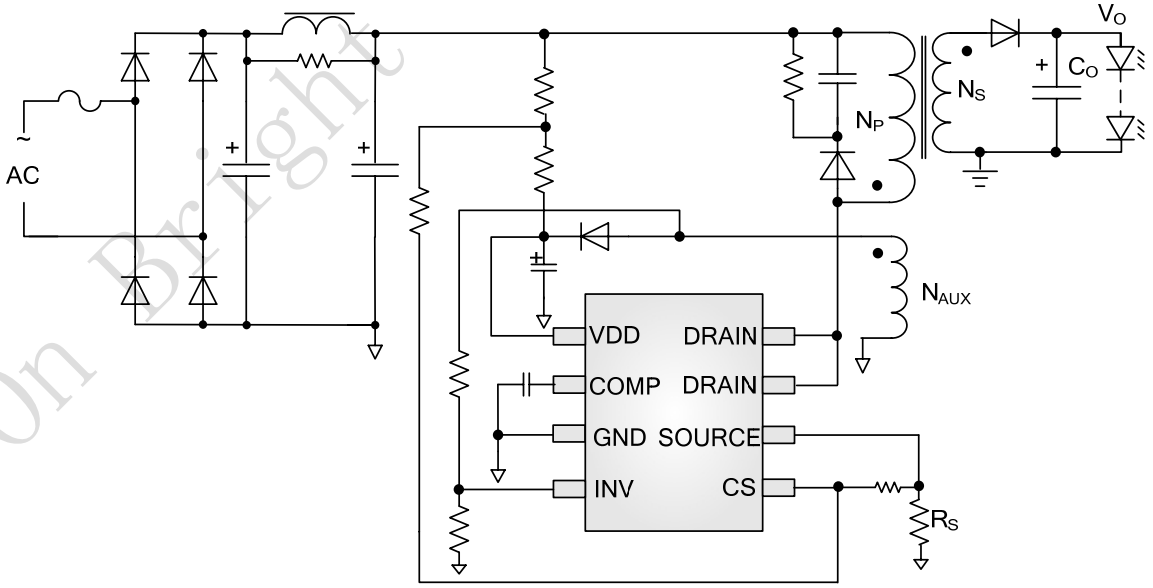
- High Precise Constant Current Regulation at Universal AC input
- Primary-side Sensing and Regulation Without TL431 and Opto-coupler
- Programmable CC Regulation
- Adjustable Constant Current and Output Power Setting
- Built-in Secondary Constant Current Control with Primary Side Feedback
- Built-in Adaptive Current Peak Regulation
- Built-in Primary winding inductance compensation
- Power on Soft-start
- Built-in Leading Edge Blanking (LEB)
- Cycle-by-Cycle Current Limiting
- VDD Under Voltage Lockout with Hysteresis (UVLO)
- VDD OVP
- VDD Clamp

APPLICATIONS

Low Power AC/DC offline SMPS for

- LED applications

TYPICAL APPLICATION

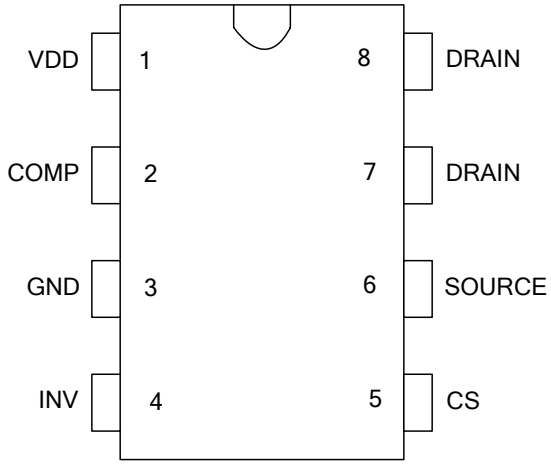


OB3396

GENERAL INFORMATION

Pin Configuration

The pin map is shown as below for DIP8.



Ordering Information

Part Number	Description
OB3396AP	DIP8, Pb-free, Tube

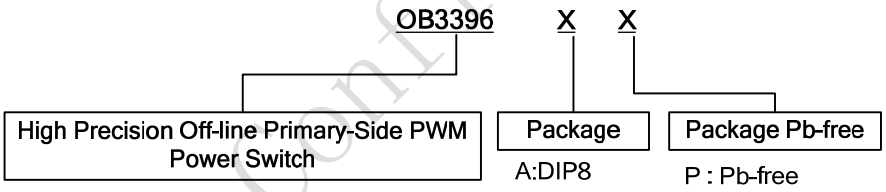
Package Dissipation Rating

Package	RθJA (℃/W)
DIP8	75

Absolute Maximum Ratings

Parameter	Value
Drain Voltage(off state)	-0.3 to BVdss
VDD Voltage	-0.3 to V_{DD}_clamp
VDD Zener Clamp Continuous Current	10 mA
COMP Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
INV Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



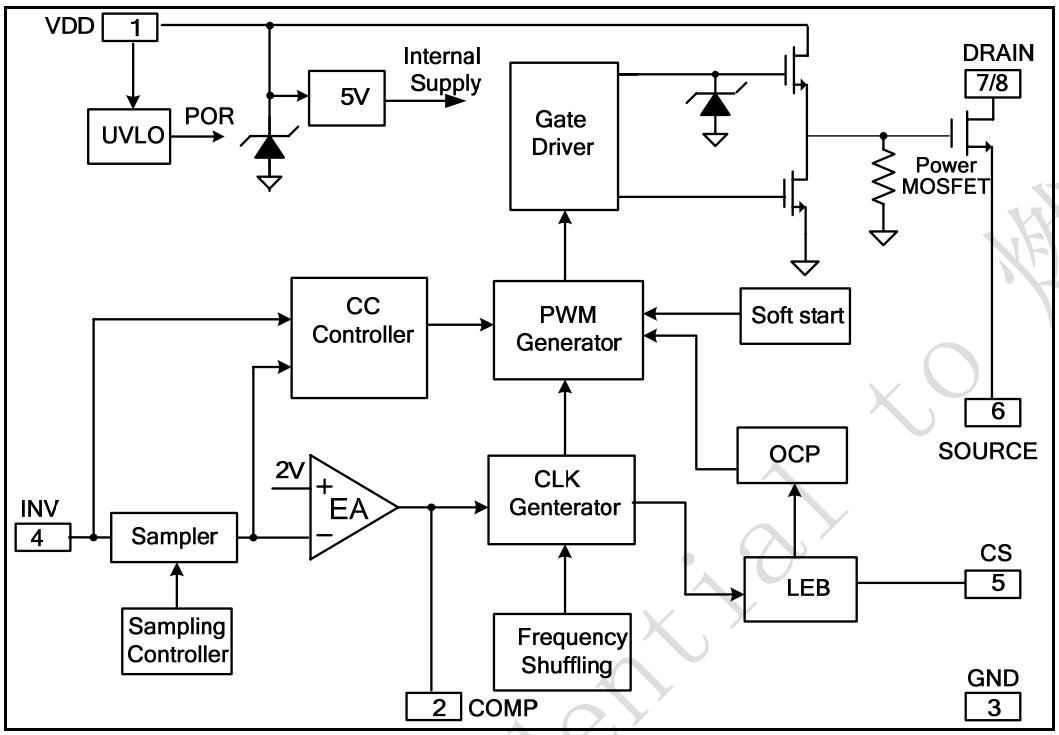
Marking Information

Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
A:DIP8 Package
P:Pb-free Package
S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	VDD	P	Power Supply
2	COMP	I	Loop Compensation
3	GND	P	Ground
4	INV	I	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
5	CS	I	Current sense input.
6	SOURCE	I	HV MOSFET Source
7,8	DRAIN	O	HV MOSFET Drain

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

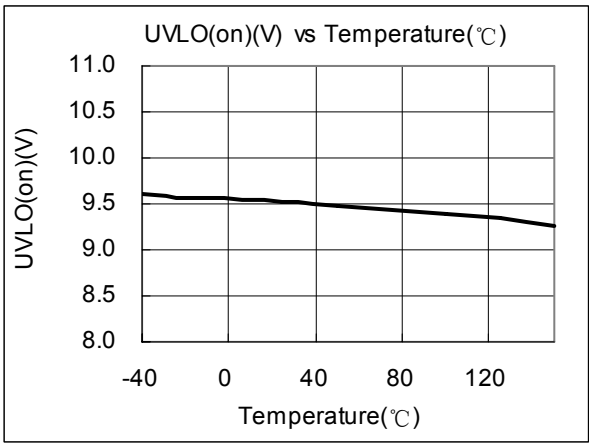
(TA = 25℃, VDD=VDDG=16V, if not otherwise noted)

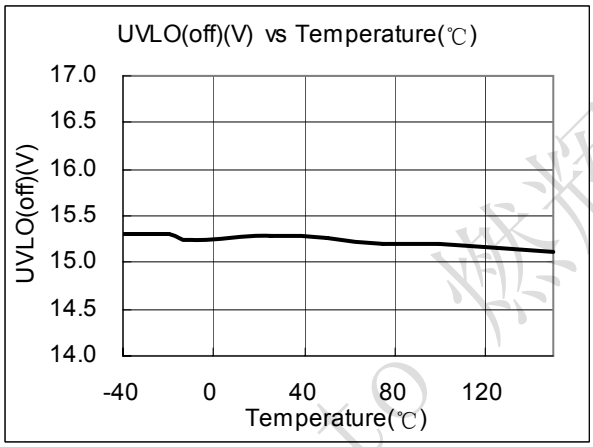
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
$I_{DD\ ST}$	Startup Current	VDD=13V		5	20	uA
$I_{DD\ op}$	Operation Current	Operation supply current INV=2V, CS=0V, VDD=VDDG=20V	-	2	3	mA
UVLO(ON)	VDD Under Voltage Lockout Enter	VDD falling	8.6	9.4	10.6	V
UVLO(OFF)	VDD Under Voltage Lockout Exit	VDD rising	13.9	15.2	16.4	V
V_{DD}_clamp	Maximum VDD operation voltage	I_{DD}=10mA	27	28.5	30	V
OVP	Over voltage protection Threshold	Ramp VDD until gate shut down	26	27.5	29	V
Current Sense Input Section						
TLEB	LEB time			625		ns
Vth_oc	Over current threshold		785	800	815	mV
Td_oc	OCP Propagation delay			110		ns
Z_{SENSE}_IN	Input Impedance		50			Kohm
T_ss	Soft start time			17		ms
Frequency Section						
Freq_Max[Note 1]	IC Maximum frequency		60	65	70	KHz
Freq_Nom	System Nominal switch frequency			50		KHz
Freq_startup		INV=0V, Comp=5V		14		KHz
△f/Freq	Frequency shuffling range			+/-6		%
Error Amplifier section						
Vref_EA	Reference voltage for EA		1.96	2	2.04	V
Gain	DC gain of EA			60		dB
Power MOSFET Section						
BVdss	MOSFET Drain-Source Breakdown Voltage		600			V
Rdson	On Resistance	Static, Id=1.0A		4.4	5.5	Ω

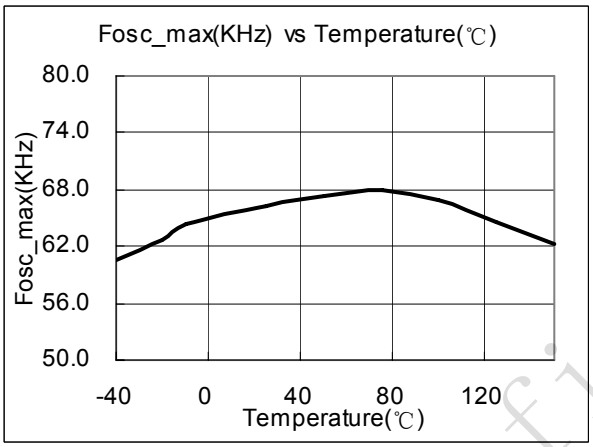
Note:

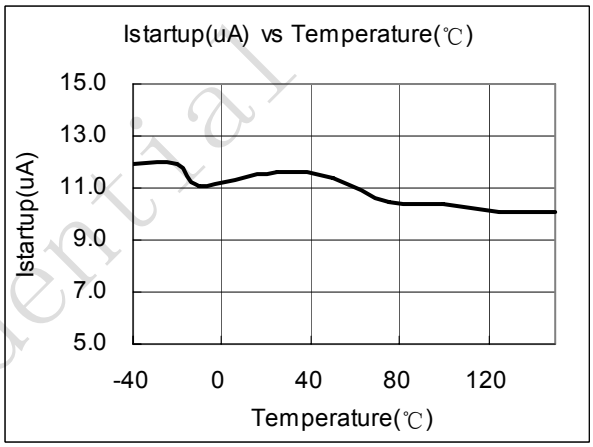
1. Freq_Max indicates IC internal maximum clock frequency. In system application, the maximum operation frequency of 65KHz nominal occurs at maximum output power or the transition point from CV to CC.

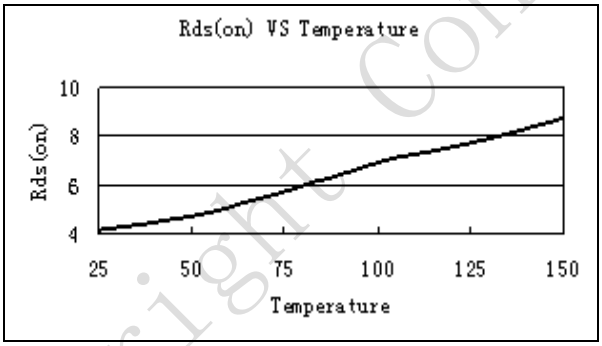
CHARACTERIZATION PLOTS











OPERATION DESCRIPTION

OB3396 is a cost effective PWM controller optimized for off-line LED lighting applications which can achieve LED current. Based on flyback converter topology working in DCM mode, It operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. Proprietary built-in CC control can achieve high precision LED current meeting LED lighting application requirements.

- **Startup Current and Start up Control**

Startup current of OB3396 is designed to be very low so that VDD could be charged up above UVLO threshold and starts up quickly. A large value startup resistor can therefore be used to minimize the power loss in application.

- **Operating Current**

The Operating current of OB3396 is as low as 2.0mA. Typical good efficiency is achieved with the low operating current together with 'Multi-mode' control features.

- **Soft Start**

OB3396 features an internal soft start to minimize the component electrical over-stress during power on startup. As soon as VDD reaches UVLO (OFF), the control algorithm will ramp peak current voltage threshold gradually from nearly zero to normal setting of 0.8V. Every restart is a soft start.

- **Principle of CC Operation**

To support OB3396 proprietary CC control, system needs to be designed in DCM mode for flyback system (Refer to Typical Application Diagram on page1). The LED output current I_{LED} is given by:

$$I_{LED} = \frac{1}{2} L_P \cdot F_{SW} \cdot I_{PK}^2 \cdot \eta \Big/ (V_O + V_F) \qquad (1)$$

Where Lp indicates the inductance of primary winding, Ipk is the peak current of primary winding and V_F is the diode forward voltage drop of the secondary .

Refer to the equation 1, the change of the primary winding inductance results in the change of the constant output current. To compensate the change from variations of primary winding inductance, the switching frequency is locked by an internal loop such that the switching frequency is

$$F_{SW} = \frac{1}{2T_{Demag}} \qquad (2)$$

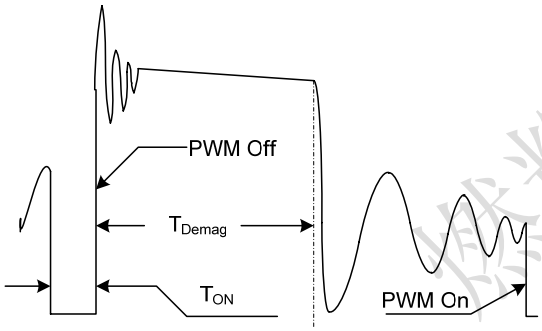


Figure.1 Auxiliary voltage waveform

Since T_{Demag} is inversely proportional to the inductance, as a result, the product *Lp* and *fsw* is constant, thus output current will not change as primary winding inductance changes. Up to ±7% variation of the primary winding inductance can be compensated.

The output LED current is

$$I_{LED} = \frac{\eta}{4} \cdot N \cdot \frac{V_{th\_oc}}{R_s} \qquad (3)$$

Where N is the ratio of transformer between primary side winding and secondary winding.

- **Adjustable CC point and Output Power**

In OB3396, the CC point and maximum output power can be externally adjusted by external current sense resistor Rs at SOURCE pin as illustrated in Typical Application Diagram. The output power is adjusted through CC point change. The larger Rs, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig.2.

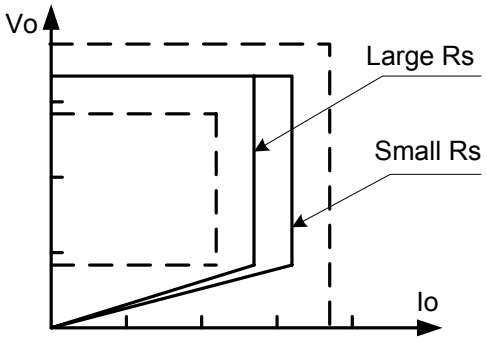


Fig.2 Adjustable output power by changing Rs

- **Operation switching frequency**

The switching frequency of OB3396 is adaptively controlled according to the load conditions and the operation modes. No external frequency setting components are required. The operation switching frequency at maximum output power is set to 65K

Hz internally.
For flyback operating in DCM, The maximum output power is given by

$$P_{O\max} = \frac{1}{2}\eta L_P F_{SW} I_{pk}^2 \quad (4)$$

Where Lp indicate the inductance of primary winding and Ip is the peak current of primary winding.
The principle of CC operation sets the product *Lp* and *fsw* to be a constant, thus the maximum output power and constant current in CC mode will not change as primary winding inductance changes. Up to +/-7% variation of the primary winding inductance can be compensated.

- **Frequency shuffling for EMI improvement**

The frequency shuffling (switching frequency modulation) is implemented in OB3396. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB3396. The switch current is detected by a sense resistor into the SOURCE pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on state so that the external RC filtering on sense input is no longer needed. The PWM duty cycle is determined by the current sense input voltage and the EA output voltage.

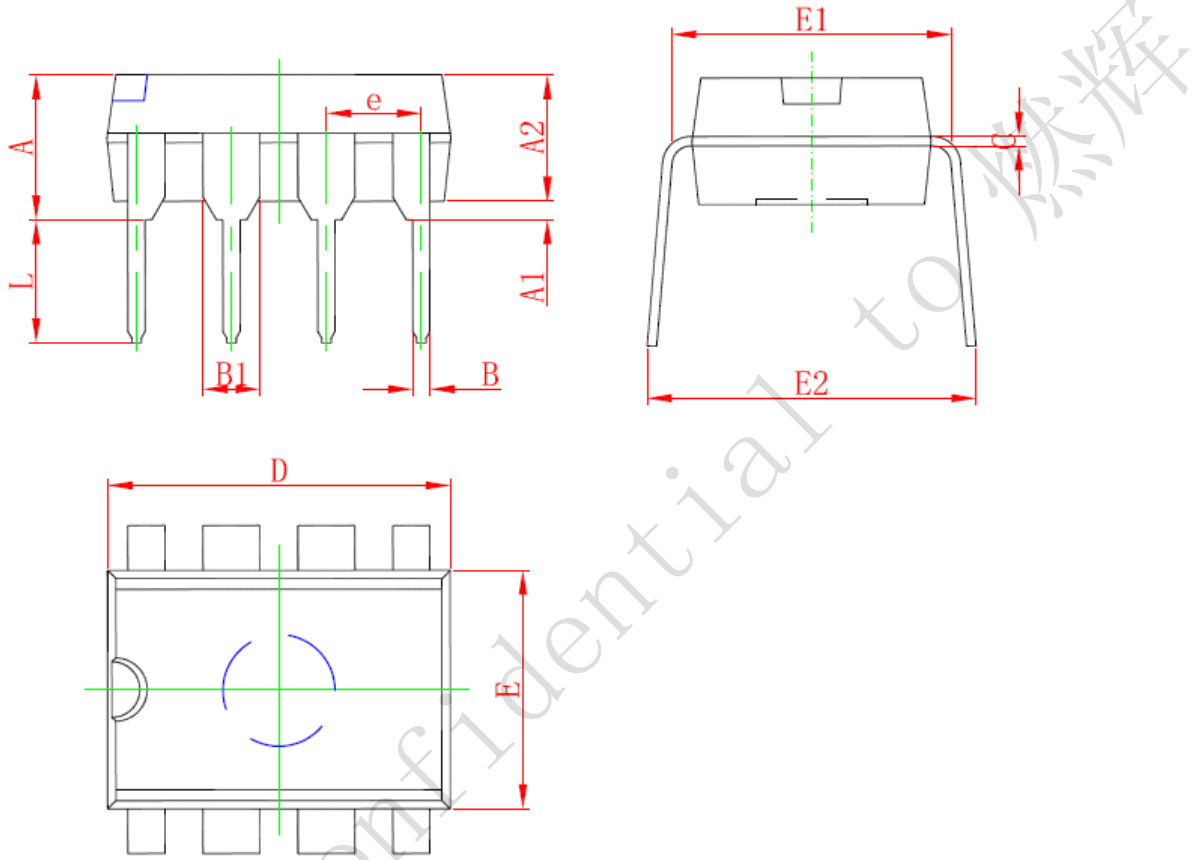
- **Gate Drive**

The internal power MOSFET in OB3396 is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive compromises EMI.
A good tradeoff is achieved through the built-in totem pole gate design with right output strength control.

- **Protection Control**

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), VDD clamp, Power on Soft Start, and Under Voltage Lockout on VDD (UVLO).
VDD is supplied by transformer auxiliary winding output. The output of OB3396 is shut down when VDD drops below UVLO (ON) limit and the power converter enters power on start-up sequence thereafter.

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

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