

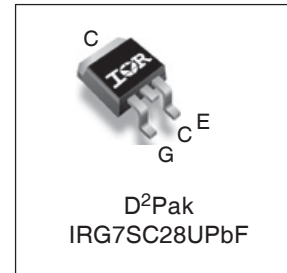
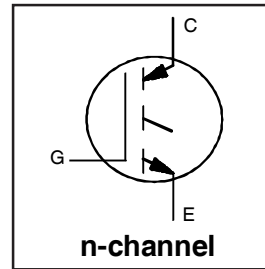
PDP TRENCH IGBT

IRG7SC28UPbF

Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}^{TM}) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
$V_{CE\ min}$	600	V
$V_{CE(on)}\ typ.\ @\ I_C = 40A$	1.70	V
$I_{RP\ max}\ @\ T_C = 25^\circ C\ ①$	225	A
$T_J\ max$	150	$^\circ C$



G	C	E
Gate	Collector	Emitter

Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}^{TM} rating per silicon area which improve panel efficiency. Additional features are 150 $^\circ C$ operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	± 30	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	60	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	30	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	225	
$P_D @ T_C = 25^\circ C$	Power Dissipation	171	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	68	
	Linear Derating Factor	1.37	W/ $^\circ C$
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	$^\circ C$
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	0.73	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ②	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{CES}	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_{CE} = 1.0mA$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ^③	15	—	—	V	$V_{GE} = 0V, I_{CE} = 1.0A$
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.57	—	V/°C	Reference to 25°C , $I_{CE} = 1.0mA$
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.25	—	V	$V_{GE} = 15V, I_{CE} = 12A$ ③
		—	1.42	—		$V_{GE} = 15V, I_{CE} = 24A$ ③
		—	1.70	1.95		$V_{GE} = 15V, I_{CE} = 40A$ ③
		—	1.96	—		$V_{GE} = 15V, I_{CE} = 70A$ ③
		—	2.97	—		$V_{GE} = 15V, I_{CE} = 160A$ ③
		—	1.75	—		$V_{GE} = 15V, I_{CE} = 40A, T_J = 150^\circ\text{C}$ ③
$V_{GE(th)}$	Gate Threshold Voltage	2.2	—	4.7	V	$V_{CE} = V_{GE}, I_{CE} = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
I_{CES}	Collector-to-Emitter Leakage Current	—	0.5	20	μA	$V_{CE} = 600V, V_{GE} = 0V$
		—	30	—		$V_{CE} = 600V, V_{GE} = 0V, T_J = 100^\circ\text{C}$
		—	90	—		$V_{CE} = 600V, V_{GE} = 0V, T_J = 125^\circ\text{C}$
		—	305	—		$V_{CE} = 600V, V_{GE} = 0V, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	$V_{GE} = 30V$
	Gate-to-Emitter Reverse Leakage	—	—	-100	nA	$V_{GE} = -30V$
g_{fe}	Forward Transconductance	—	55	—	S	$V_{CE} = 25V, I_{CE} = 40A$
Q_g	Total Gate Charge	—	70	—	nC	$V_{CE} = 400V, I_C = 40A, V_{GE} = 15V$ ③
Q_{gc}	Gate-to-Collector Charge	—	25	—	nC	
$t_{d(on)}$	Turn-On delay time	—	30	—	ns	$I_C = 40A, V_{CC} = 400V$ $R_G = 22\Omega, L = 100\mu H$ $T_J = 25^\circ\text{C}$
t_r	Rise time	—	35	—		
$t_{d(off)}$	Turn-Off delay time	—	260	—		
t_f	Fall time	—	145	—		
$t_{d(on)}$	Turn-On delay time	—	25	—	ns	$I_C = 40A, V_{CC} = 400V$ $R_G = 22\Omega, L = 100\mu H$ $T_J = 150^\circ\text{C}$
t_r	Rise time	—	40	—		
$t_{d(off)}$	Turn-Off delay time	—	280	—		
t_f	Fall time	—	320	—		
t_{st}	Shoot Through Blocking Time	100	—	—	ns	$V_{CC} = 240V, V_{GE} = 15V, R_G = 5.1\Omega$
E_{PULSE}	Energy per Pulse	—	770	—	μJ	$L = 220nH, C = 0.40\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$
		—	930	—		$L = 220nH, C = 0.40\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$
ESD	Human Body Model	Class H1C (2000V) (Per JEDEC standard JESD22-A114)				
	Machine Model	Class M4 (425V) (Per EIA/JEDEC standard EIA/JESD22-A115)				
C_{ies}	Input Capacitance	—	1880	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	75	—		$V_{CE} = 30V$
C_{res}	Reverse Transfer Capacitance	—	45	—		$f = 1.0MHz$
L_C	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_E	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

Notes:

- ① Half sine wave with duty cycle ≤ 0.02 , $t_{on} = 1.0\mu\text{sec}$.
- ② R_{θ} is measured at T_J of approximately 90°C .
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.

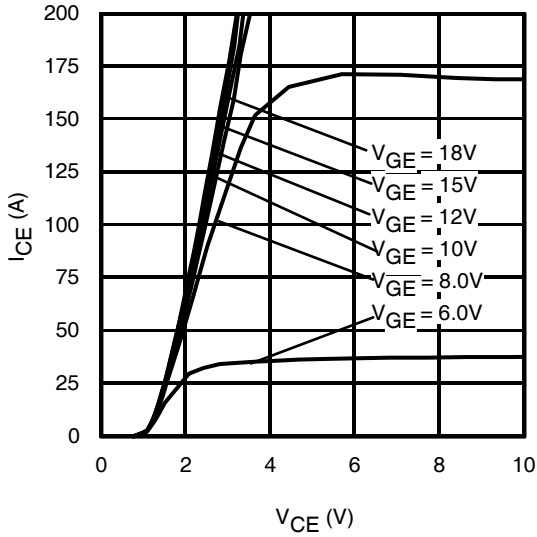


Fig 1. Typical Output Characteristics @ 25°C

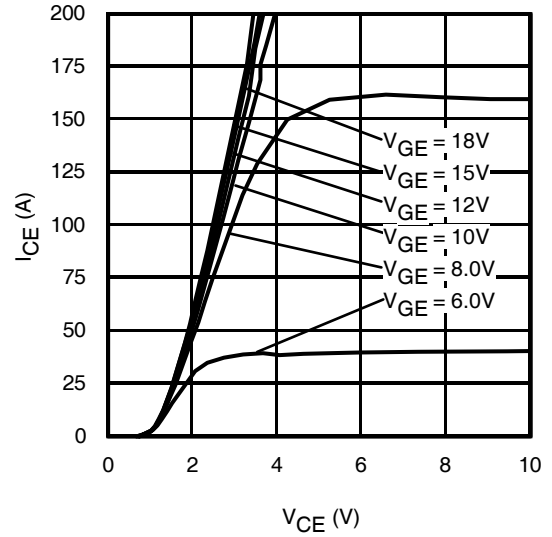


Fig 2. Typical Output Characteristics @ 75°C

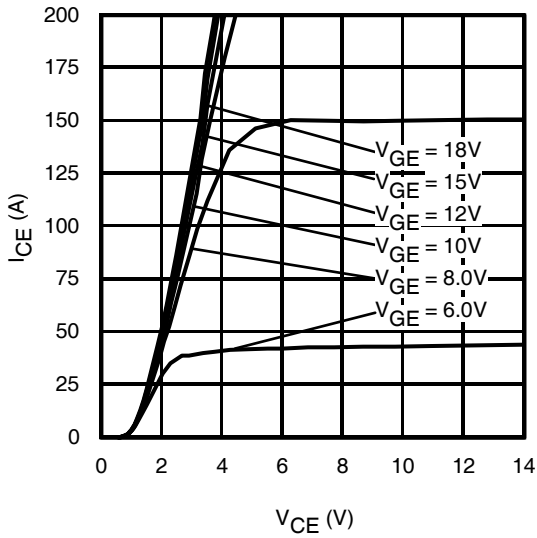


Fig 3. Typical Output Characteristics @ 125°C

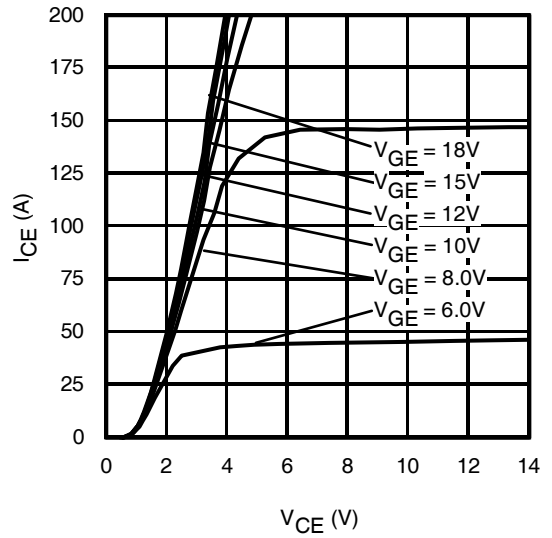


Fig 4. Typical Output Characteristics @ 150°C

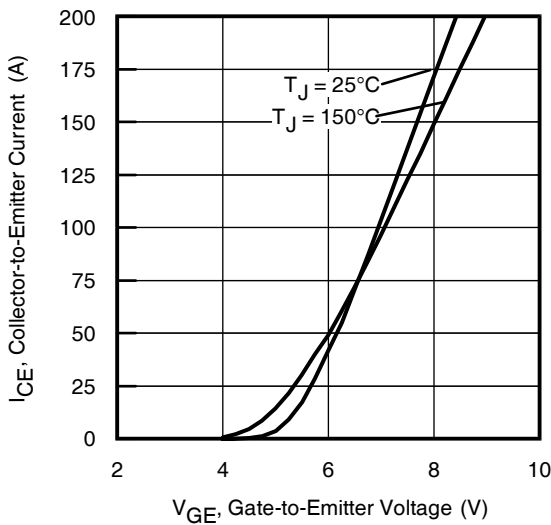


Fig 5. Typical Transfer Characteristics

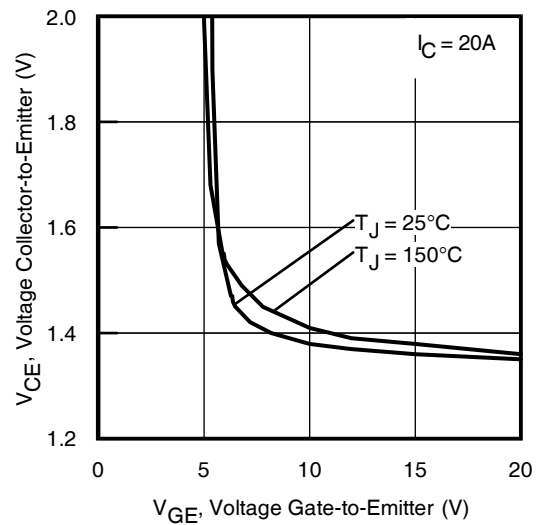


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

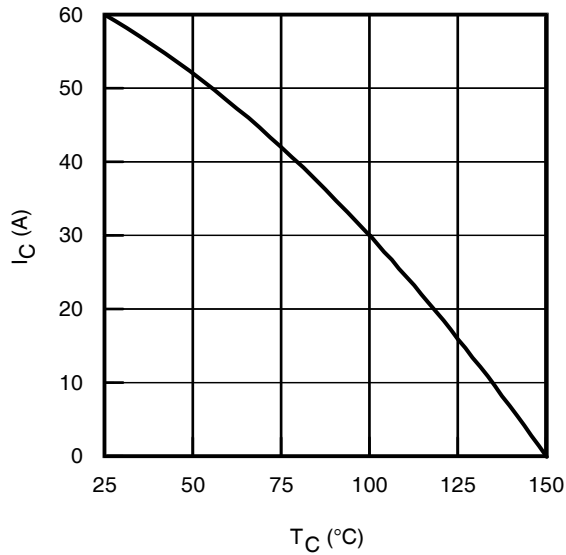


Fig 7. Maximum Collector Current vs. Case Temperature

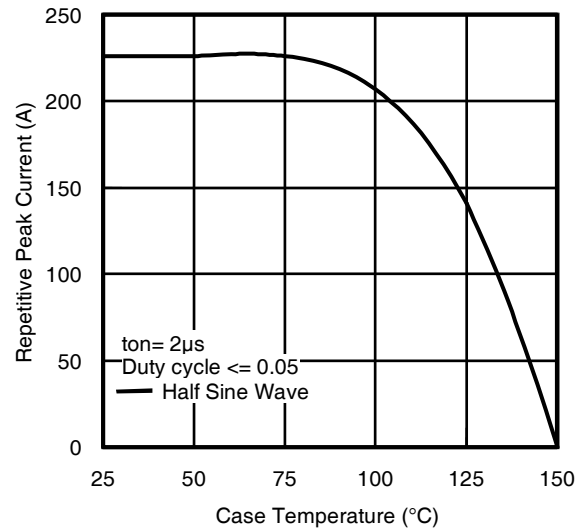


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

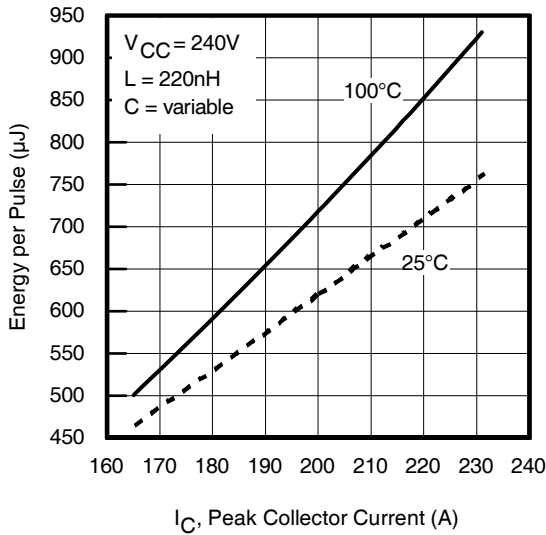


Fig 9. Typical E_{PULSE} vs. Collector Current

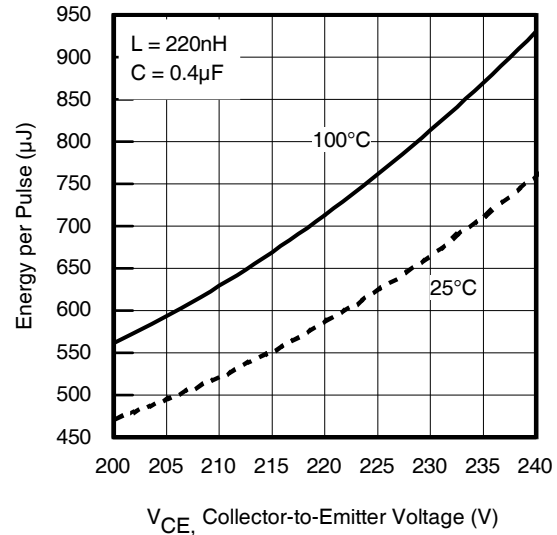


Fig 10. Typical E_{PULSE} vs. Collector-to-Emitter Voltage

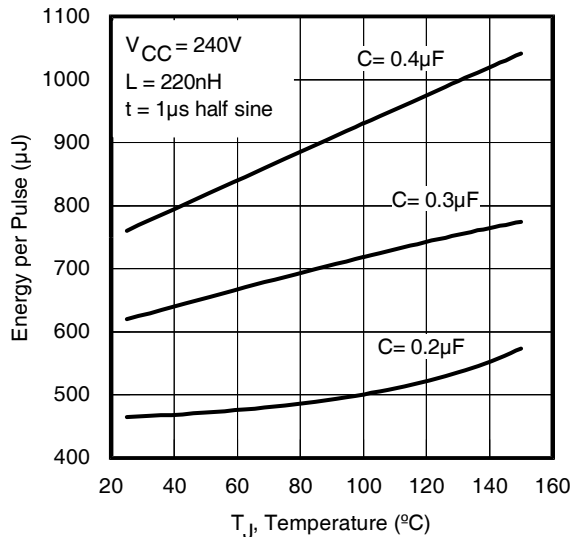


Fig 11. E_{PULSE} vs. Temperature

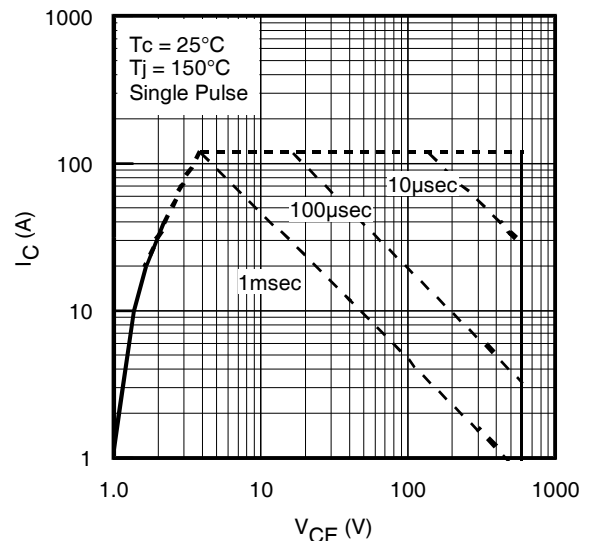


Fig 12. Forward Bias Safe Operating Area

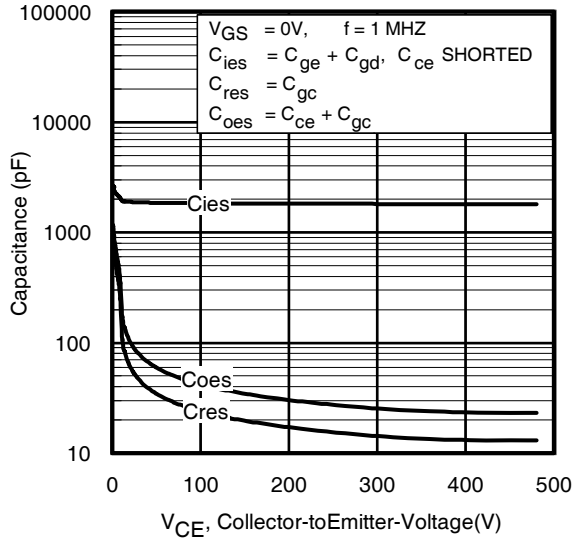


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

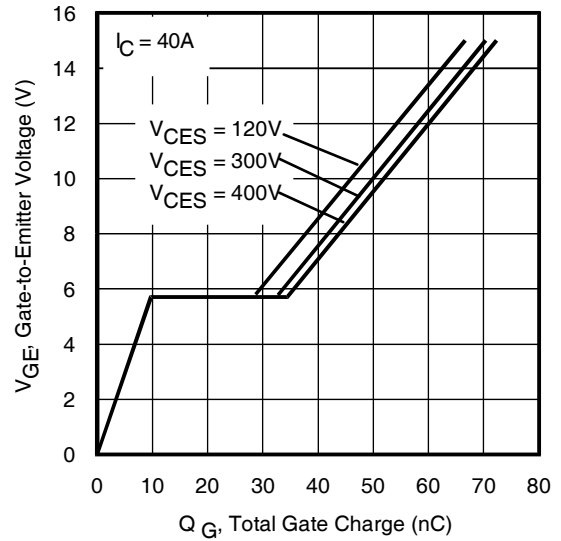


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

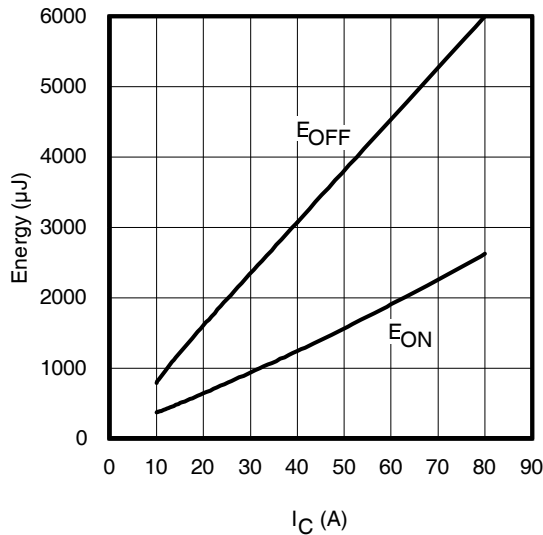


Fig 15 - Typ. Energy Loss vs. I_C

$T_J = 150^\circ C; L = 250\mu H; V_{CE} = 400V, R_G = 22\Omega; V_{GE} = 15V$

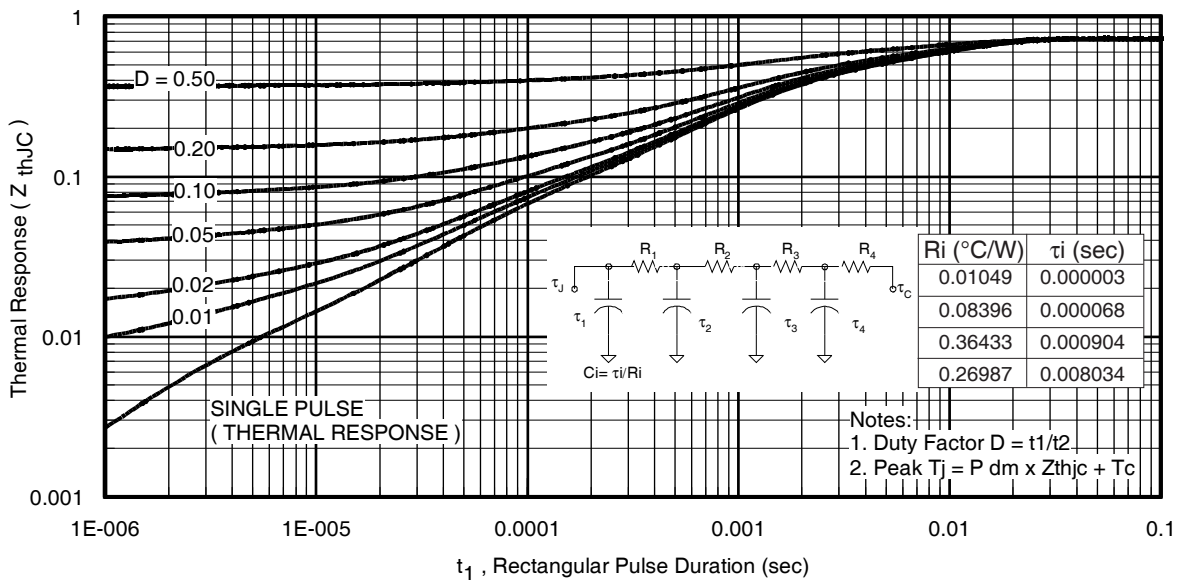


Fig 16. Maximum Effective Transient Thermal Impedance, Junction-to-Case

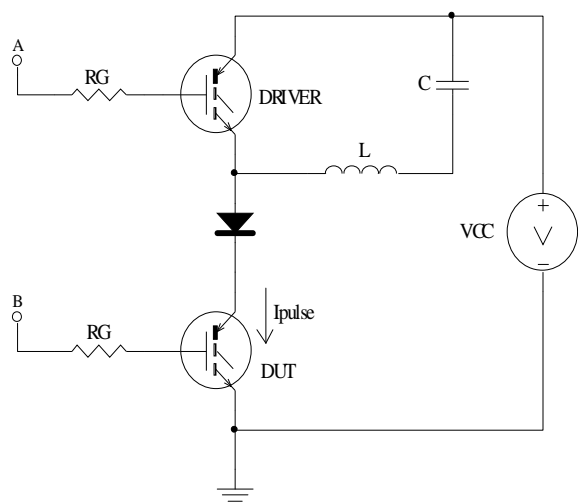


Fig 16a. t_{st} and E_{PULSE} Test Circuit

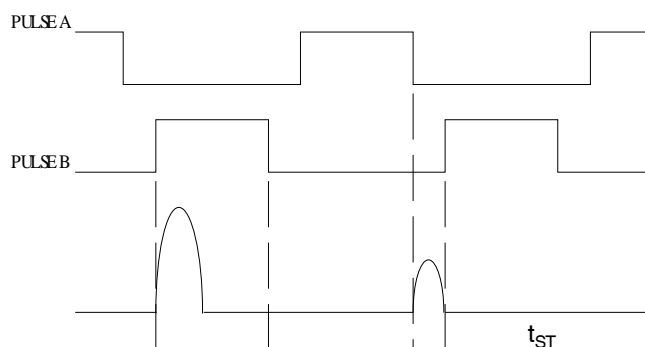


Fig 16b. t_{st} Test Waveforms

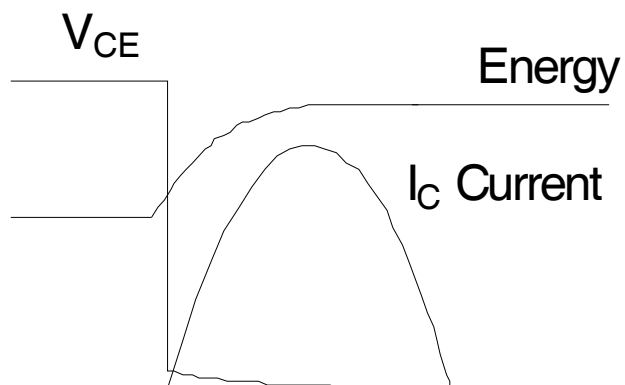


Fig 16c. E_{PULSE} Test Waveforms

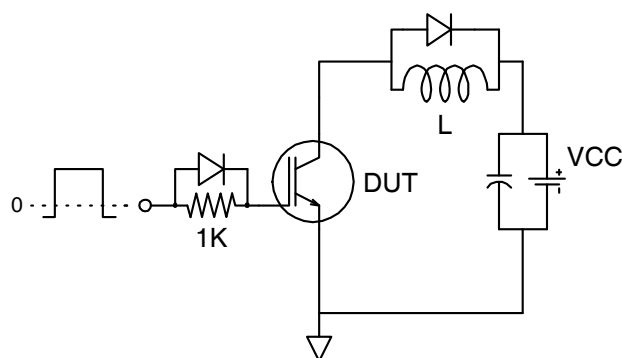
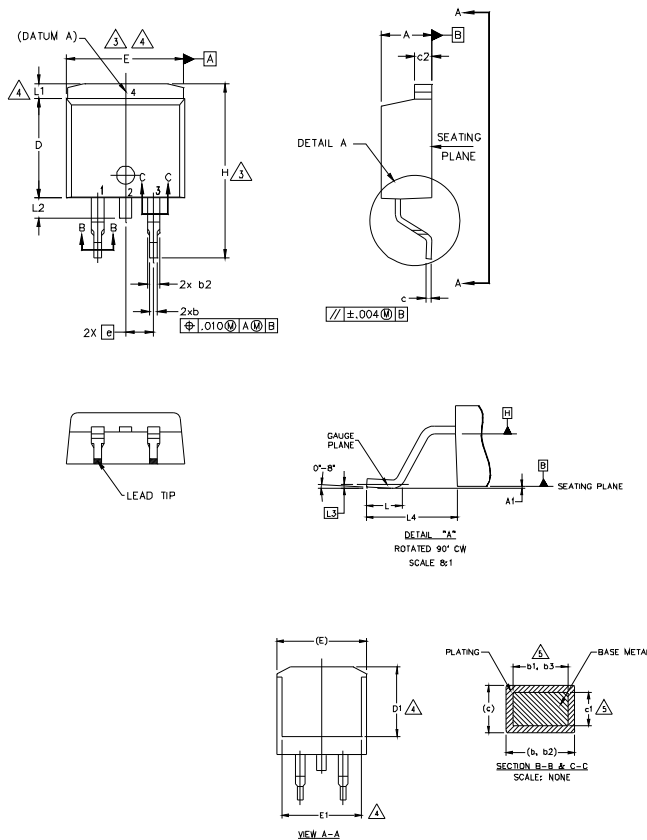


Fig 17 - Gate Charge Circuit (turn-off)

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	
L2	1.27	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

DIODES

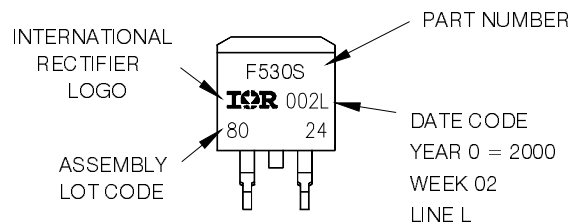
- 1.- ANODE *
- 2, 4.- CATHODE
- 3.- ANODE

* PART DEPENDENT.

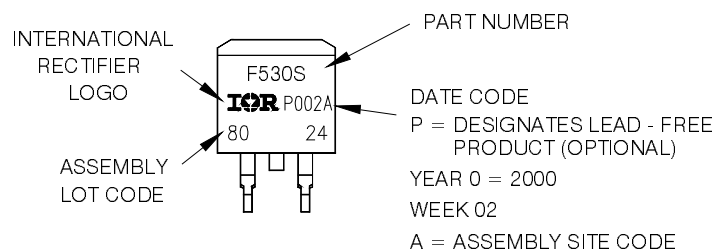
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead - Free"



OR

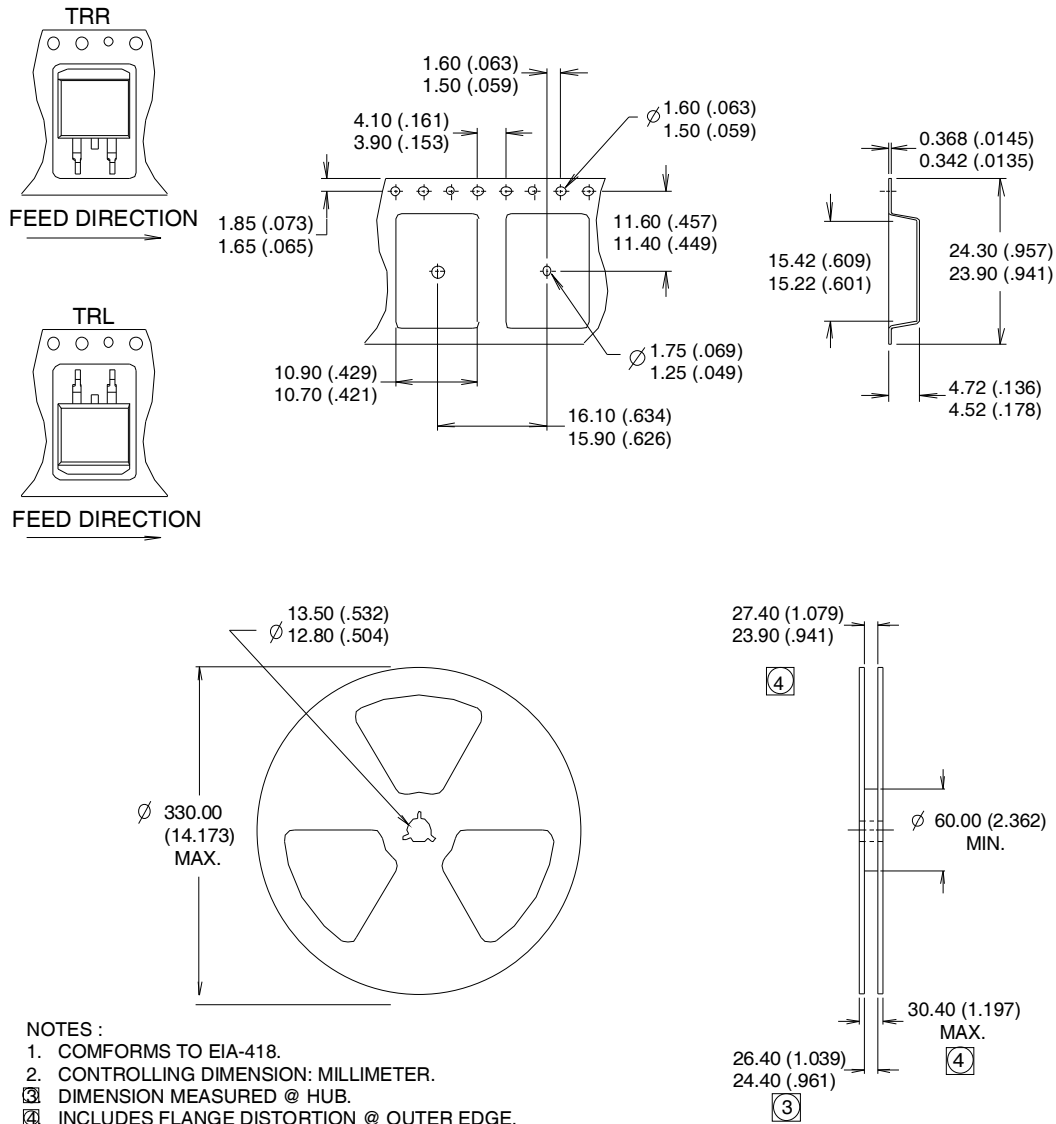


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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