

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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# **Phase-out/Discontinued**

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Phase-out/Discontinued

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

DESCRIPTION

The 2SK1758 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance  
 $R_{DS(on)} = 4.2 \Omega$  ( $V_{GS} = 10 V, I_D = 1 A$ )
- Low  $C_{iss}$   $C_{iss} = 360 pF$  TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

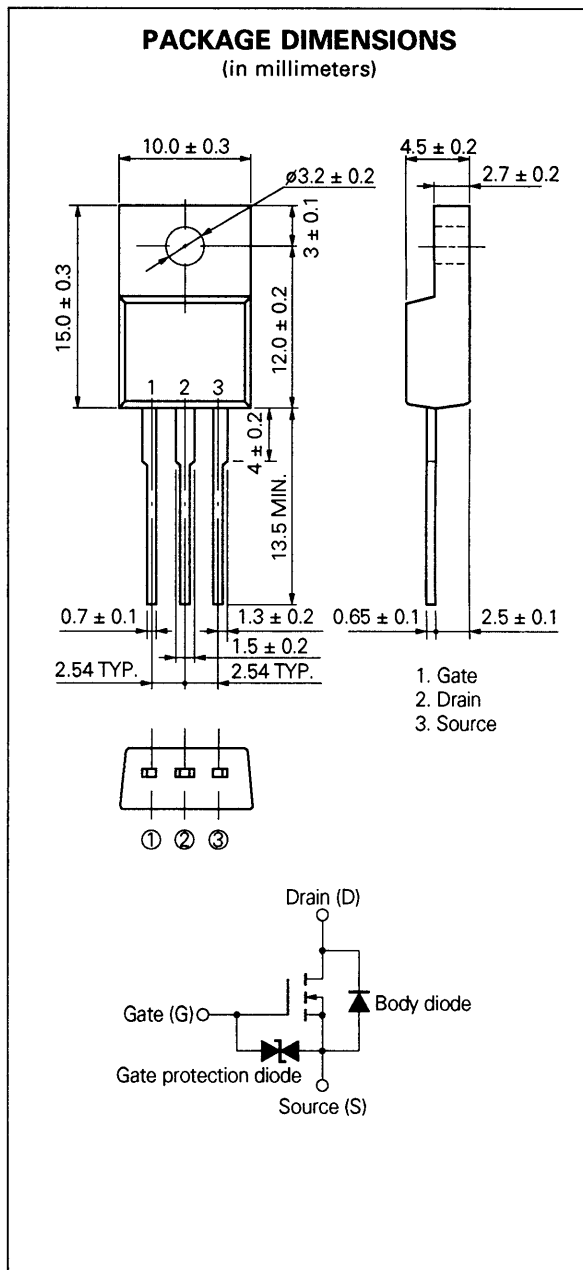
ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

Drain to Source Voltage	$V_{DSS}$	600	V
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 2.0$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 8.0$	A
Total Power Dissipation ( $T_c = 25^\circ C$ )	$PT_1$	30	W
Total Power Dissipation ( $T_a = 25^\circ C$ )	$PT_2$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ C$
Single Avalanche Current	$I_{AS}^{**}$	3.0	A
Single Avalanche Energy	$E_{AS}^{**}$	96	mJ

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$

\*\* Starting  $T_{ch} = 25^\circ C, R_G = 25 \Omega, V_{GS} = 20 V \rightarrow 0$

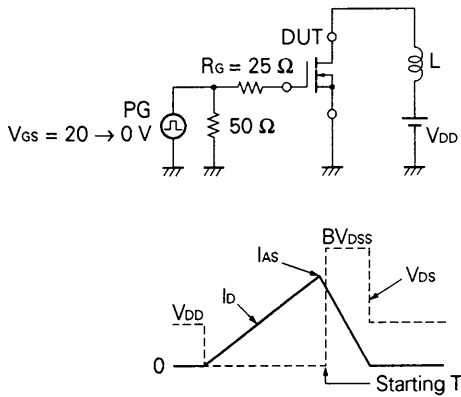
PACKAGE DIMENSIONS  
(in millimeters)



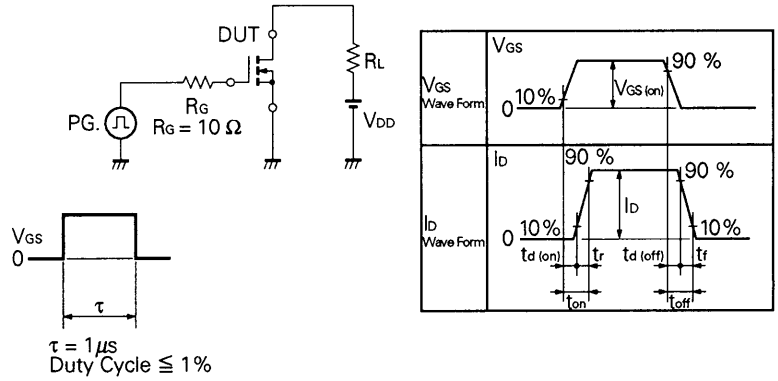
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		2.8	4.2	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.0		4.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	0.5	1.3		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		360		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		130		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		50		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		5		ns	V <sub>GS(on)</sub> = 10 V
Rise Time	t <sub>r</sub>		6		ns	V <sub>DD</sub> = 150 V
Turn-Off Delay Time	t <sub>d(off)</sub>		60		ns	I <sub>D</sub> = 1 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		20		ns	R <sub>L</sub> = 150 Ω
Total Gate Charge	Q <sub>G</sub>		17		nC	V <sub>GS</sub> = 10 V
Gate to Source Charge	Q <sub>GS</sub>		3		nC	I <sub>F</sub> = 2 A
Gate to Drain Charge	Q <sub>GD</sub>		10		nC	V <sub>DD</sub> = 400 V
Diode Forward Voltage	V <sub>F(S-D)</sub>		0.85		V	I <sub>F</sub> = 2 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		270		ns	I <sub>F</sub> = 2 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		1.4		μC	di/dt = 50 A/μs

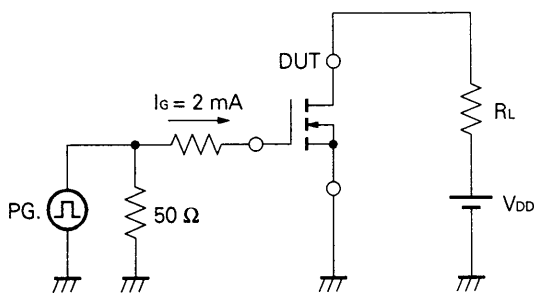
**Test Circuit 1: Avalanche Capability**



**Test Circuit 2: Switching Time**

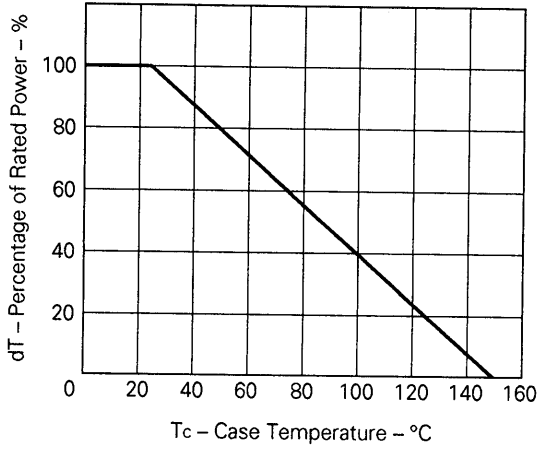


**Test Circuit 3: Gate Charge**

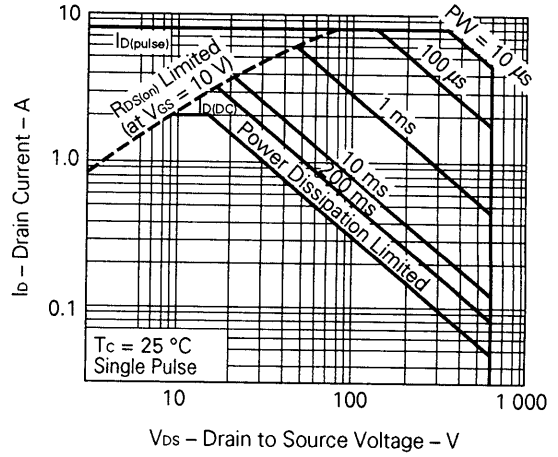


TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

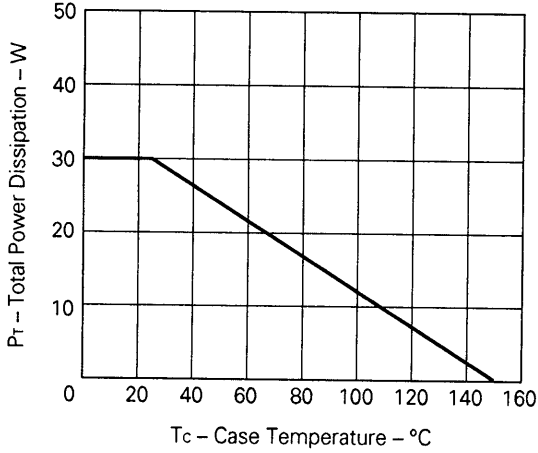
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



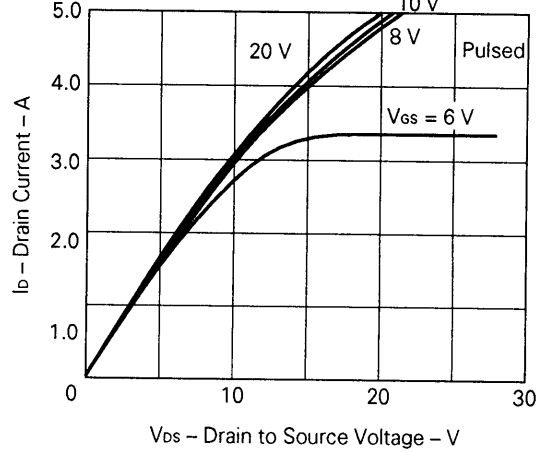
FORWARD BIAS SAFE OPERATING AREA



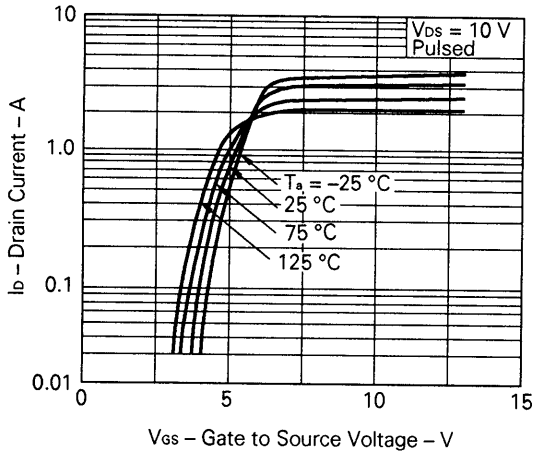
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



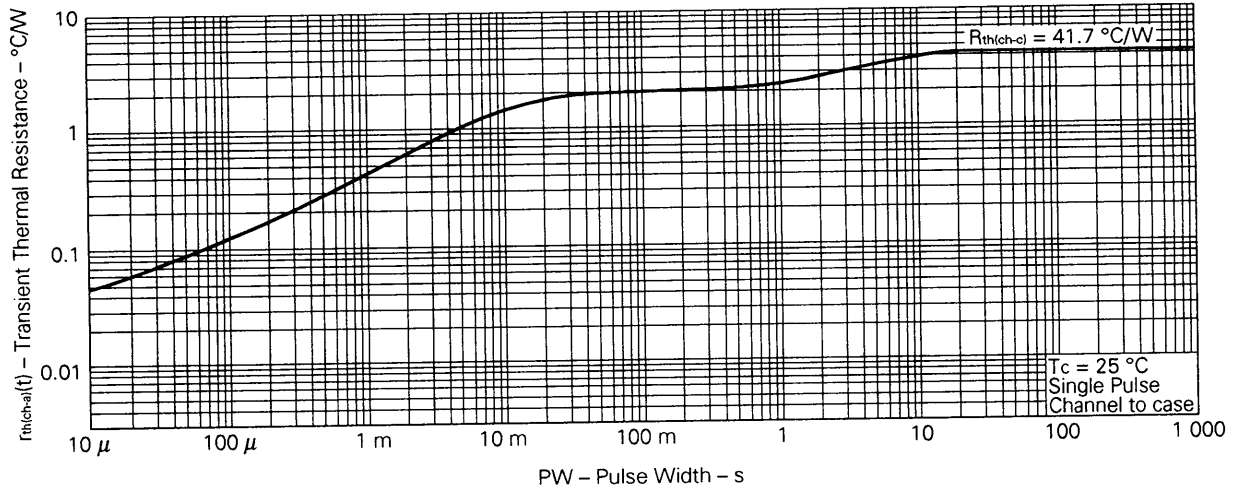
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



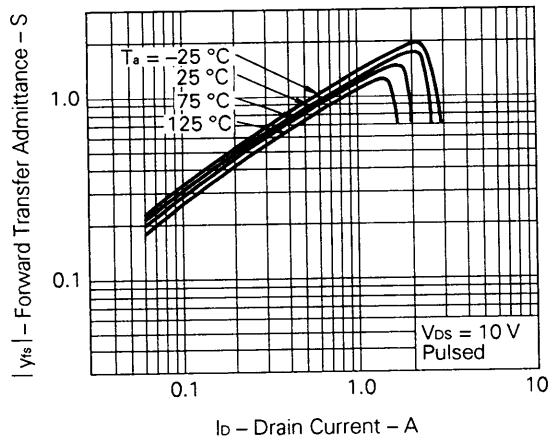
TRANSFER CHARACTERISTICS



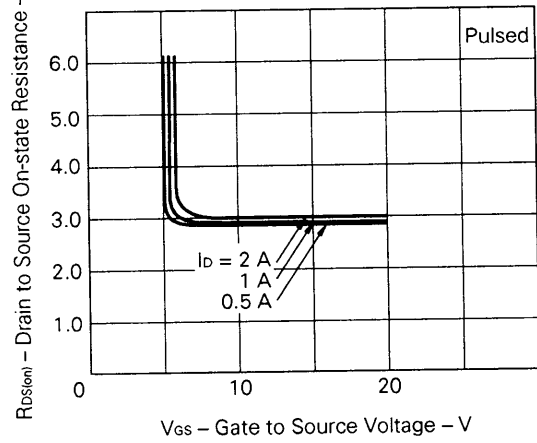
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



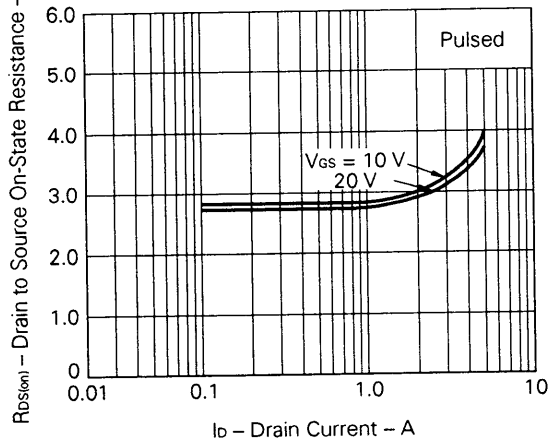
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



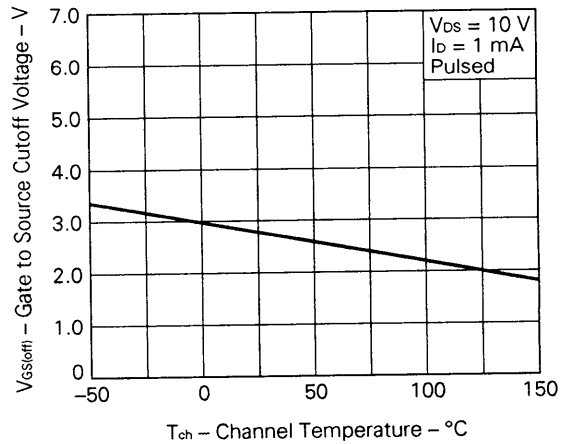
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

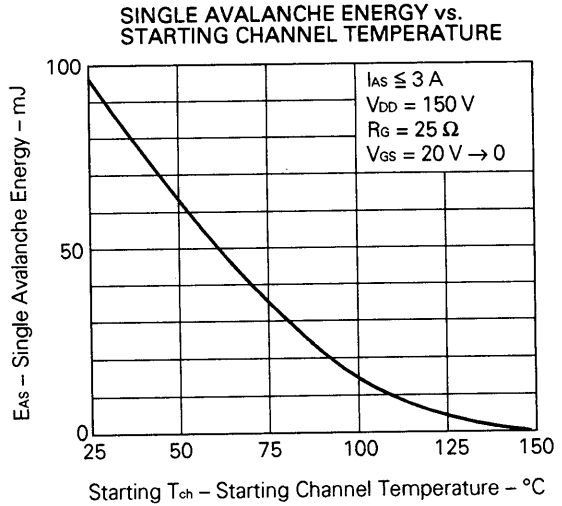
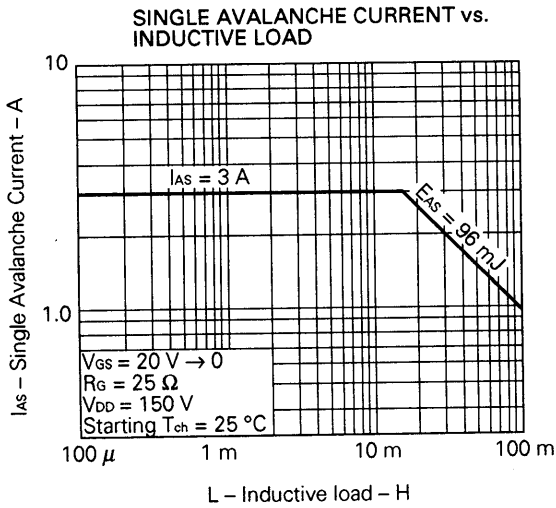
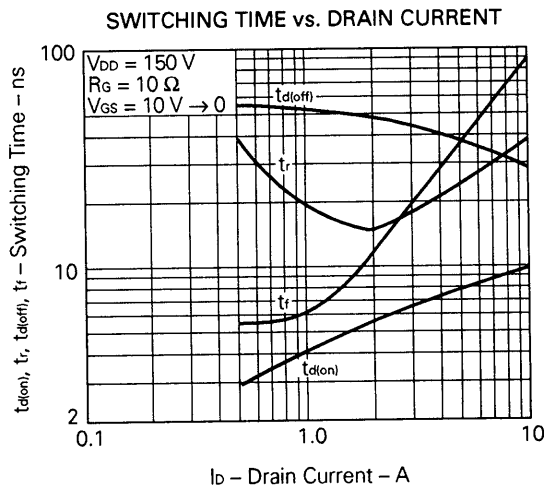
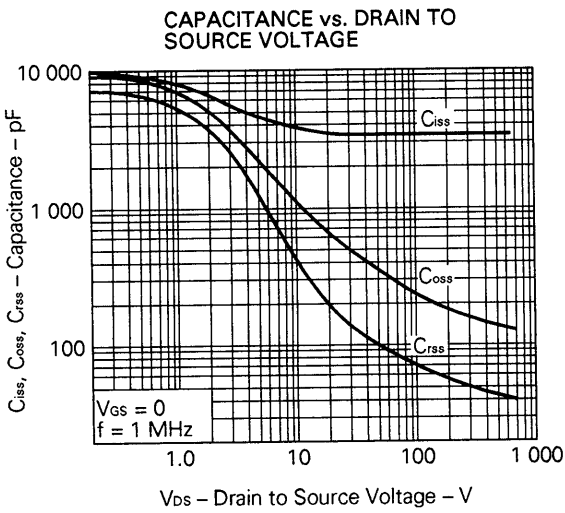
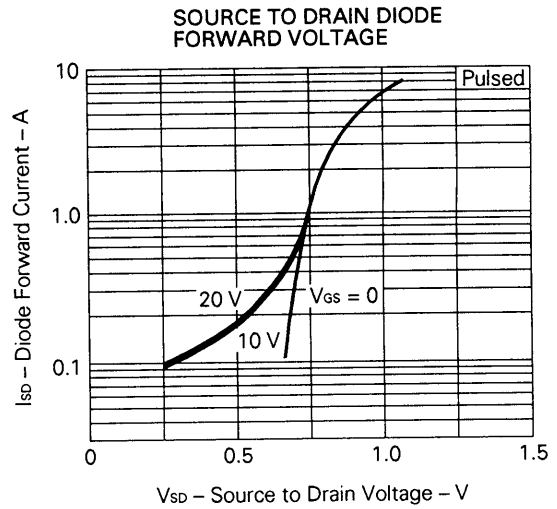
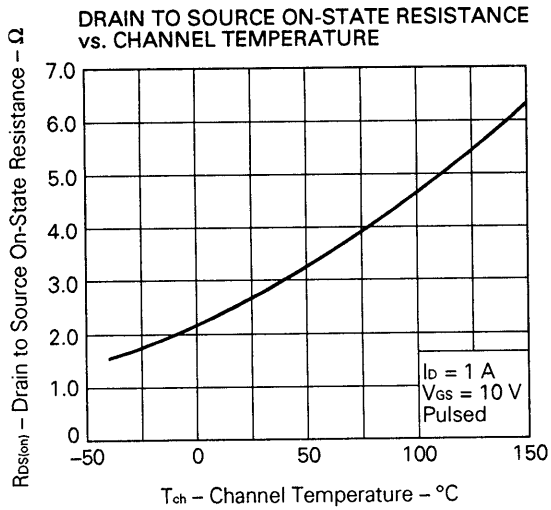


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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