



2SK1284-AZ

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April 1st, 2010
Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR
2SK1284, 1284-Z

SWITCHING
 N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK1284 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

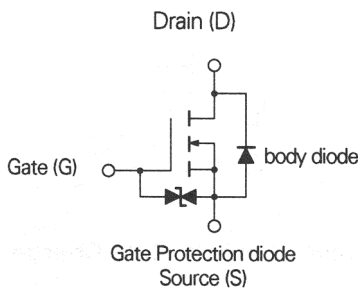
- Low On-state Resistance
 $R_{DS(on)} \leq 0.32 \Omega$ ($V_{GS} = 10 V, I_D = 2 A$)
 $R_{DS(on)} \leq 0.40 \Omega$ ($V_{GS} = 4.0 V, I_D = 2 A$)
- Low C_{iss} : $C_{iss} = 500 pF$ TYP.
- Built-in G-S Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

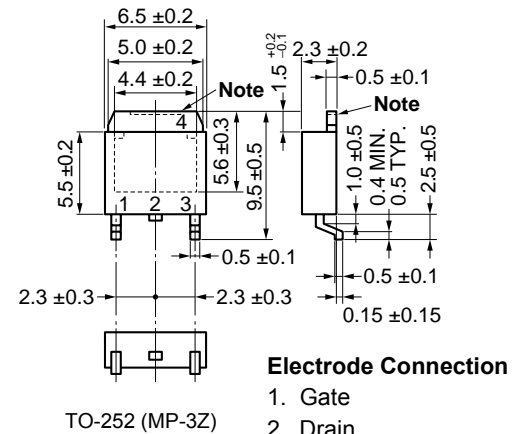
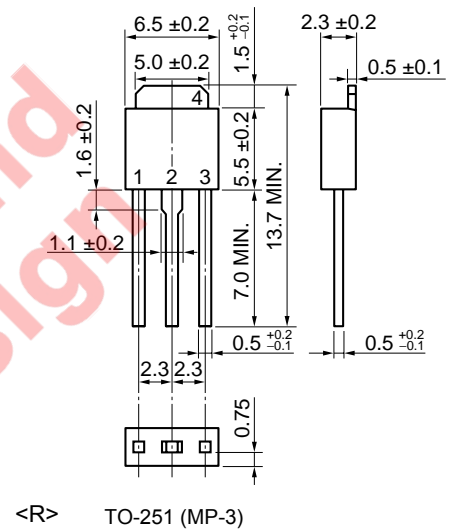
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage (AC)	$V_{GSS(AC)}$	± 20	V
Gate to Source Voltage (DC)	$V_{GSS(DC)}$	-10, +20	V
Drain Current (DC)	$I_{D(DC)}$	± 3.0	A
Drain Current (pulse) ^{Note}	$I_{D(pulse)}$	± 12	A
Total Power Dissipation (TC = 25°C)	P_{T1}	20	W
Total Power Dissipation (TA = 25°C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Note $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

EQUIVALENT CIRCUIT



PACKAGE DRAWINGS (Unit: mm)



Electrode Connection

1. Gate
2. Drain
3. Source
4. Drain Fin

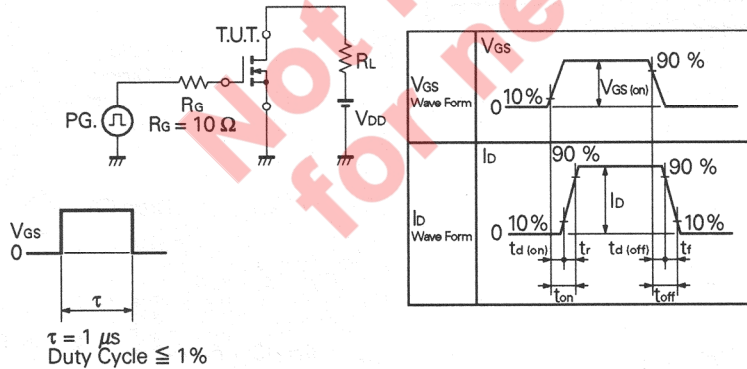
Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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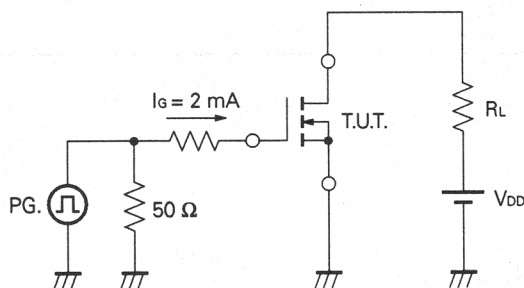
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.26	0.32	Ω	V _{GS} = 10 V, I _D = 2 A
Drain to Source On-state Resistance	R _{DS(on)}		0.32	0.40	Ω	V _{GS} = 4.0 V, I _D = 2 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	2.4			S	V _{DS} = 10 V, I _D = 2 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		500		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		160		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		20		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		40		ns	V _{GS(on)} = 10 V
Rise Time	t _r		55		ns	V _{DD} = 50 V
Turn-Off Delay Time	t _{d(off)}		500		ns	I _D = 2 A, R _G = 10 Ω
Fall Time	t _f		120		ns	R _L = 25 Ω
Total Gate Charge	Q _G		13		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		3		nC	I _D = 3 A
Gate to Drain Charge	Q _{GD}		2		nC	V _{DD} = 80 V
Diode Forward Voltage	V _{SD}		0.9		V	I _{SD} = 3 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		140		ns	I _F = 3 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		250		nC	di/dt = 50 A/μs

Test Circuit 1: Switching Time

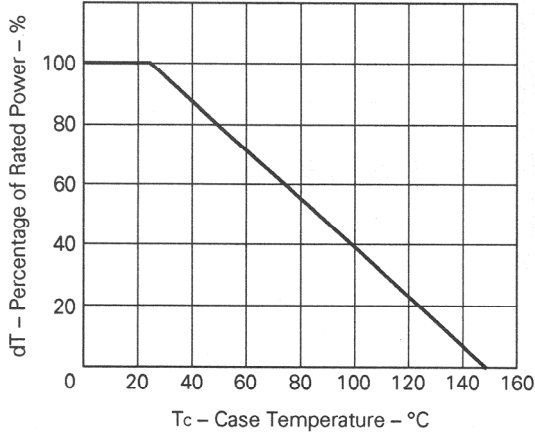


Test Circuit 2: Gate Charge

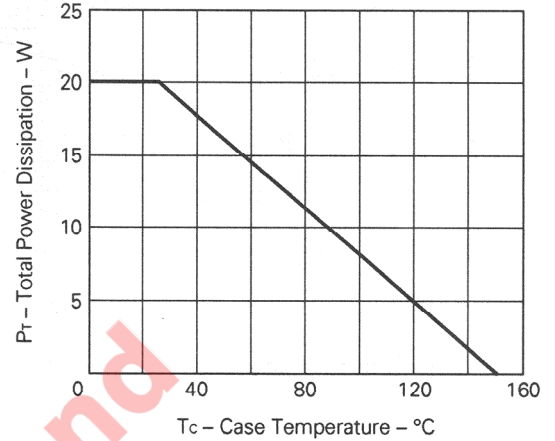


TYPICAL CHARACTERISTICS (T_a = 25 °C)

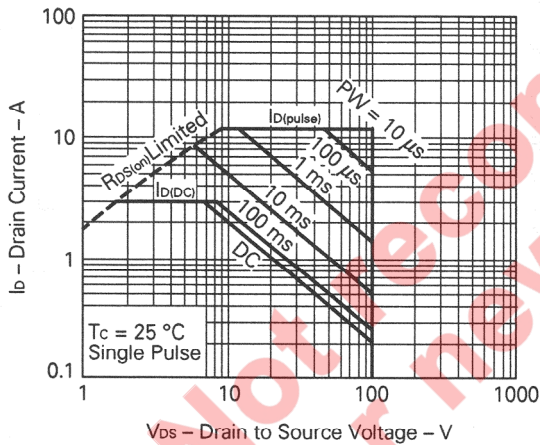
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



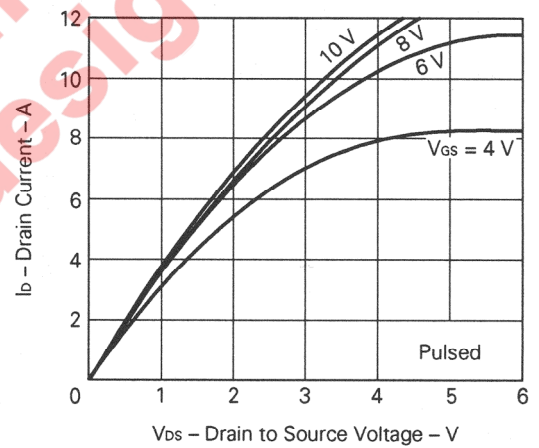
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



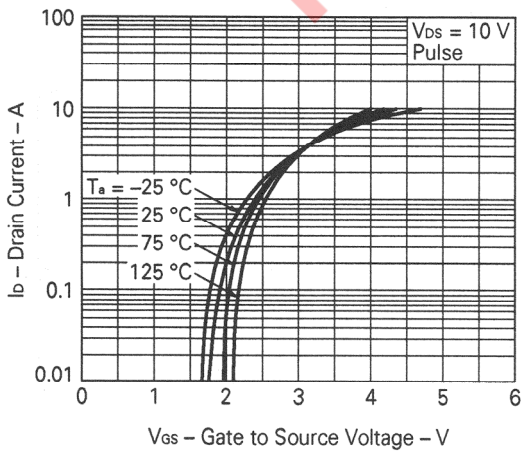
FORWARD BIAS SAFE OPERATING AREA

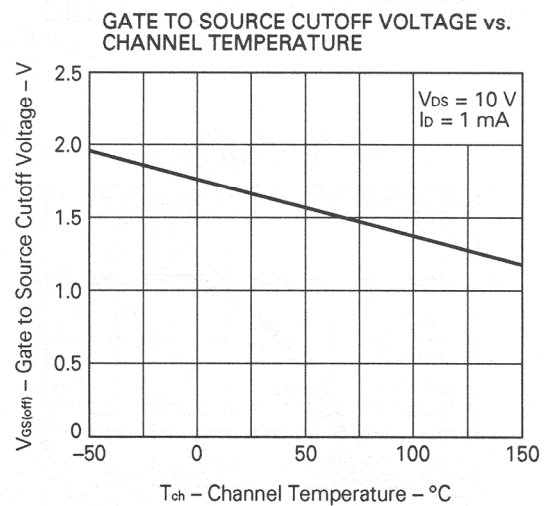
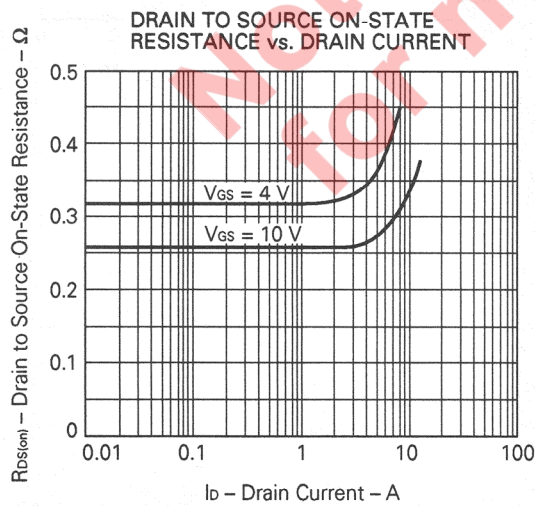
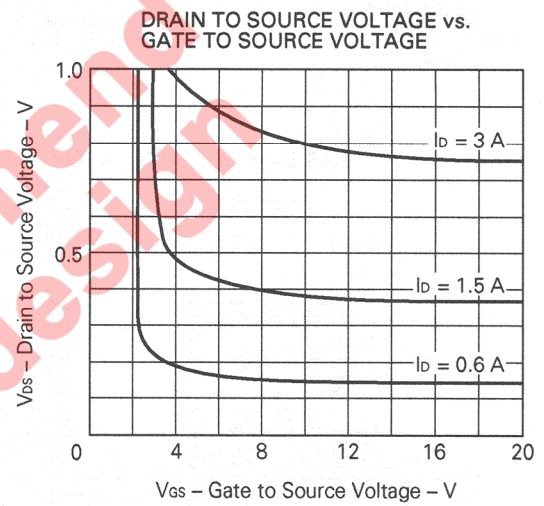
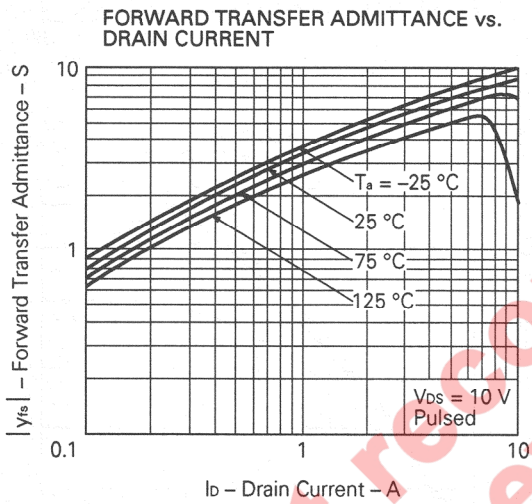
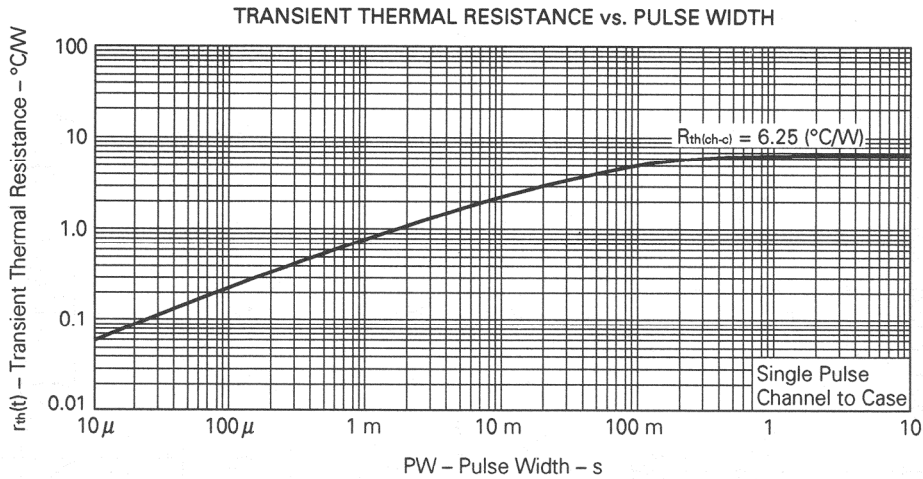


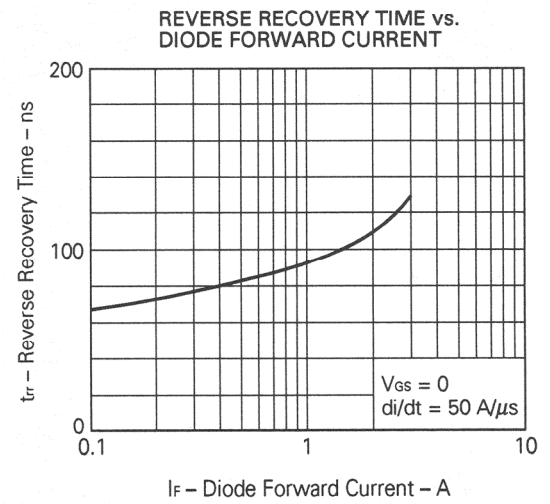
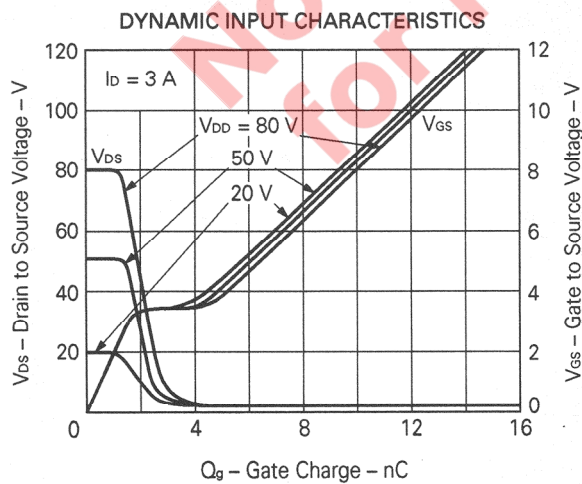
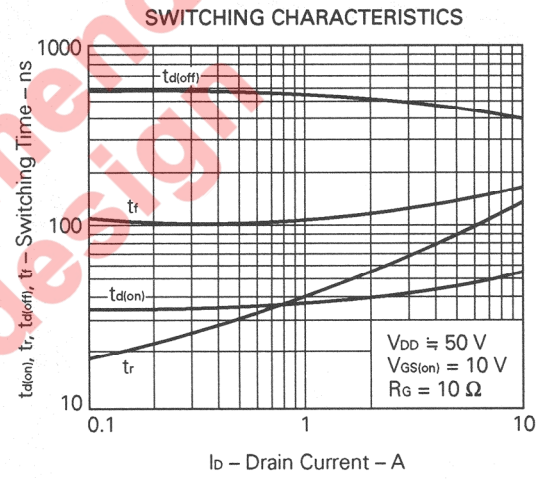
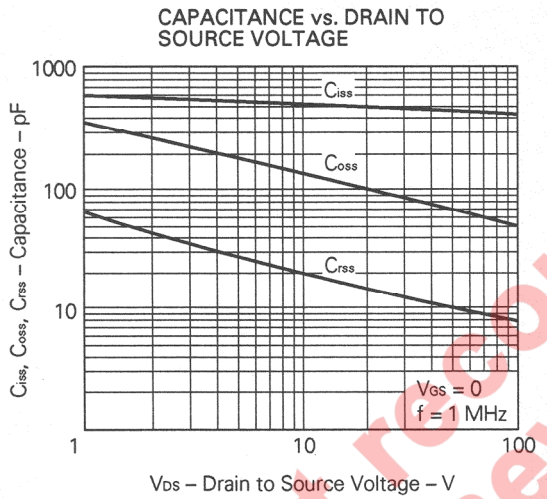
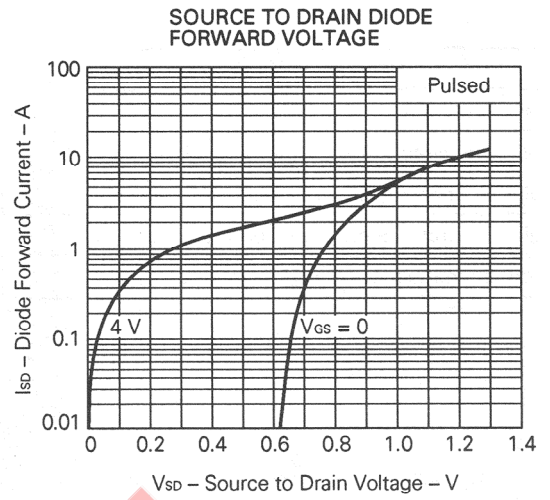
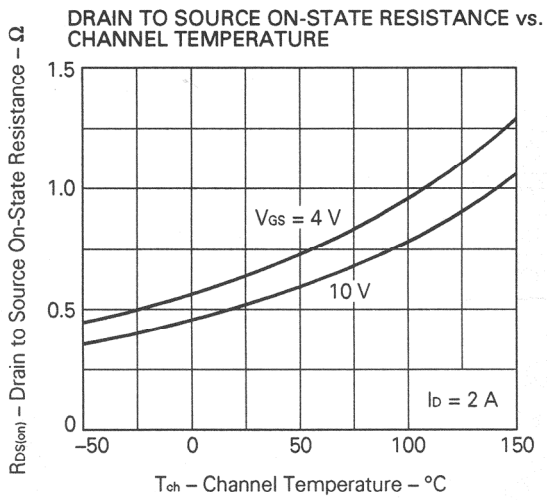
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



TRANSFER CHARACTERISTICS







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