Unit: mm

TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (Ultra-High-Speed U-MOSIII)

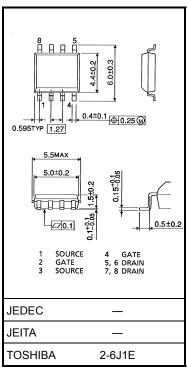
TPC8214-H

High-Efficiency DC / DC Converter Applications CCFL Inverters

- · Small footprint due to a small and thin package
- · High-speed switching
- Small gate charge: Q_{SW} = 2.0 nC (typ.)
- Low drain-source ON-resistance: $R_{DS (ON)} = 130 \text{ m}\Omega \text{ (typ.)}$
- High forward transfer admittance: |Y_{fS}| =5.4 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 100 V)
- Enhancement mode: V_{th} = 1.1 to 2.3 V (V_{DS} = 10 V, I_D = 1 mA)

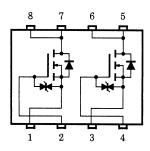
Absolute Maximum Ratings (Ta = 25°C)

Cha	racteristic	Symbol	Rating	Unit	
Drain-source vo	Itage	V_{DSS}	100	V	
Drain-gate volta	ge (R _{GS} = 20 kΩ)	V_{DGR}	100	V	
Gate-source vol	tage	V _{GSS}	±20	V	
Drain current	D C (Note 1)	I _D	2.2	Α	
Diam current	Pulse (Note 1)	I_{DP}	8.8	A	
Drain power	Single-device operation (Note 3a)	P _{D (1)}	1.5	W	
dissipation (t = 10 s) (Note 2a)	Single-device value at dual operation (Note 3b)	P _D (2)	1.1		
Drain power dissipation (t = 10 s) (Note 2b)	Single-device operation (Note 3a)	P _{D (1)}	0.75	W	
	Single-device value at dual operation (Note 3b)	P _{D 2)}	0.45		
Single-pulse ava	lanche energy (Note 4)	EAS	3.9	mJ	
Avalanche curre	nt	I _{AR}	2.2	Α	
Repetitive avalar (Note	nche energy e 2a, Note 3b, Note 5)	EAR	0.026	mJ	
Channel tempera	ature	T _{ch}	150	°C	
Storage tempera	ture range	T _{stg}	-55∼150	°C	



Weight: 0.085 g (typ.)

Circuit Configuration



Note: For Notes 1 to 5, refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

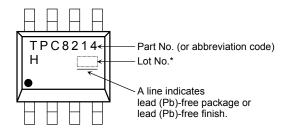
This transistor is an electrostatic-sensitive device. Handle with care.

2007-02-21

Thermal Characteristics

Characteristic	Symbol	Max	Unit		
Thermal resistance, channel to ambient	Single-device operation (Note 3a)	R _{th (ch-a) (1)}	83.3	_	
(t = 10 s) (Note 2a)	Single-device value at dual operation (Note 3b)	R _{th (ch-a) (2)}	114	°C/W	
Thermal resistance, channel to ambient	Single-device operation (Note 3a)	R _{th (ch-a) (1)}	167	C/VV	
(t = 10 s) (Note 2b)	Single-device value at dual operation (Note 3b)	R _{th} (ch-a) (2)	278		

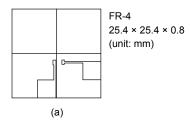
Marking

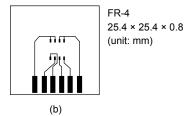


Note 1: The channel temperature should not exceed 150°C during use.

Note 2:

- a) Device mounted on a glass-epoxy board (a)
- b) Device mounted on a glass-epoxy board (b)





Note 3:

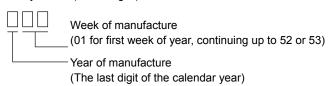
- a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.)
- b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.)

Note 4: V_{DD} = 50 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω , I_{AR} = 2.2 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: • on the lower left of the marking indicates Pin 1.

* Weekly code: (Three digits)



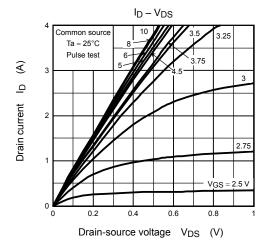


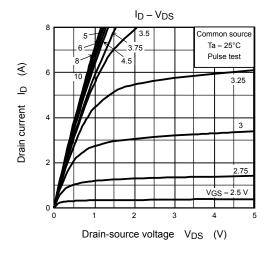
Electrical Characteristics (Ta = 25°C)

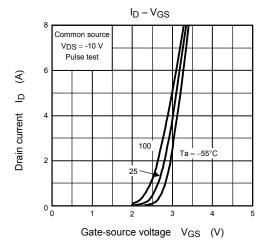
Chara	cteristic	Symbol	ol Test Condition Min Typ. Max		Unit		
Gate leakage cu	ırrent	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V	_	_	±10	μA
Drain cutoff curr	ent	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	_	_	10	μΑ
Drain-source br	source breakdown voltage V (BR) DSS I _D = 10 mA, V _{GS} = 0 V 100 —		_	_	V		
Dialii Source bi	eakdown voltage	V _{(BR)DSX}	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	60 — —			
Gate threshold	voltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	1.1	_	2.3	V
Drain-source O	N-resistance	R _{DS} (ON)	V _{GS} = 4.5 V, I _D = 1.1 A	_	140	190	mΩ
Diam Source O	14-resistance	R _{DS} (ON)	V _{GS} = 10 V , I _D = 1.1 A	_	130	180	11122
Forward transfe	r admittance	Y _{fs}	V _{DS} = 10 V , I _D = 1.1 A	A 2.7 5.4 —		I	S
Input capacitano	ce	C _{iss}		_	360	1	pF
Reverse transfe	r capacitance	C _{rss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	_	22	-	
Output capacitance		C _{oss}		_	75	_	
Switching time	Rise time	t _r	$V_{GS} \stackrel{10}{\overset{\circ}{0}} \stackrel{V}{\overset{\circ}{V}} \stackrel{I_{D}}{\overset{\circ}{\longrightarrow}} \stackrel{1.1}{\overset{\circ}{\nearrow}} \stackrel{A}{\overset{\circ}{\nearrow}} \stackrel{V}{\overset{\circ}{\nearrow}} \stackrel{V}{\overset{V}} \stackrel{V} \overset{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V} \overset{V}{\overset{V}} \stackrel{V}{\overset{V}} \stackrel{V} \overset{V} \overset{V} \overset{V} \overset{V}{\overset{V}} \stackrel{V} \overset{V} \overset{V} \overset{V} $	_	7	_	
	Turn-on time	ton		_	14	ı	ne
	Fall time	t _f		_	3	ı	ns
	Turn-off time	t _{off}		_	17	_	
Total gate charge (gate-source plus gate-drain) (Note 7)		0	$V_{DD} \simeq 80~V,~V_{GS} = 10~V,~I_D = 2.2~A$	_	7.5		
		Q_g	$V_{DD} \simeq 80 \ V, V_{GS} = 5 \ V, I_D = 2.2 \ A$	_	4.5		
Gate-source charge 1		Q _{gs1}		_	1.6	_	nC
Gate-drain ("Miller") charge		Q _{gd}	$V_{DD} \simeq 80 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2.2 \text{ A}$	_	1.3	_	
Gate switch charge		Q _{SW}		_	2.0	_	

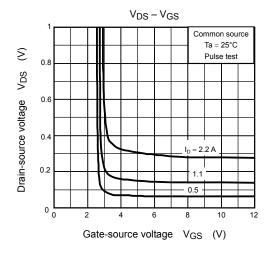
Source-Drain Ratings and Characteristics (Ta = 25°C)

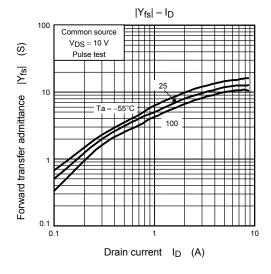
Characteristic		Symbol	Test Condition	Min	Тур.	Max	Unit
Drain reverse current	Pulse (Note 1)	I _{DRP}	_	_	_	8.8	Α
Forward voltage (diode)		V_{DSF}	I _{DR} = 2.2 A, V _{GS} = 0 V	_	_	-1.2	V

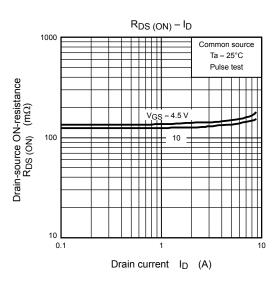


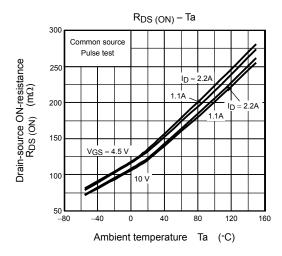


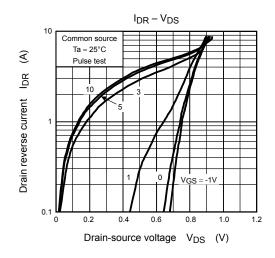


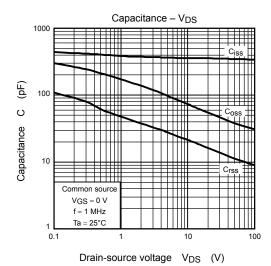


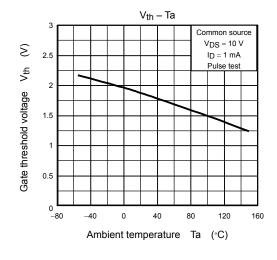


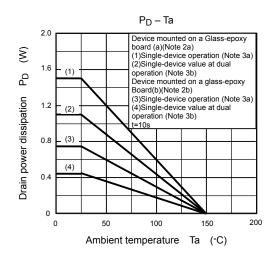


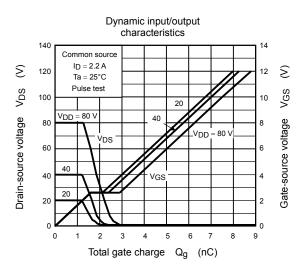


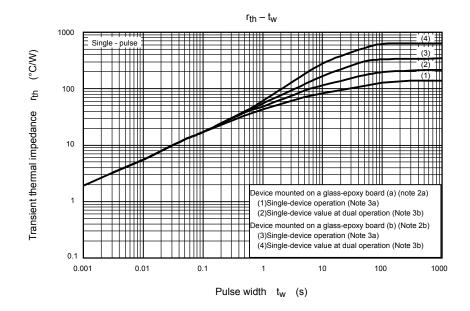


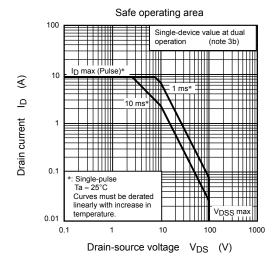












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