Fuji Switching Power Control I C

FA5516
FA5517
FA5518

Application Note

Aug-2005

Warning

1. This Data Book contains the product specifications, characteristics, data, materials and structures as of August 2005. The contents are subject to change without prior notice for specification changes or other reasons. When using a product listed in this Data Book, be sure to obtain the latest specifications and check the data.

2. All applications described in this Data Book give examples of applications of Fuji Electric's products for your reference. No right or license, either express or implied, under any patent, copyright, trade secret or other intellectual property right owned by Fuji Electric Co., Ltd. shall be granted.

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4. The products introduced in this Data Book are intended for use in the following electronic and electrical equipment which requires ordinary reliability:
   - Computers · OA equipment · Communications equipment (terminal devices)
   - Measurement equipment · Machine tools · Audiovisual equipment
   - Electrical home appliances · Personal equipment · Industrial robots, etc.

5. If you need to use a semiconductor product in this Data Book for equipment requiring higher reliability than normal, such as listed below, be sure to contact Fuji Electric Device Technology Co., Ltd. to obtain prior approval. When using these products, take adequate safety measures such as a backup system to prevent the equipment from malfunctioning when a Fuji Electric's product incorporated in the equipment becomes faulty.
   - Transportation equipment (mounted on vehicles and ships) · Trunk communications equipment
   - Traffic-signal control equipment · Gas leakage detectors with an auto-shutoff function
   - Disaster prevention / security equipment · Safety devices

6. Do not use a product in this Data Book for equipment requiring extremely high reliability such as:
   - Space equipment · Airborne equipment · Atomic control equipment
   - Submarine repeater equipment · Medical equipment

7.

8. If you have any question about any portion of this Data Book, ask Fuji Electric Device Technology Co., Ltd. or its sales agencies. Neither Fuji Electric Device Technology Co., Ltd. nor its agencies shall be liable for any injury or damage caused by any use of the products not in accordance with instructions set forth herein.

Contents

Note)

- The contents of this Data Book are subject to change without prior notice for improvement or other reasons.
- Application examples and parts constants listed in this Data Book are intended for design reference, without giving due consideration to unevenness in parts characteristics and usage conditions.
  When using, be sure to design the relevant circuit giving due consideration to unevenness in parts characteristics and usage conditions.

1. Outline

FA5516/17/18 series are current-mode switching power control ICs that can directly drive power MOSFETs. Low-power dissipation is achieved due to adoption of high-withstand voltage CMOS process. In addition, stand-by power consumption can substantially be reduced due to a built-in start-up circuit. Many functions are incorporated in an eight pin package, reducing the number of external parts and allowing compact and high cost performance power supply

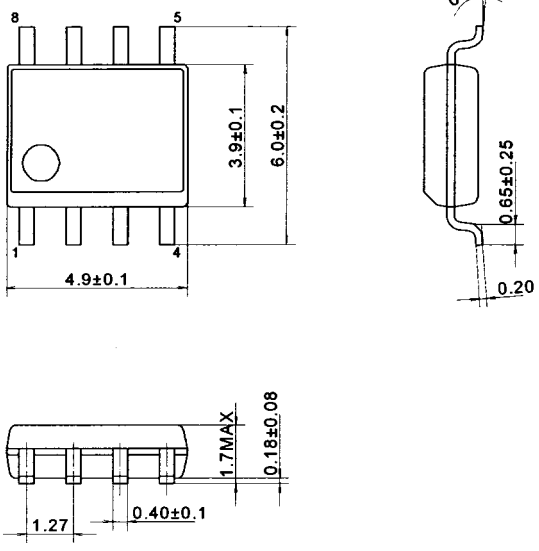
2. Features

- Built-in start-up circuit of 500V withstand voltage that is cut off after start-up (input current after cutoff: 20μA (typ.))
- Low power dissipation due to adoption of high-withstand voltage CMOS process
  During operation : 1.2mA (typ.) (for FA5518)
- Built-in frequency-decreasing function at light load
- Oscillating frequency
  FA5516 : 130kHz(typ.),FA5517 : 100kHz(typ.),FA5518 : 60kHz(typ.)
- Built-in latch-mode cutoff function at overload
- Built-in latch-mode cutoff function at overvoltage
- Built-in malfunction-protective circuit at low voltage (13V ON / 9V OFF)
- 8 pin package (DIP / SOP)

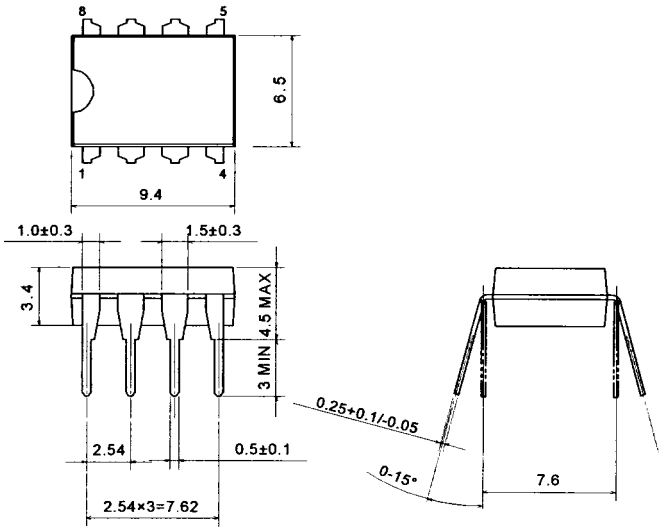
3. External dimension diagram

Unit : mm

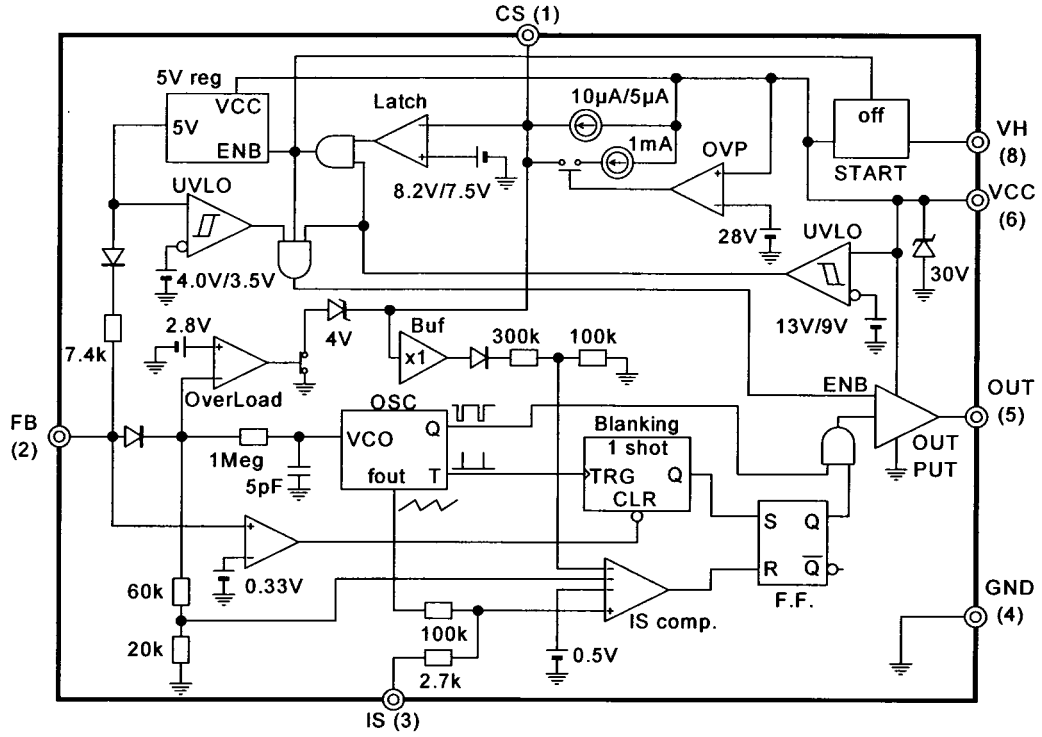
SOP-8 (FA5516N/FA5517N/FA5518N)



DIP-8 (FA5516P/FA5517P/FA5518P)



4. Block diagram



5. Pin assignments

Pin	Symbol	Function	Description
1	CS	Soft start/latch-mode stop	Soft start, latch-mode stop
2	FB	Feedback input	Input for controlling current comparator threshold voltage
3	IS	Current sensor input	Input for monitoring MOSFET current
4	GND	Ground	Power supply ground
5	OUT	Output	Output for directly driving a MOSFET
6	VCC	Power supply	Power supply for ICs
7	(NC)	No connection	No connection
8	VH	High voltage input	Input terminal for start-up circuit

6. Line-up of FA5516/17/18 series

Type	Switching Frequency (kHz)	Package
FA5516P	130 (typ.)	DIP-8
FA5516N		SOP-8
FA5517P	100 (typ.)	DIP-8
FA5517N		SOP-8
FA5518P	60 (typ.)	DIP-8
FA5518N		SOP-8

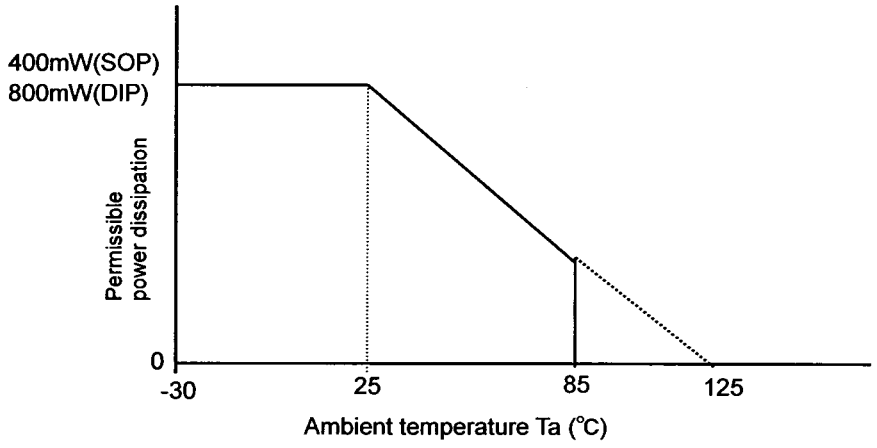
7. Ratings and characteristics

* In defining a current, "+" represents a sink current and "−" a source current.

(1) Absolute maximum ratings

Item		Symbol	Rating	Unit
Supply voltage	Low impedance source (Icc>15mA)	V_{CC1}	28	V
	Built-in Zener clamp (Icc<15mA)	V_{CC2}	Self Limiting	V
OUT pin peak current		I_{OH}	-0.5	A
		I_{OL}	+1.0	A
OUT pin voltage		V_{OUT}	-0.3～VCC+0.3	V
FB/ IS pin voltage		V_{LT}	-0.3～5.0	V
CS pin current		I_{CS}	2.0	mA
CS pin minimum voltage		V_{CSL}	-0.3	V
VH pin Voltage		V_{VH}	-0.3～500	V
Total power dissipation (Ta=25℃)		Pd	800 (DIP-8) 400 (SOP-8)	mW
Ambient temperature		Ta	-30～+85	℃
Maximum junction temperature		Tj	125	℃
Storage temperature		Tstg	□40～+150	℃

Permissible power dissipation decreasing characteristics



(2) Recommended operating conditions

Item		Symbol	MIN	TYP	MAX	Unit
Supply voltage		V_{CC}	10	18	26	V
VH pin voltage	DC	$V_{VH(DC)}$	80		450	V(DC)
	Half-wave rectification	$V_{VH(AC1)}$	80		288	V(AC)
	Full-wave rectification	$V_{VH(AC2)}$	80		288	V(AC)
VH pin series resistor		R_{VH}	2.2		47	k□
CS pin capacitor		C_{CS}	0.01		1	μF
VCC pin capacitor		C_{VCC}	10	33		μF

(3) Electrical characteristics (Vcc=18V, Tj=25°C, unless otherwise specified)

Oscillator (FB pin)

Item	Symbol	Condition		MIN	TYP	MAX	Unit
Oscillating frequency	Fosc	FB=3V	FA5516	117	130	143	kHz
			FA5517	90	100	110	
			FA5518	54	60	66	
Supply voltage stability	Fdv	Vcc=10～26V		-2		2	%
Temperature stability	FdT	Ta=-30～85°C			-0.07		%/°C
FB pin voltage for the start of frequency decrease	VfbM			0.9	1.0	1.1	V
Frequency reduction ratio	kf	⊿f/⊿VFB FB=0.8V ～ 0.9V	FA5516		310		kHz/V
			FA5517		240		
			FA5518		140		
Oscillating frequency at light load	F06	FB=0.6V	FA5516		13		kHz
			FA5517		10		
			FA5518		7		
Minimum frequency	Fmin			0.5	1.5	4.0	kHz

Pulse width modulator (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum duty cycle	D_{MAX}	FB=3V,CS=3V	76	80	84	%
Minimum duty cycle	D_{MIN}	FB=0V,CS=3V			0	%
FB voltage for pulse stop	V_{THFB0}	Duty cycle=0%	230	330	430	mV
FB pin current	I_{fb0}	FB=0V	-620	-520	-420	μA

Current sensor (IS pin)

Item	Symbol	Condition		MIN	TYP	MAX	Unit
Voltage gain	A_{VIS}	⊿VFB/⊿VIS		3.8	4.0	4.2	V/V
Maximum threshold voltage	V_{thIS1}	FB=4V,duty=10%		450	500	550	mV
Duty cycle for starting slope compensation	DSS		FA5516		36.0		%
			FA5517		34.6		
			FA5518		31.7		
Slope compensation value	SLP	FB=4V	FA5516		-24		mV/μs
			FA5517		-17.5		
			FA5518		-10		
Input bias current	I_{IS}	VIS=0V Average current	FA5516		-8.5		μA
			FA5517		-9.0		
			FA5518		-9.5		
Minimum ON pulse width	Tmin	FB=3V CS=0V IS=1V	FA5516		0.4		μs
			FA5517		0.6		
			FA5518		0.8		
Blanking time	Tblank		FA5516		0.2		μs
			FA5517		0.4		
			FA5518		0.6		
Output delay time	T_{pdIS}	IS to OUT			200		ns

Soft-start circuit (CS pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Charging current	I_{CS0}	CS=0V	-14	-10	-5	μA
Threshold voltage for changing charging current	V_{THCS1}			3		V
Input threshold voltage	V_{THCS0}	OUT=Tmin, FB=3V		0.6		V

Latch-mode cutoff circuit (CS pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Charging current	I_{CS4}	CS=4V	-7	-5	-2.5	μA
Sink current	I_{sink}	CS=6V	20	35	50	μA
Cutoff threshold voltage	V_{THCSF}	ON→OFF	7.7	8.2	8.7	V
	V_{THCSN}	OFF→ON	7.0	7.5	8.0	V
Hysteresis width	V_{THHYS}			0.7		V
Clamp voltage at latch mode	V_{CS2}	FB=open		8.8		V

Cutoff circuit at overload (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Detection threshold voltage	V_{THFB}		3.2	3.5	3.8	V

Cutoff circuit at overvoltage (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Threshold voltage	V_{THVCC}		26.0	28.0	30.0	V
CS pin charging current	I_{SOCS2}	CS=4V		-1.0		mA

Malfunction-protective circuit at low voltage (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
ON threshold voltage	V_{CCON}		11.5	13.0	14.5	V
OFF threshold voltage	V_{CCOFF}		8.0	9.0	10.0	V
Hysteresis width	V_{HYS}		3.0	4.0	5.0	V

Output section (OUT pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Low output voltage	V_{OL}	I_{OL}=100mA		0.3	0.6	V
High output voltage	V_{OH}	I_{OH}=-100mA,V_{CC}=18V	14.8	16.4		V
Rise time	tr	CL=1nF		50		ns
Fall time	tf	CL=1nF		40		ns

High voltage input section (VH pin, VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
VH pin input current	IHrun	VH=450V,Vcc> Vccon	10	20	30	μA
	IHstb	VH=100V,Vcc=0V		3.4		mA
VCC voltage at latch mode	VCCL	VH=100V		22		V
VCC pin charging current	Ipre1	Vcc=10V,VH=100V		-2.4	-1.4	mA
	Ipre2	Vcc=13V,VH=100V at latch mode		-1.7	-0.9	mA

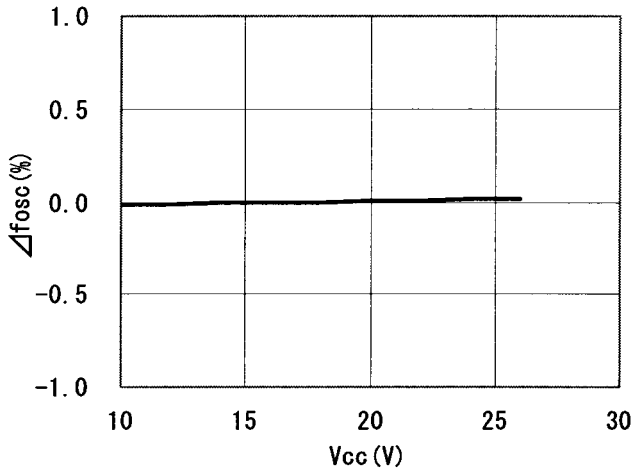
Consumption current (VCC pin)

Item	Symbol	Condition		MIN	TYP	MAX	Unit
Supply current during operation	ICCOP1	Duty cycle =DMAX, FB=3V, no load	FA5516		1.4	2.0	mA
			FA5517		1.3	2.0	
			FA5518		1.2	2.0	
	ICCOP2	Duty cycle=0%, FB=0V			1.3	2.0	mA
Consumption current at latch mode	ICCL	FB=open, CS=open			270	350	μA
Zener voltage	Vz	Iz=2mA			30		V

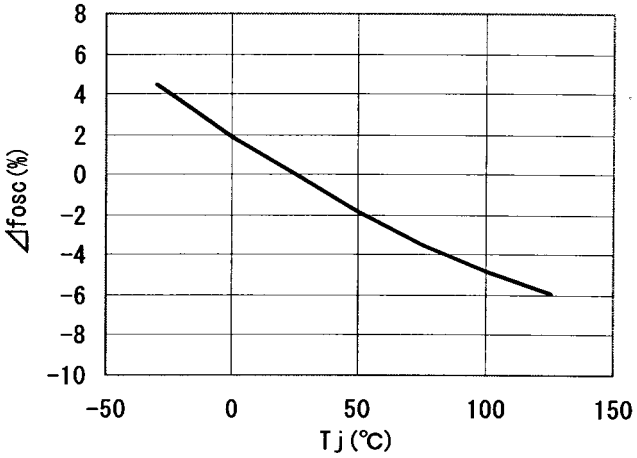
8. Characteristic curves

- Unless otherwise specified, Ta=25℃, Vcc=18V
- In defining a current, "+" represents a sink current and "-" a source current.
- The data stated in this chapter are intended for giving typical IC characteristics and not for guaranteeing performance.

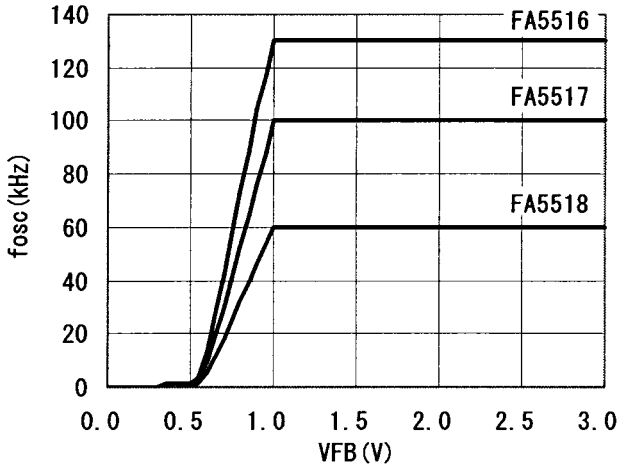
発振周波数変化率(⊿fosc) vs. 電源電圧(Vcc)



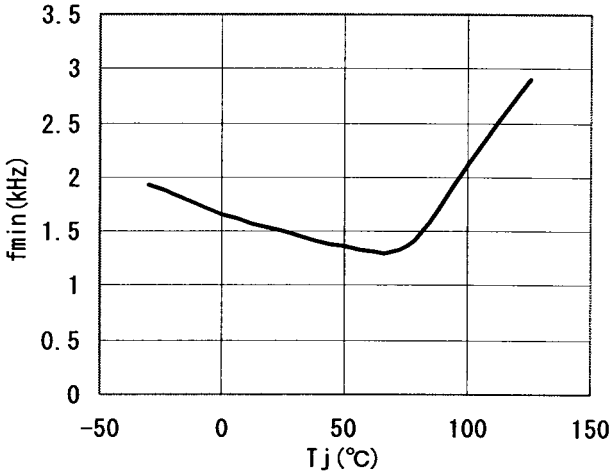
発振周波数変化率(⊿fosc) vs. ジャンクション温度(Tj)



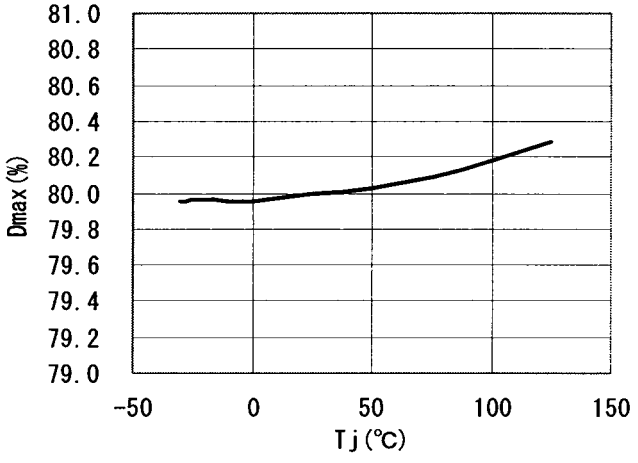
発振周波数(fosc) vs. FB端子電圧(VFB)



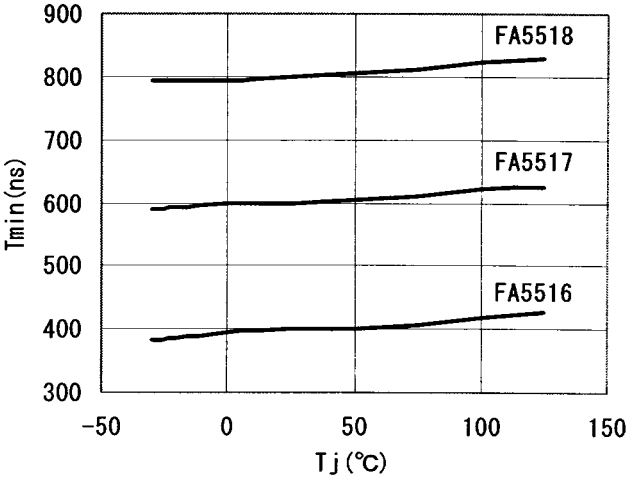
最低周波数(fmin) vs. ジャンクション温度(Tj)



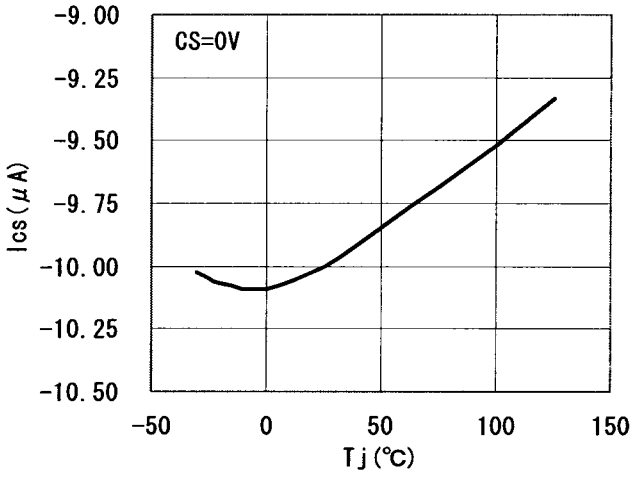
最大デューティーサイクル(Dmax) vs. ジャンクション温度(Tj)



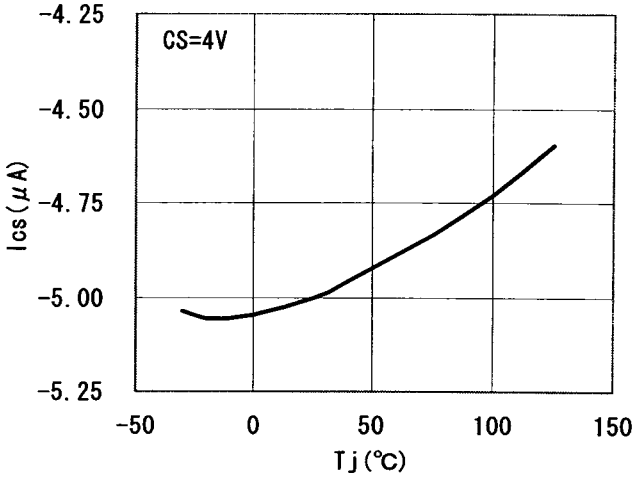
最低オン幅(Tmin) vs. ジャンクション温度(Tj)



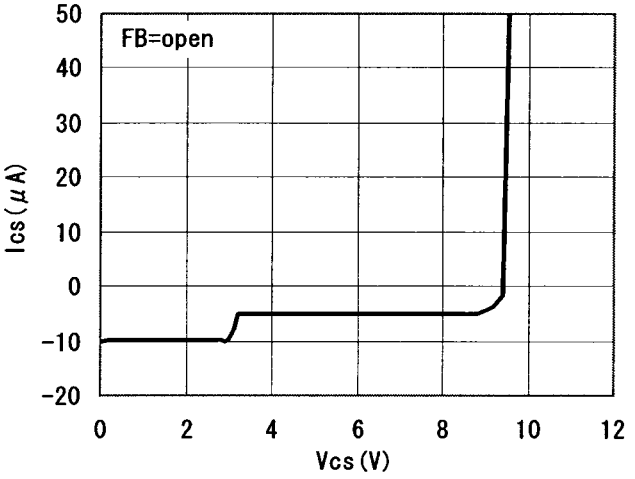
CS端子充電電流(Ics) vs. ジャンクション温度(Tj)



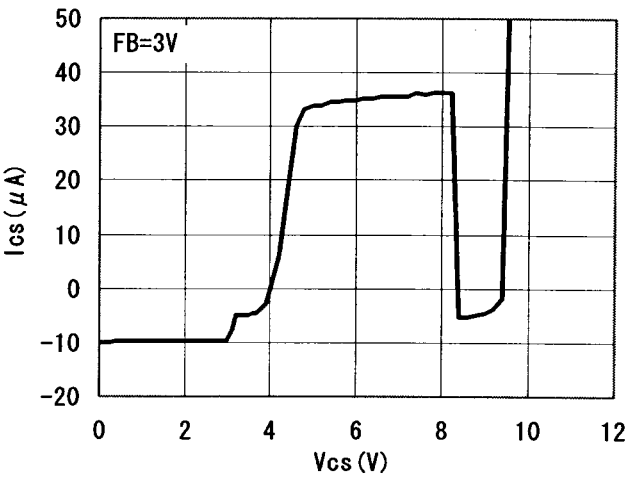
CS端子充電電流(Ics) vs. ジャンクション温度(Tj)



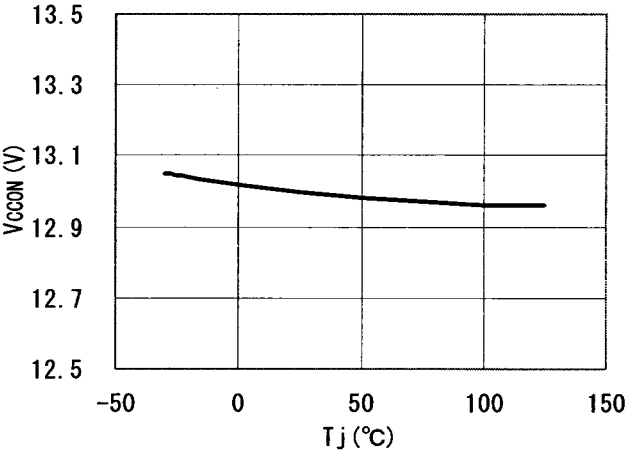
CS端子電流(Ics) vs. CS端子電圧(Vcs)



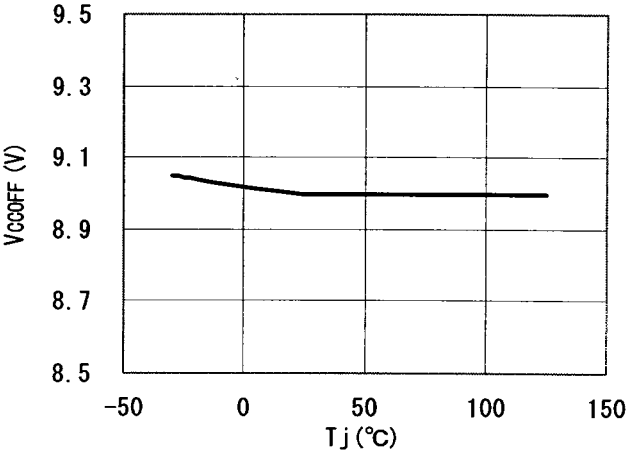
CS端子電流(Ics) vs. CS端子電圧(Vcs)



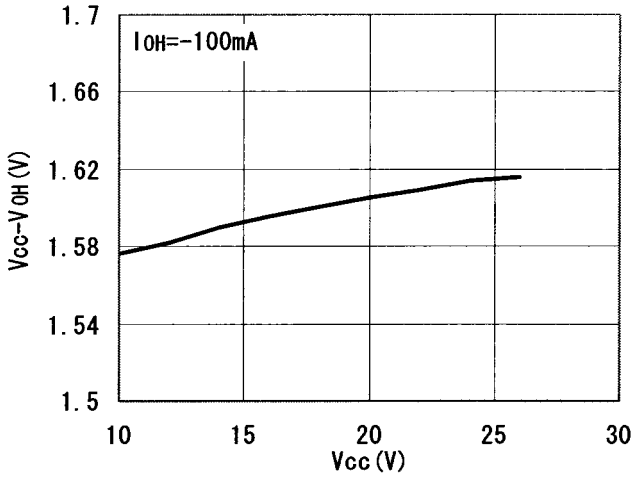
UVLO ONスレッシュ電圧(VCCON)
vs. ジャンクション温度(Tj)



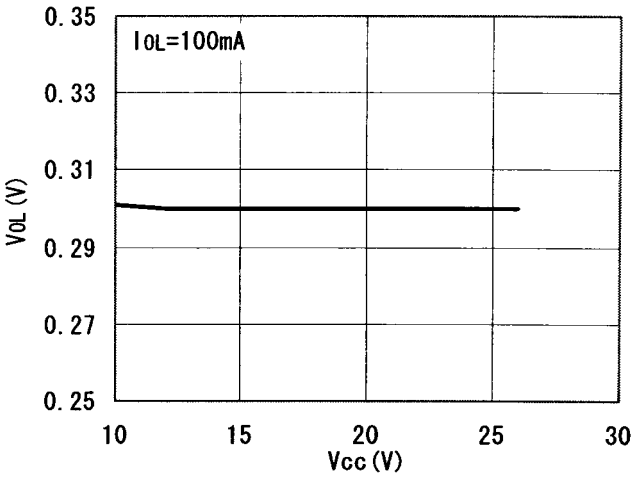
UVLO OFFスレッシュ電圧(VCCOFF)
vs. ジャンクション温度(Tj)



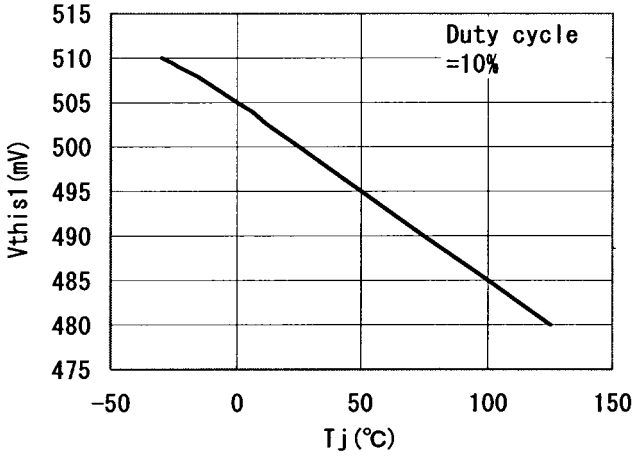
OUT端子H出力電圧(VOH) vs. 電源電圧(Vcc)



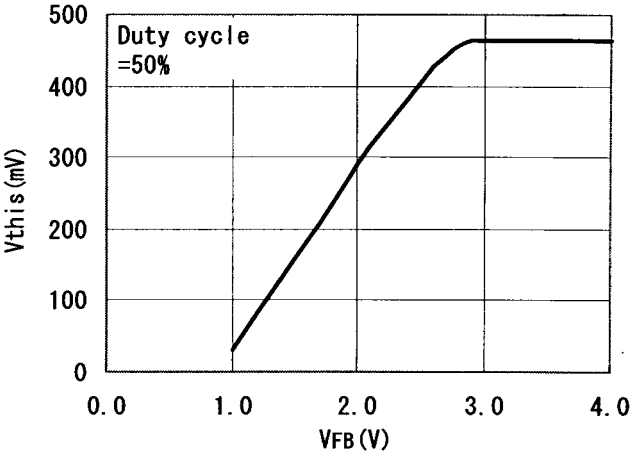
OUT端子L出力電圧(VOL) vs. 電源電圧(Vcc)



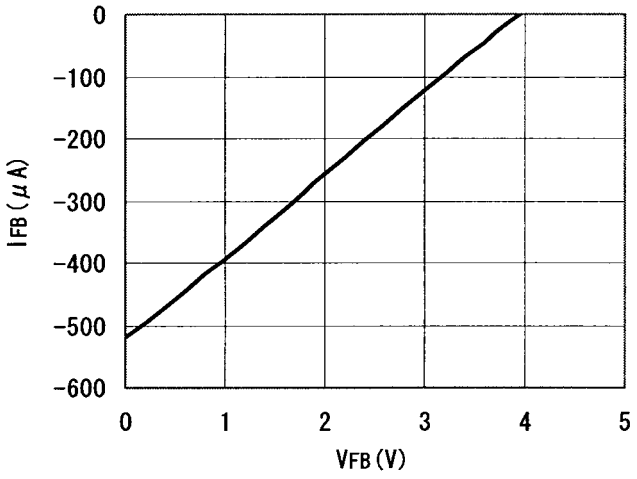
IS端子 最大入力スレッシュ電圧(Vthis1) vs. ジャンクション温度(Tj)



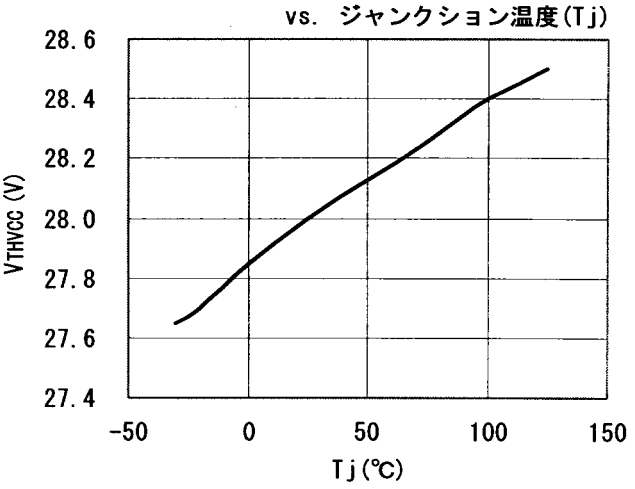
IS端子 入力スレッシュ電圧(Vthis) vs. FB端子電圧(VFB)



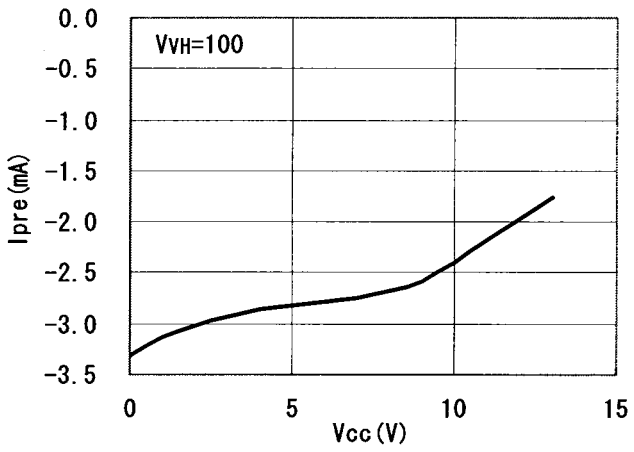
FB端子電流(IFB) vs. FB端子電圧(VFB)



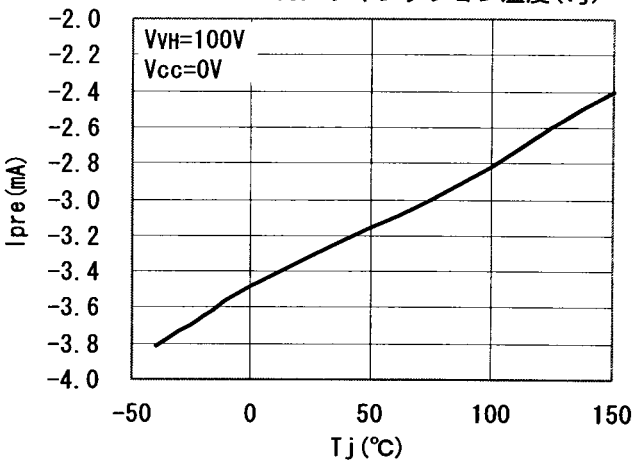
VCC端子 過電圧時遮断回路 スレッシュ電圧(VTHVCC) vs. ジャンクション温度(Tj)



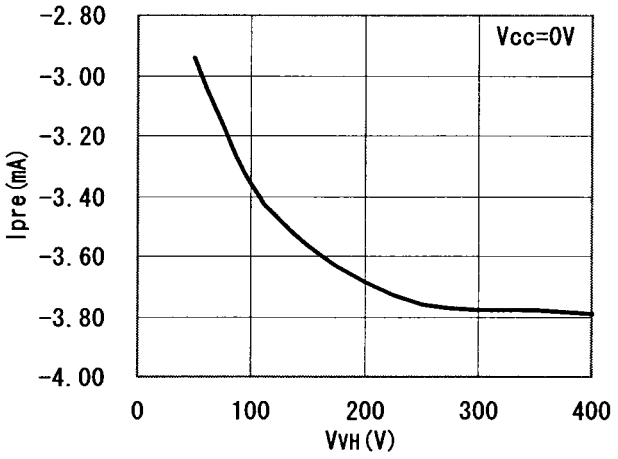
起動回路　VCC端子充電電流(Ipre)
vs.　電源電圧(Vcc)



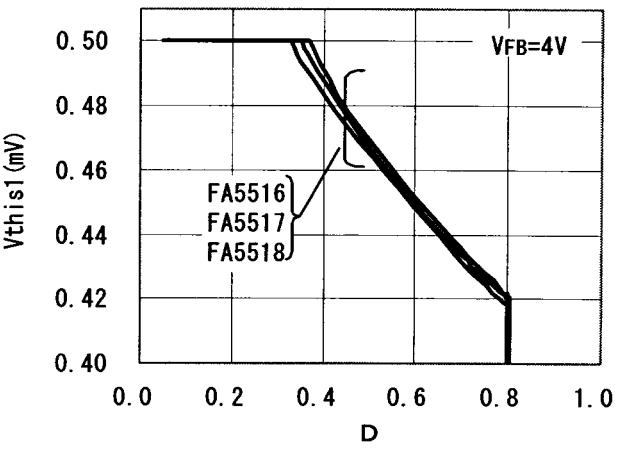
起動回路　VCC端子充電電流(Ipre)
vs.　ジャンクション温度(Tj)



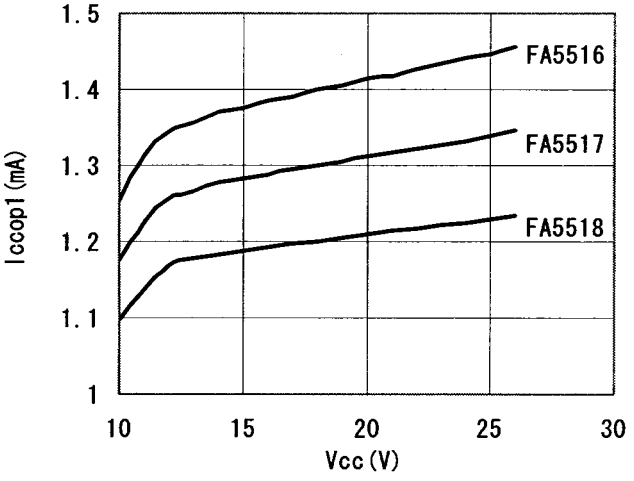
起動回路　VCC端子充電電流(Ipre)
vs.　VH端子電圧(VVH)



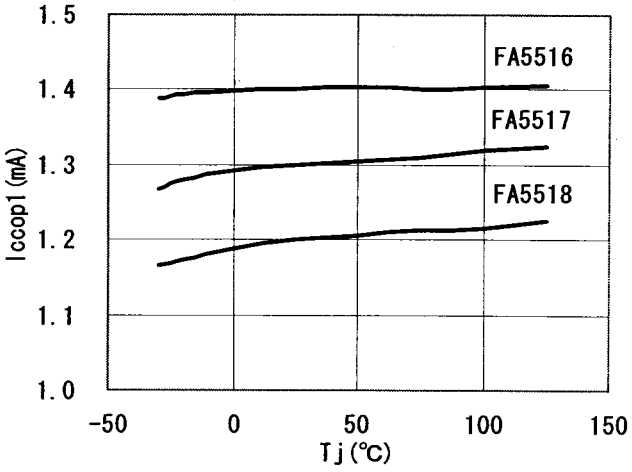
IS端子　最大入力スレッシュ電圧(Vthis1) vs.
デューティーサイクル(D)



動作時電源電流(Iccop1) vs.　電源電圧(Vcc)



動作時電源電流(Iccop1) vs.　ジャンクション温度(Tj)



9. Description of block circuits

(1) Start-up circuit

The FA5516/17/18 has built-in start-up circuits with maximum rated voltage of 500V.

Wiring is shown in **Figs.1** to **3**.

When power is turned on, a current is supplied to the VCC pin from the start-up circuit, charging the capacitor, C2, connected to the VCC pin, increasing its voltage, activating the IC, and the power supply starts operation.

The current supplied to the VCC pin from the VH pin is approximately 3mA at Vcc=0V, decreases as Vcc increases and becomes approximately 1.7mA at the start-up voltage. A resistor is connected in series to the VH pin to prevent the IC from being damaged due to surge voltage in AC and other lines.

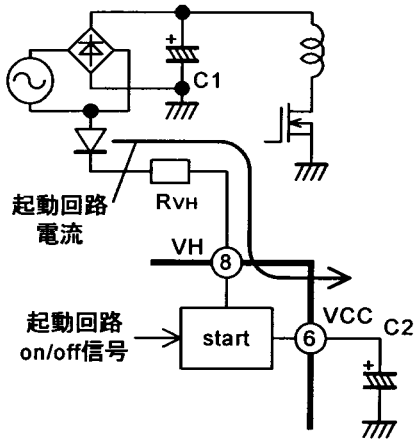


Fig.1 Start-up circuit 1 (half wave)

Fig.1 shows the commonest wiring, connecting the VH pin to half-wave rectified AC input voltage and taking the longest start-up time of the three ways of wiring. When AC input voltage is turned off after the circuit changed to a latch mode due to overload or overvoltage protection, the latch mode can be reset in a relatively short time of several seconds because a current is not supplied from the VH pin.

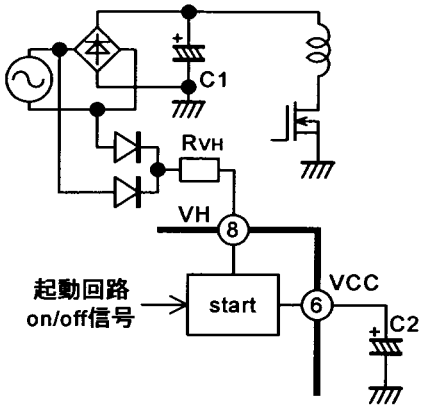
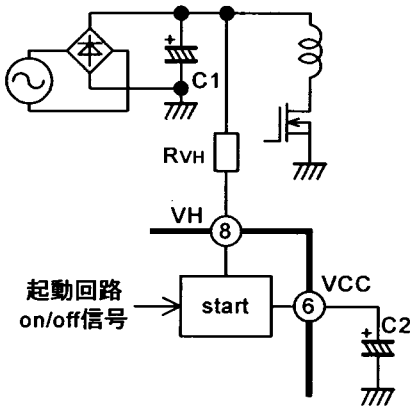


Fig.2 Start-up circuit 2 (full wave)

In **Fig.2**, the VH pin is connected to full-wave rectified AC input voltage, reducing start-up time to approximately half as compared to half-wave rectification circuit shown in **Fig.1**. The latch mode can be reset in a short time same as in **Fig.1** because AC input voltage is cut off.

In **Fig.3**, the VH pin is connected to rectified and smoothed AC input voltage, resulting in the shortest start-up time of the three ways of wiring. In this way of wiring, it takes time for the latch mode to be reset because charged C1 voltage is applied to the VH pin even if the IC have changed to the latch mode. Depending on usage conditions, in general it takes several minutes.

When VCC pin voltage exceeds ON threshold voltage of the low-voltage malfunction-protective circuit and the IC is activated, the start-up circuit is cut off and VH pin input current becomes 20μA (typ.).



※注意:図3の接続は、AC入力を遮断しても、
ラッチモードのリセットに数分必要

Fig.3 Start-up circuit 3 (DC)

When the IC changes to the latch mode due to overload or overvoltage protection, the start-up circuit is activated again, the latch condition is maintained and Vcc voltage is held at approximately 22V.

(See "9.-(8) Overload protection," "9.-(9) Overvoltage protection.")

(2) Oscillator

The oscillator determines switching frequency. For normal operation, the oscillating frequency is set at 130kHz for FA5516, 100kHz for FA5517 or 60kHz for FA5518 inside the IC.

In addition, the IC has a function to automatically decrease oscillating frequency at light load to reduce standby power dissipation. When FB pin voltage becomes 1.0V or less at light load, the frequency starts decreasing.

At light load, as FB pin voltage drops, the frequency decreases almost linearly to the minimum operating frequency (**Fig.4**). The minimum operating frequency, Fmin, is set at 1.5kHz.

The oscillator generates a trigger signal for determining the switching frequency, a pulse signal for determining the maximum duty cycle and a ramp signal for slope compensation.

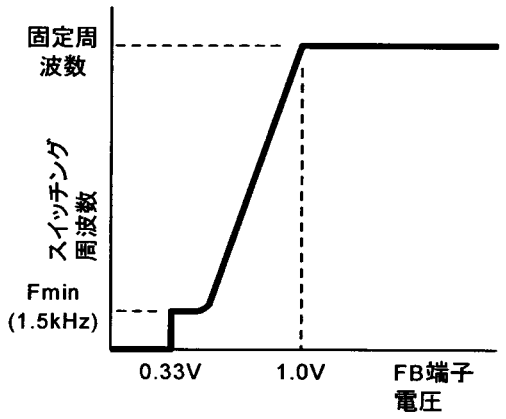


Fig.4 Oscillating frequency

(3) Current comparator and PWM latch

FA5516/17/18 are current mode comparators. **Fig.5** shows a block diagram for basic operation and **Fig.6** a timing chart.

A trigger signal is generated by the oscillator and input to the PWM latch (F.F.) as a set signal through a blanking circuit, increasing PMW latch output and also OUT pin voltage.

On the other hand, the current comparator (IS comp.) monitors a MOSFET current and generates a reset signal when OUT pin voltage reaches the threshold voltage. Then, PWM latch (F.F.) output and OUT pin voltage go into low state

The output is controlled through varying IS comparator threshold voltage due to a feedback signal.

As shown in **Fig.7**, FB pin voltage and CS pin voltage are level-shifted and input to the current comparator (IS comp.) as threshold voltage. In addition, the reference voltage of 0.5V is input to the IC to determine IS pin maximum threshold voltage.

The lowest of the three inputs is given a high priority.

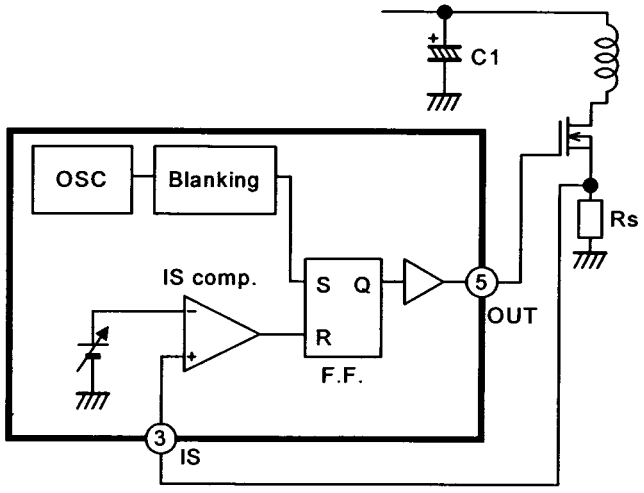


Fig.5 Current-mode basic operation circuit block

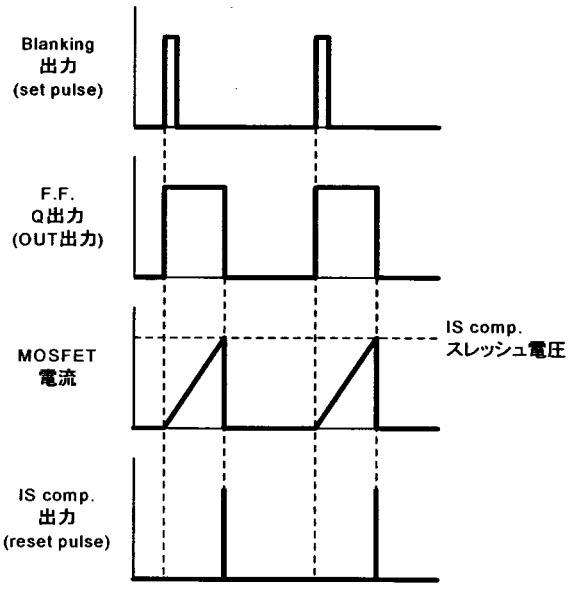


Fig. 6 Timing chart for current-mode basic operation

At start-up, soft start can be realized through gradually increasing the threshold voltage based on CS pin voltage.

At normal operation, the threshold voltage is varied based on FB pin voltage to keep power supply output voltage constant.

In addition, the maximum IS pin threshold voltage limits MOSFET overcurrent. The maximum threshold voltage is 500mV (typ.) over the range where the duty cycle is 30% or less. When the duty cycle exceeds 30%, the maximum threshold voltage varies due to slope compensation as described later. For details, refer to the mid right diagram "IS pin maximum input threshold voltage vs. duty cycle" in p.13.

The oscillator generates a pulse to determine the maximum duty cycle of an OUT pulse and the maximum duty cycle is set at 80% (typ.) using this pulse..

For details, refer to "9-(12) Timing chart" in p.21.

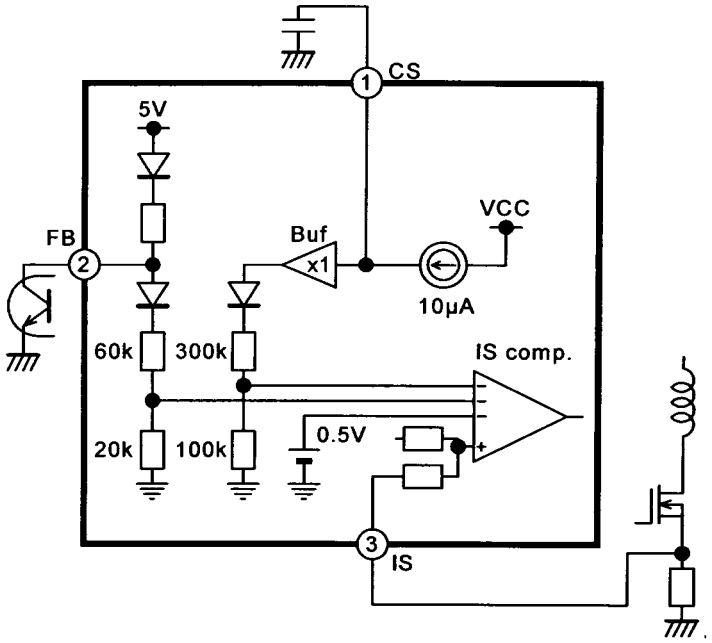


Fig.7 Current comparator

(4) Blanking

When MOSFET turns on, a surge current is generated due to discharge current from the capacitor in the main circuit or gate drive current. If the surge current reaches the IS pin threshold voltage, current comparator output could be inverted and normal pulses would not be generated from the OUT pin.

To avoid this, a blanking function is incorporated into the current comparator. When a trigger signal is input from the oscillator, the blanking circuit outputs a certain-width pulse signal as a PWM latch (F.F.) set signal.

Since the set signal is given a high priority in PWM latch input signals, the output of PWM latch (F.F.) will not be inverted while the set signal is input from the blanking circuit, even if a rest signal is input from the current comparator (IS comp.).

As a result, the IS pin input voltage is ignored for a blanking time (200ns for FA5516, 400ns for FA5517 and 600ns for FA5518) immediately after an output pulse has been generated from the OUT pin and does not respond to a surge current at turn-on.

(See **Fig.8.**)

In general, the blanking circuit eliminates the need for a noise filter at the IS pin.

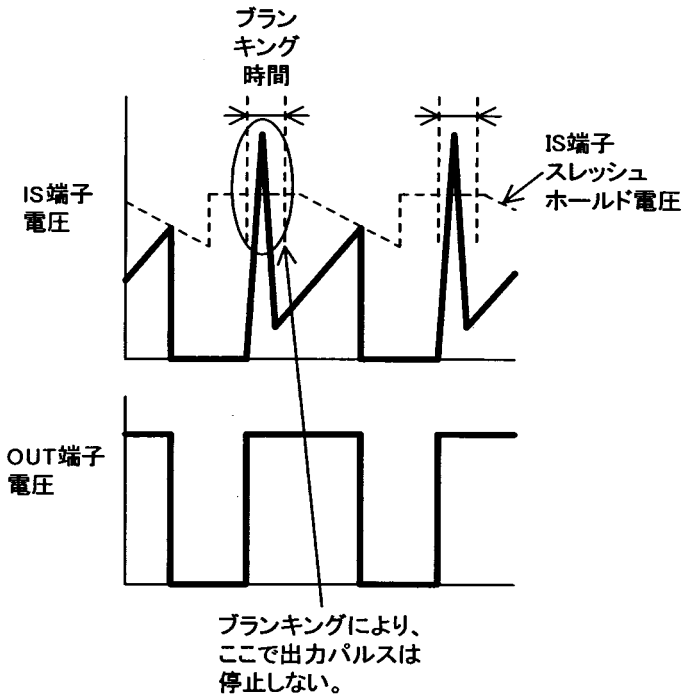


Fig.8 Blanking

(5) Minimum ON pulse width

As described in "(4) Blanking," the input voltage at the IS pin is ignored during a blanking period right after turn-on. Consequently, the sum of blanking time and output delay time (200ns) is the minimum ON pulse width at the OUT pin of the IC. The minimum ON pulse width for FA5516, FA5517 and FA5518 are 400ns, 600ns and 800ns, respectively.

In addition, a dedicated comparator is incorporated not to generate pulses at no load.

When FB pin voltage is below 0.33V or less, the output of the comparator is inverted and a clear signal "CLR" is input to the blanking circuit. Then, the blanking circuit will not output a set signal and no set signals will be input to PMW latch (F.F.), keeping the output voltage low.

(See "9-(12) Timing chart.")

(6) Slope compensation

In the current mode control, subharmonic oscillation may occur at a continuous current mode operation with a duty cycle of 50% or more.

To avoid this, FA5516, FA5517 and FF5518 have built-in slope compensation circuits.

For details of subharmonic oscillation phenomenon and slope compensation effect, see p.31.

As shown in **Fig.9**, a ramp signal generated from the oscillator and an MOSFET source current signal are combined and input to the current comparator (IS comp.) to realize slope compensation.

When the duty cycle exceeds 50%, slope compensation is needed to prevent subharmonic oscillation. Therefore, a ramp signal is set to be added only when the duty cycle exceeds 30%. (slope compensation start duty cycle: 36% for FA5516, 34.6% for FA5517 and 31.7% for FA5518)

While the ramp signal is added, the threshold voltage at the FB pin gradually decreases with time within each switching cycle as shown in **Fig.10** even when voltages at the FB pin and CS pin are constant.

(See "9-(12) Timing chart.")

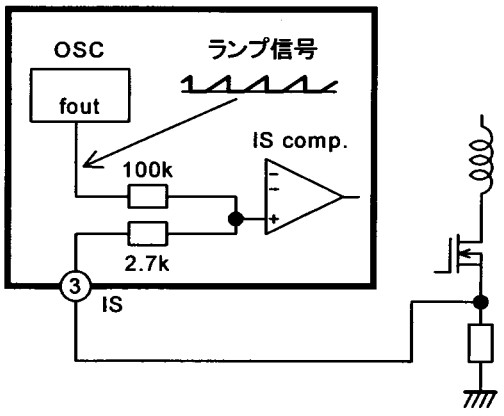


Fig.9 Slope compensation circuit

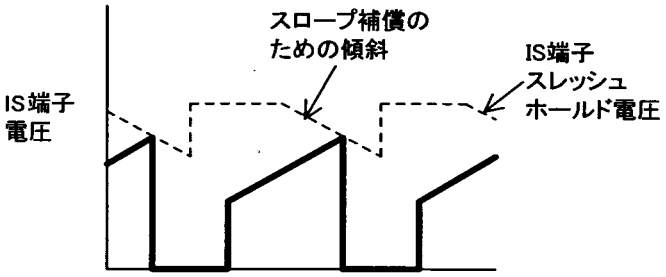


Fig.10 Slope compensation

(7) Soft start circuit

The CS pin is connected to a built-in constant current source. The current for soft start is 10μA.

The capacitor externally connected to the CS pin is charged by the constant current source, gradually increasing CS pin voltage.

MOSFET current gradually increases at start-up because CS pin voltage is input to the current comparator (IS comp.), realizing soft start.

As a guide for soft start time, the time tss taken until CS pin voltage increases from 0V to 3V is given by the following equation.

tss(s)=0.3 × Cs[μF] (typical value)
where Cs is CS pin capacitance (μF).

In normal operation, CS pin voltage is clamped at approximately 4V by a zener diode in the IC.

The FB pin is provided with a built-in circuit to stop pulses when FB pin voltage is 0.33V or less, but the CS pin is not provided with such a circuit. As a result, OUT pulses of minimum ON width are output even when CS pin voltage is 0V.
(See "9-(12) Timing chart.")

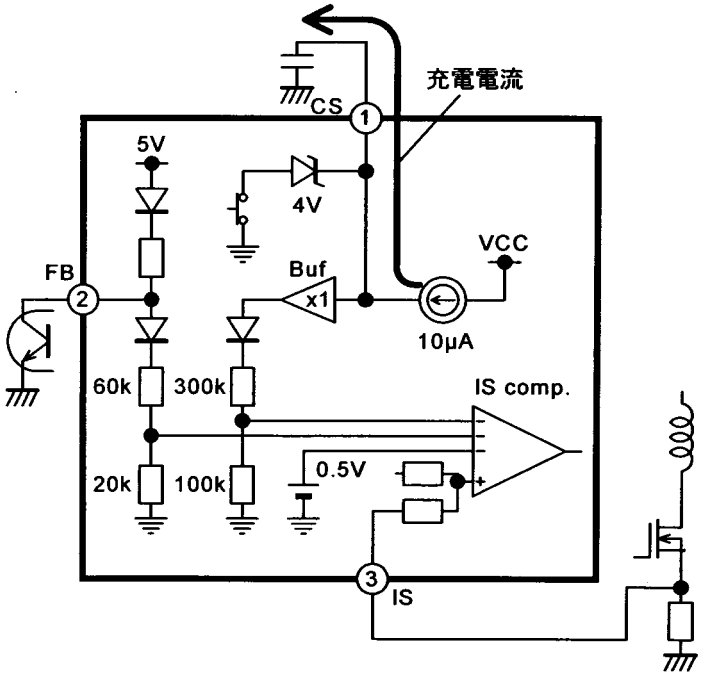


Fig.11 Soft start circuit

(8) Overload protection

FA5516, FA5517 and FA5518 have built-in time-latch type overload protection. **Fig.12** shows its block diagram and **Fig.13** its Timing chart.

In normal operation, FB pin voltage is 3V or less and CS pin voltage is clamped at 4V by a zener diode in the IC.

When power supply voltage drops on account of overload or short-circuit on the load side, FB pin voltage increases. If the voltage exceeds the threshold voltage for overload protection, 3.5V, output voltage of a comparator for overload detection (Overload) is inverted and 4V clamp of the CS pin is canceled, increasing CS pin voltage again due to a built-in constant current source. The current supplied from the CS pin becomes 5μA.

If the power supply voltage continues to decrease and CS pin voltage reaches the threshold voltage (8.2V) of the comparator (Latch), the output of the comparator (Latch) is inverted, turning off a 5V circuit in the IC and forcing OUT pin voltage to be low.

This status is the latch mode of the IC. In the latch mode, the start-up circuit resumes operation to supply current to Vcc and to hold the latch mode.

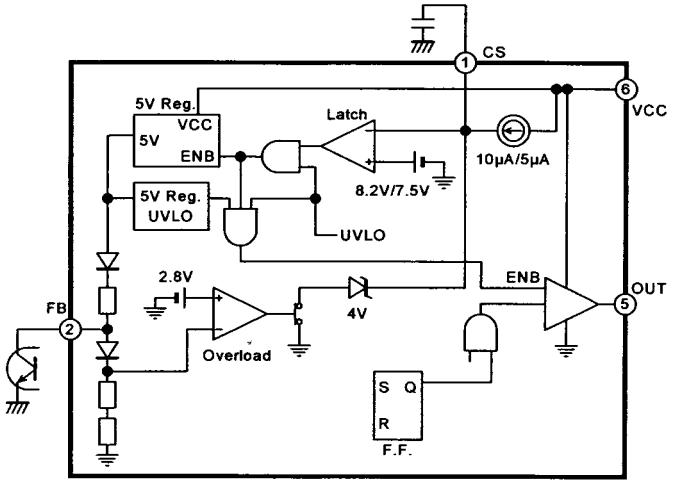


Fig.12 Overload protection circuit

When the output voltage momentarily drops due to abrupt load change and FB pin voltage restores to normal voltage before CS pin voltage reaches 8.2V, the 4V clamp circuit restarts, producing no latch mode.

The latch mode can be reset through cutting off input voltage or through forcibly decreasing CS pin voltage to 7.0V or less.

Cutting off the input voltage decreases VH pin voltage, supplying no current to the VCC pin. Thereafter, the latch mode is reset when Vcc drops below the OFF threshold voltage, 8.0Vmin.

In addition, when CS pin voltage is forcibly decreased, the latch mode comparator is re-inverted and the IC re-starts switching operation.

In the case of typical IC, delay time td (OLP), the time from overload detection to the latch mode, is given by the following equation.

$$td_{(OLP)}(s) = 0.84 \times Cs[\mu F] \quad (\text{typical value})$$

Where Cs is CS pin capacitance (μF).

Delay time td(OLP) is inversely proportional to CS charging current and proportional to the difference between CS pin clamp voltage and latch-mode threshold voltage at normal condition. Pay attention to variations in delay time resulting from variations in numerical values.

In addition, be aware that when the VH pin is connected after rectification, it takes rather long time, approximately several minutes, before the latch mode is reset.

(See "9-(1) Start-up circuit.")

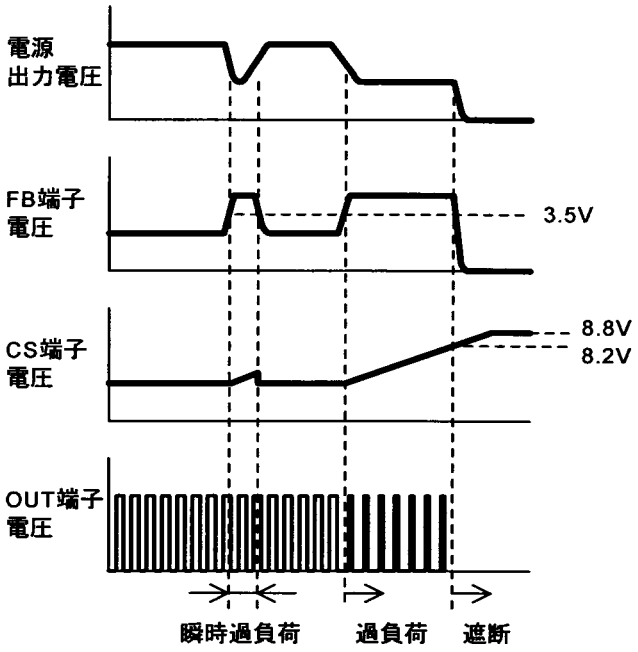


Fig.13 Overload protection timing chart

(9) Overvoltage protection

FA5516, FA5517 and FA5518 have built-in overvoltage protection circuits to monitor Vcc voltage. **Fig.14** shows its block diagram and **Fig.15** its timing chart.

When VCC voltage increases and exceeds comparator (OVP) reference voltage, 28V, an internal 1mA constant current source is tuned on.

Since sink capability of the zener diode which clamps the CS pin at 4V is 35μA, CS pin voltage quickly increases when the 1mA constant current source is turned on. When CS voltage exceeds comparator (Latch) reference voltage, 8.2V, the IC changes to the latch mode.

In the case of typical IC, delay time td (OLP), the time from overload detection to the latch mode, is given by the following equation.

td (OLP) (ms)=4.2 × Cs[μF] (typical value)
Where Cs is CS pin capacitance (μF).

In the latch mode, an internal power supply source, 5V Reg circuit, is turned off and OUT pin voltage is held to be low., and the current form the CS pin changes to 5μA.

The latch mode can be reset through decreasing Vcc voltage due to cutting off of input voltage or through forcibly decreasing CS pin voltage to 7.0V or less. Moreover, pay attention to the relationship between wiring at the VH pin and reset time in the latch mode.
(See "9-(1) Start-up circuit.")

(10) Undervoltage lockout circuit

The IC has a built-in undervoltage lockout circuit to prevent malfunction when Vcc voltage drops. When Vcc voltage increases from 0V, the IC starts operation at Vcc=13V(typ.). As the supply voltage decreases, the IC stops operation at Vcc=9V(typ.).

When the undervoltage lockout circuits operates and the IC stops operation, OUT pin and CS pin voltage are forced to be low, resetting soft start, and overload and overvoltage timer latch protection.

(11) Output circuit

The output circuit consists of push-pull configuration, capable of directly driving a MOSFET. The maximum peak currents at the OUT pin are 0.5A for source current and 1.0A for sink current.

If the IC stops operation when the undervoltage lockout circuit operates or in the latch mode, OUT pin voltage is forced to be low to shut down the MOSFET.

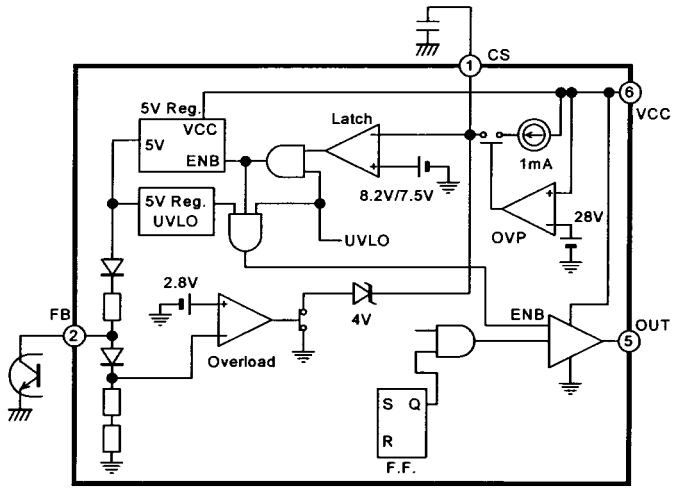


Fig.14 Overvoltage protection circuit

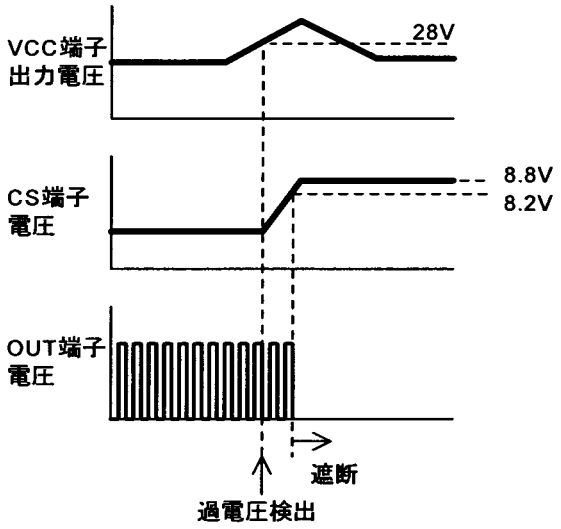


Fig.15 Overvoltage protection timing chart

(12) Timing chart

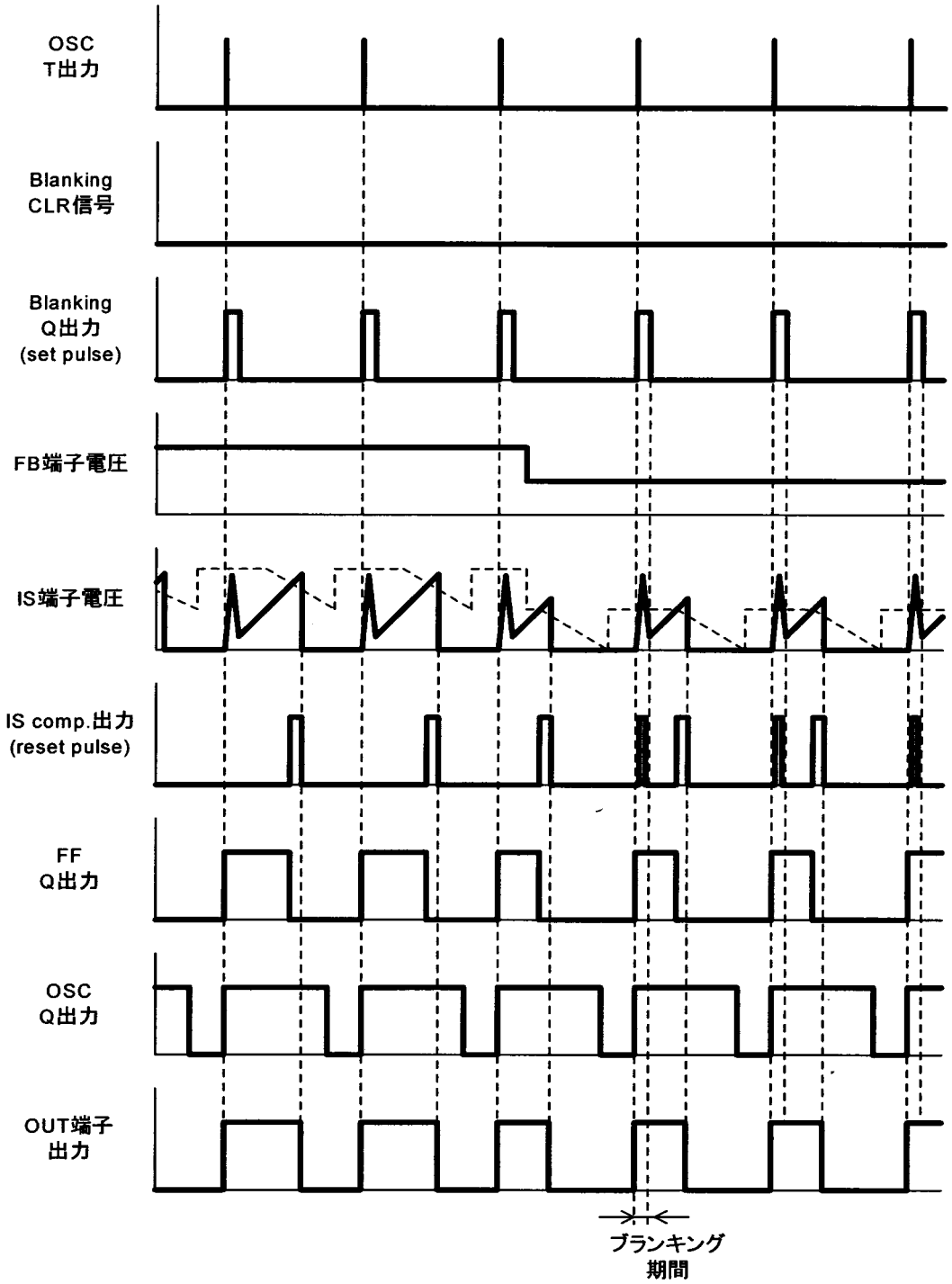


Fig.16 Timing chart at normal operation

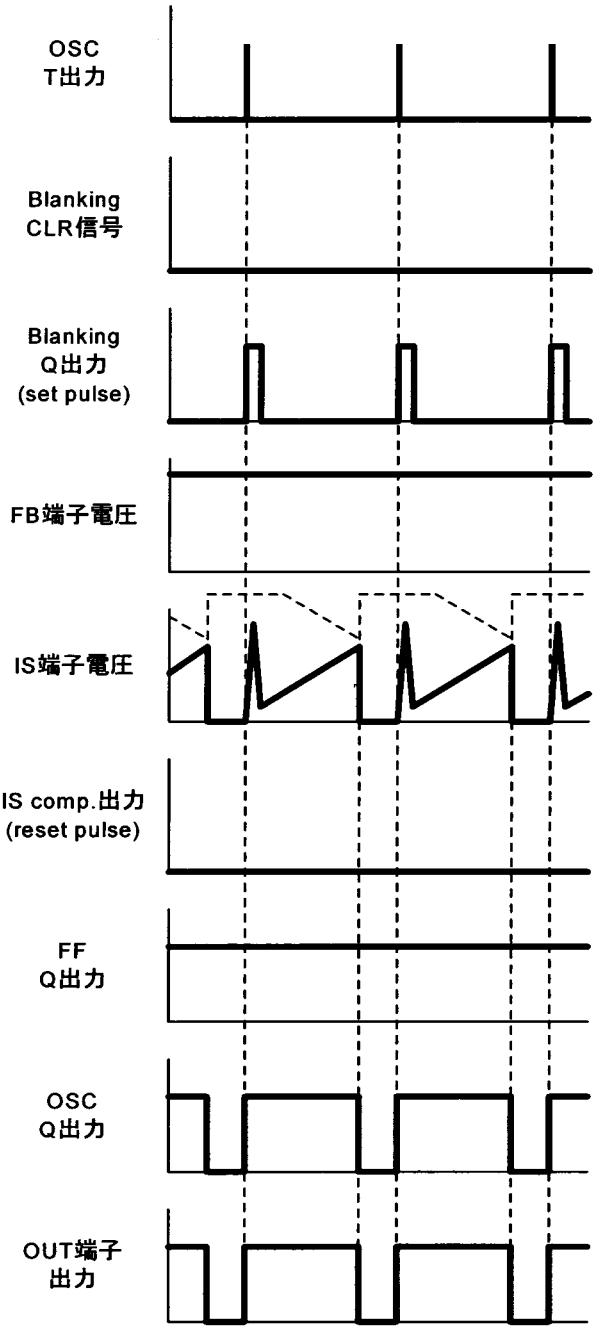


Fig.17 Timing chart when Dmax operates

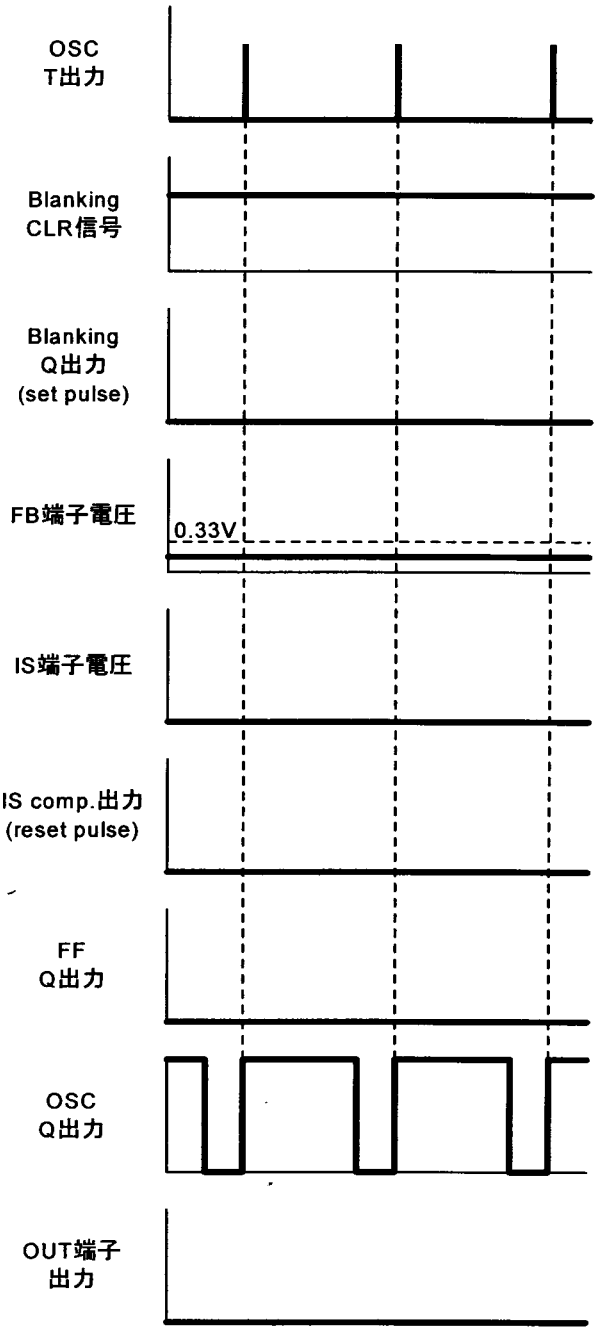


Fig.18 Timing chart at FB<0.33V

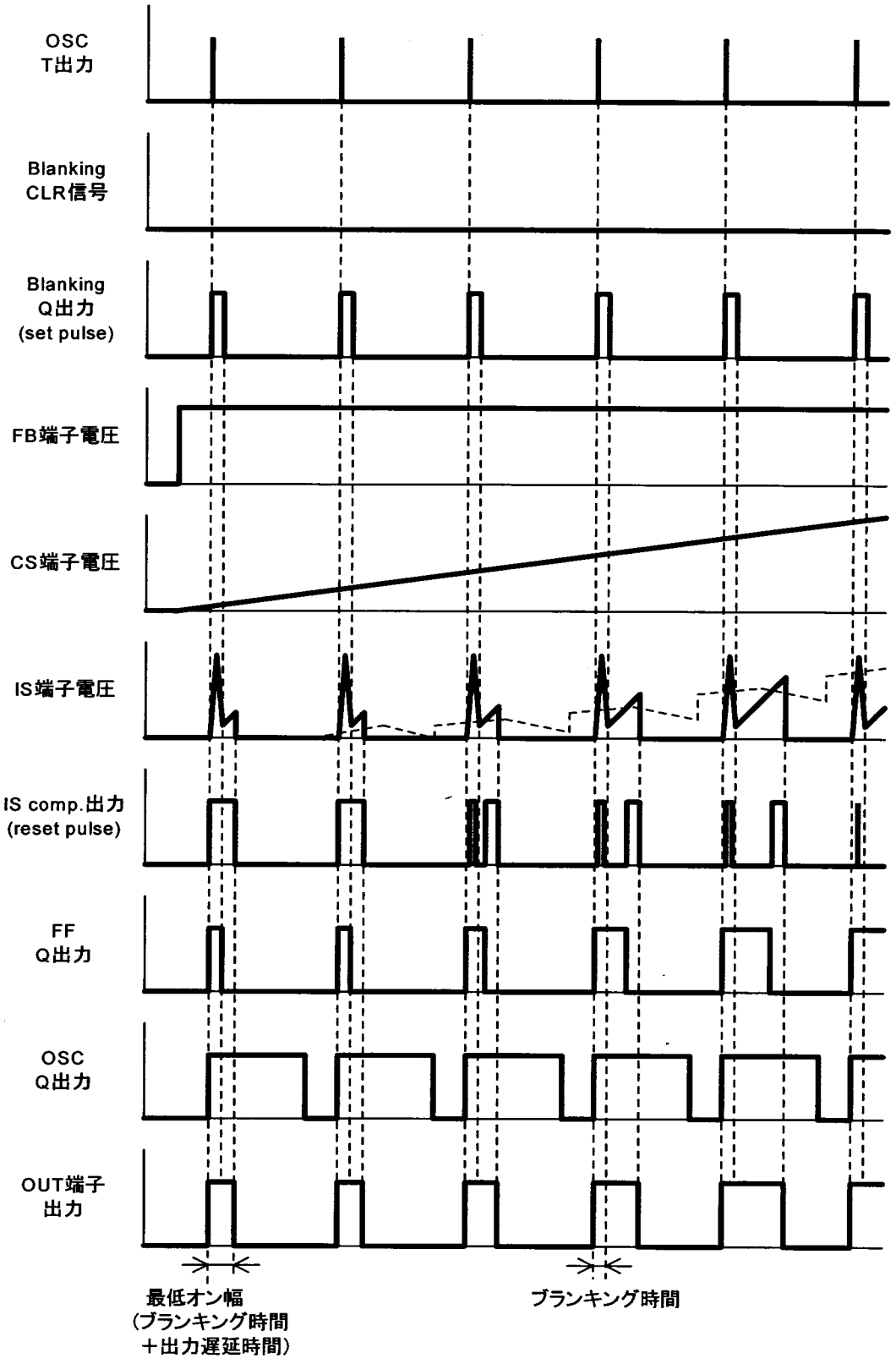


Fig.19 Timing chart at start-up (soft start)

10. Design advice

(1) Start-up and stop

To properly start up and stop the power supply, optimum values shall be set for capacitors connected to the CS pin and VCC pin.

(1-1) At start-up (1)

It takes certain time until the output voltage reaches to the set voltage after the IC has been activated. During this period, FB pin voltage reaches its maximum voltage and the 4V clamp circuit does not operate. As a result, with proper CS pin capacitance and proper start-up, CS pin voltage waveform during start-up will be as shown in **Fig.20**.

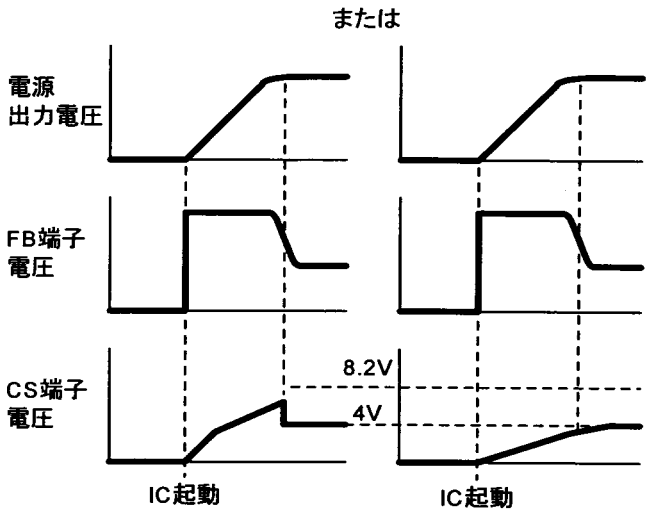


Fig.20 CS pin voltage waveform at start-up (1)
(at normal start)

On the other hand, when CS pin capacitance is too small, CS pin voltage may reach the threshold voltage of the latch mode as shown in **Fig.21** before the output voltage increases to the set value. The IC changes into a latch mode and the power supply cannot start properly. In cases like this, increase CS pin capacitance.

(1-2) At start-up (2)

Fig.22 shows Vcc voltage at start-up when proper capacitance is connected.

When input power is turned on, the Vcc capacitor is charged by the current supplied from the start-up circuit and its voltage increases. Then, when Vcc reaches the ON threshold voltage, the IC starts operation. In normal operation, the IC operates at the voltage supplied from an auxiliary winding. Right after IC's start-up, however, Vcc drops until the auxiliary voltage increases sufficiently. Determine the value of Vcc capacitance so that Vcc does not drop to the OFF threshold voltage.

To be specific, determine the value of Vcc pin capacitance so that the lower limit of Vcc becomes 11V or more.

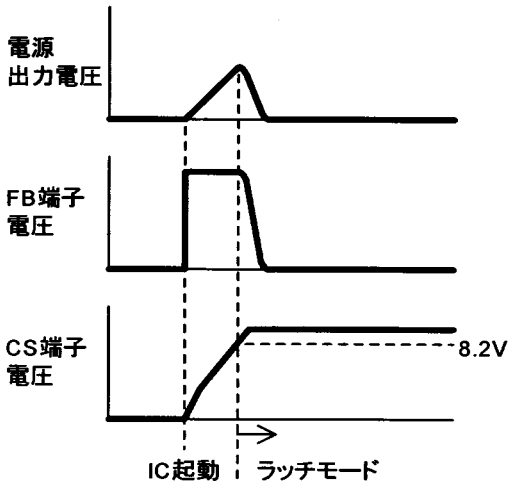


Fig21 CSpin voltage waveform at start-up (2)
(when the power supply cannot start up)

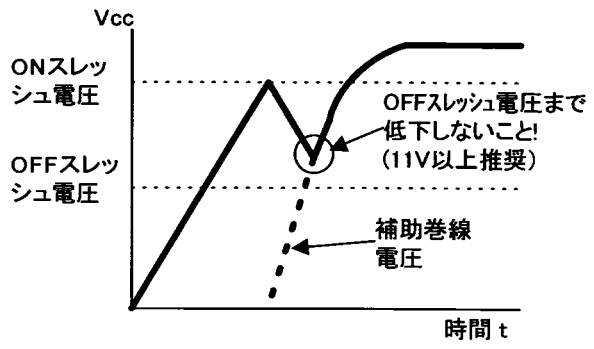


Fig.22 Vcc waveform at start-up (1)
(at normal start-up)

When Vcc capacitance is too small, Vcc drops to the OFF threshold voltage as shown in **Fig.23** before the auxiliary winding voltage increases sufficiently. In this case, Vcc repeatedly goes up and down between the ON and OFF threshold voltages, and the power supply cannot start up.

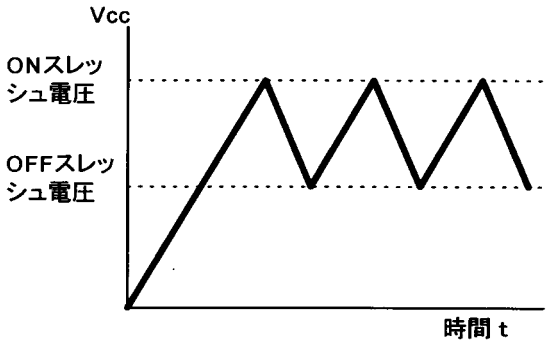


Fig.23 Vcc waveform at start-up (2)
(when the power supply cannot start up)

(1-3) At stopping

When the power supply is turned off by shutdown of input voltage, output voltage remains low for certain period of time before the IC stops operation.

During this period, FB pin voltage increases and the CS pin clamp circuit is cancelled because output voltage remains low. As a result, CS pin voltage increases as shown in **Fig.24**.

CS pin voltage shall not reach the threshold voltage of the latch mode. As shown in **Fig.25**, if CS pin voltage reaches the threshold voltage, the latch mode is held for a period of time until Vcc capacitor voltage drops to OFF threshold voltage. As a result, the power supply cannot be re-started even if input voltage is turned on again.

In such a case, the following measures shall be taken:

- Reduce the time taken until the IC stops operation after the output voltage has dropped through reducing Vcc capacitance.
- Suppress CS pin voltage rise through increasing CS pin capacitance.

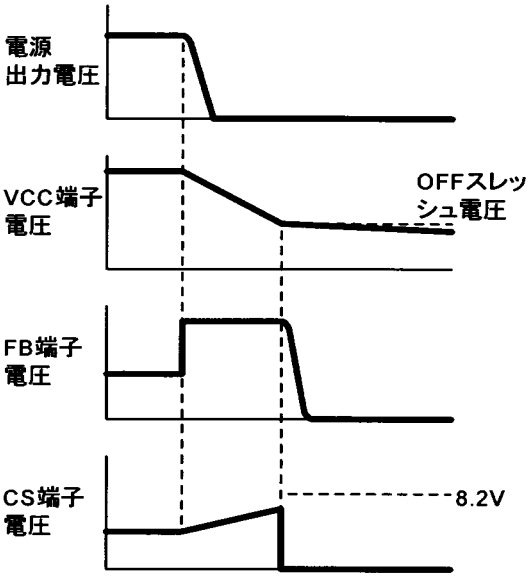


Fig.24 Waveform at stopping (1)

(2) Hold time of Vcc

In some cases, VCC pin capacitance shall be increased to hold Vcc above the OFF threshold voltage at abrupt load change after the power supply has started up.

However, when VCC pin capacitance becomes larger, start-up time gets longer.

In such a case, the circuit shown in **Fig.26** is effective.

Reducing C2 shortens start-up time, and hold time can be kept long because power is supplied via C4 after start-up.

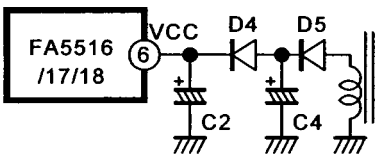


Fig.26 Vcc circuit

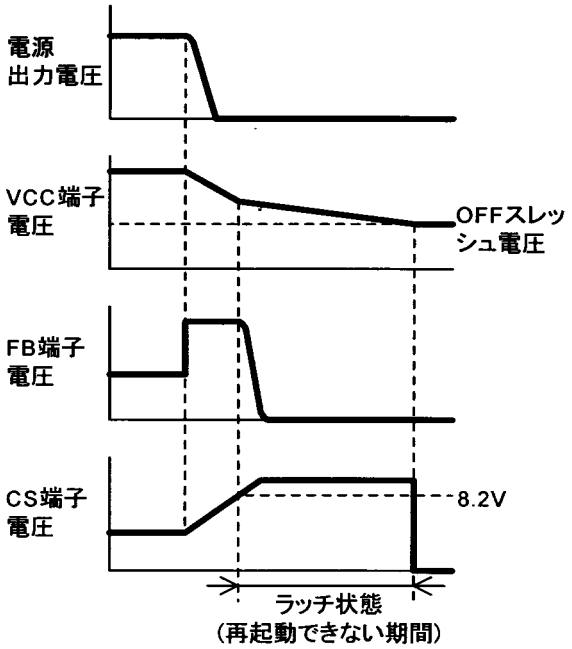


Fig.25 Waveform at stopping (2)

(3) Protection using CS pin

In normal operation, the CS pin voltage is clamped by a 4V zener diode. Externally forcing CS pin voltage to increase to the threshold voltage, 8.2V, for the latch mode allows the IC to stop its operation for protection.

In this case, a current of more than the sink capacity of 4V zener diode, 50μA, shall be applied to the CS pin.

Set the input current to the CS pin at 1mA or less as a guide.

The following shows examples of overvoltage protection at an arbitrary voltage using the CS pin.

(3-1) Overvoltage detection on the secondary side

Fig.27 shows an example of an overload detection circuit on the secondary side to change the IC into the latch mode.

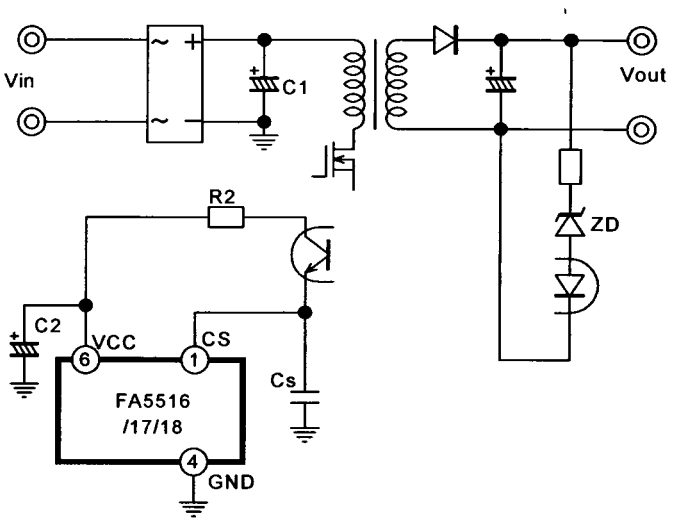


Fig.27 Overvoltage protection (1)

(3-2) Detection of Vcc (1)

Fig.28 shows a circuit where the IC is stopped in the latch mode upon detecting Vcc overvoltage. In this case, Vcc voltage is latched at approximately ZD+8.2V.

Use a ZD whose voltage is larger than the ON threshold voltage of the low-voltage malfunction preventive circuit. Otherwise, the IC cannot start.

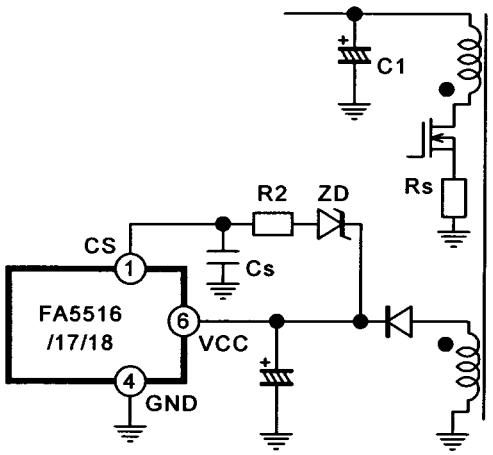


Fig.28 Overvoltage protection (2)

(3-3) Detection of Vcc (2)

Fig.29 shows another circuit to detect Vcc overvoltage. In this case, Vcc voltage is latched approximately at ZD voltage.

Use a ZD whose voltage is larger than the ON threshold voltage of the low-voltage malfunction preventive circuit. Otherwise, the IC cannot start.

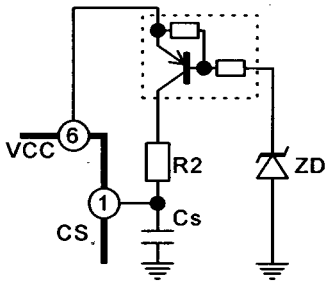


Fig.29 Overvoltage protection (3)

(4) When not using an overload protection function

As shown in **Fig.30**, connect a resistor R3 of 18kΩ between FB pin and GND.

As a result, FB pin voltage does not increase to the threshold voltage for overload protection and the IC does not change to the latch mode even at overload.

In this case, the latch protection for overvoltage is also available.

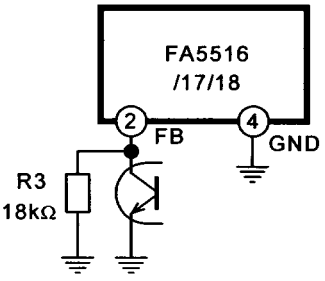


Fig.30 When not using overload protection

(5) Correction of overload detection current

If the power supply output becomes overload, the current of the MOSFETIS is limited by the maximum threshold voltage of the IS pin and power supply voltage drops. If the state continues as it is, an overload protection function operates to stop the IC in the latch mode. For details of an overload protection function, see "9-(8) Overload protection function."

When the overload protection operates, the output current of the power supply varies depending on the input voltage; and the higher the input voltage is, the larger the output current.

In such a case, connect R4 between the current detection resistor Rs and IS pin, and add a correction resistor R5 as shown in **Fig.31**. The typical resistance of R5 is several hundreds of kΩ to several MegΩ. Note that the above correction slightly decreases the value of overload current limit to stop the IC in the latch mode even if input voltage is low.

In addition, be aware that the added resistance R4 affects slope compensation.
(See "10-(6) Slope compensation.")

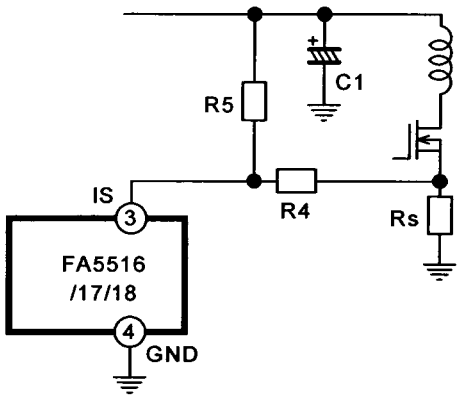


Fig.31 Correction of overload detection current

(6) Slope compensation

As described in "9.-(6) Slope compensation," slope compensation is implemented by adding a ramp signal generated from the oscillator to IS pin voltage using resistors 100kΩ and 2.7kΩ as shown in **Fig.32**. Adding R4 can change the magnitude of slope compensation as shown in **Fig.33**.

Adjusted slope compensation is calculated by the following equation:

$$SLPa = \frac{R7 + R4}{R7} \times SLP$$

Where, SLPa is adjusted slope compensation; SLP slope of compensation initially set in the IC; and R4 resistance between the IS pin and R3

At the same time, the maximum threshold voltage of R3 voltage varies and the maximum threshold voltage after adjustment is calculated by the following equation.

$$VthIS1a = \left(1 + \frac{R4}{R6 + R7}\right) \times VthIS1$$

Where, Vthis 1a is the maximum threshold voltage after adjustment.

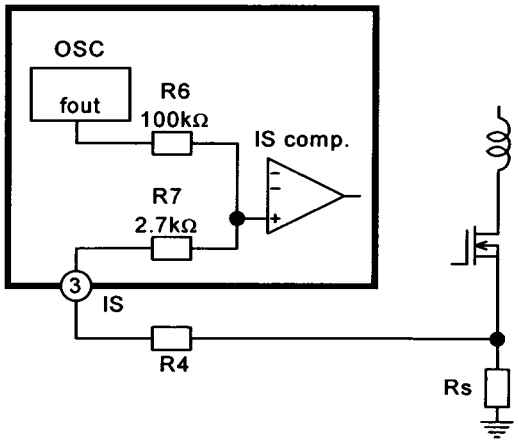


Fig.32 Adjustment of slope compensation

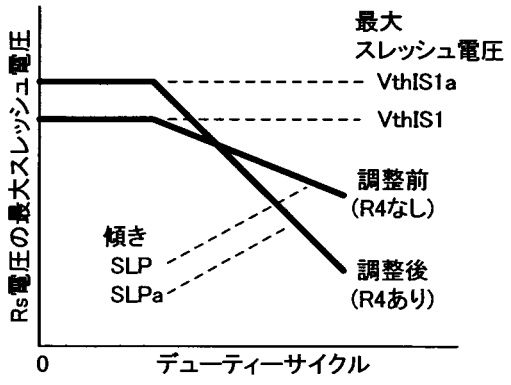


Fig.33 Maximum threshold voltage after adjustment

(7) Improvement of input power at light load

This IC is provided with a function to lower switching frequency at light load in order to reduce power dissipation. However, depending on the circuit used, switching frequency cannot be sufficiently reduced, leading to insufficient reduction of power dissipation at light load.

In such a case, connect R6 between the auxiliary winding and the IS pin as shown in **Fig.34**. When R4 is 1kΩ, R6 is several hundreds of kΩ to 1MegΩ. The smaller the R6 is, the lower the switching frequency at light load.

However, negative voltage is applied to the IS pin due to R6 for some time while MOSFET is ON. Be aware that the negative voltage shall not be lower than absolute maximum rating, -0.3V.

In addition, when switching frequency is set too low at light load, transformer or other apparatus may produce noise.

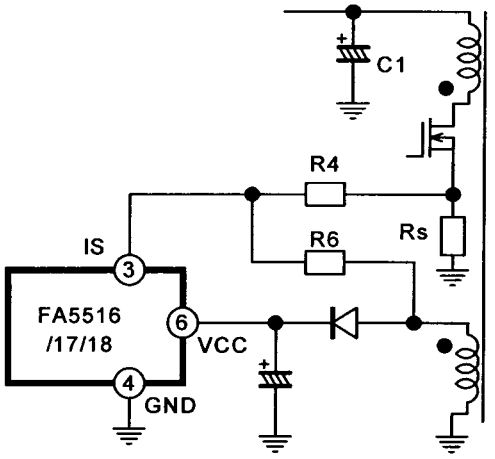


Fig34 Input power improvement circuit at light load

(8) Prevention of malfunction caused by noise

This IC is an analog IC, and noise applied to anyone of the pins may cause malfunction. If malfunction is detected, use the IC through referring to the following description and fully checking a power supply unit.

In addition, arrange the capacitors connected to pins as close to the IC as possible and take great care of wiring, for effective noise suppression.

(8-1) FB pin

The FB pin sets the threshold voltage of the current comparator. Any noise applied to the FB pin may disturb output pulses. Usually the capacitor C5 is connected as shown in **Fig.35** to suppress noise.

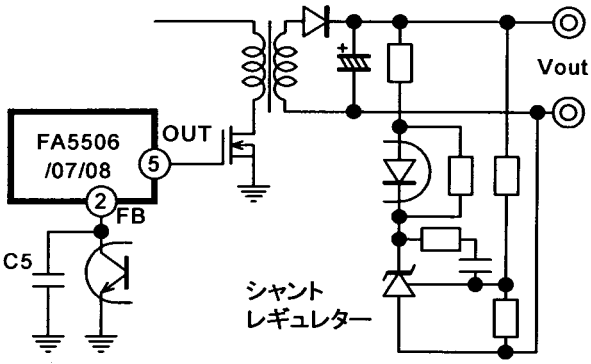


Fig.35 Prevention of malfunction caused by noise (FB pin)

(8-2) IS pin

As described in "9.-(4) Blanking," this IC has a blanking function, and malfunction caused by a surge current produced at turn-on of the MOSFET is hard to occur.

A malfunction, however, may occur when a surge current is excessively large or when any noise is externally applied at other than turn-off.

In such a case, add a CR filter to the IS pin as shown in **Fig.36**.

Choose a CR filter with resistance as small as possible (preferably 100Ω or less) because the value of resistance affects the magnitude of slope.

(See "10.-(6) Slope compensation.")

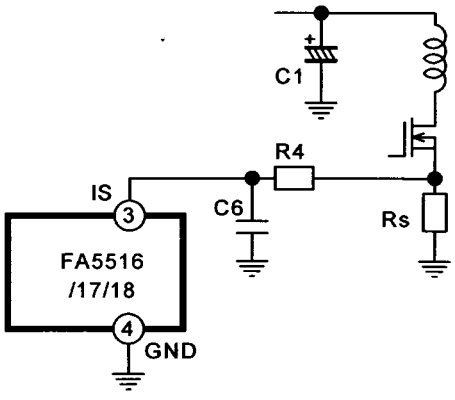


Fig36 Prevention of malfunction caused by noise (IS pin)

(8-3) VCC pin

Relatively large noise may occur at the VCC pin because a large current flows from the VCC pin at the instant of driving the MOSFET. If noise is excessively large, a malfunction may occur of the IC. Pay full attention to capacitance and characteristics of the capacitor between the VCC pin and GND to reduce noise as much as possible.

(9) Prevention of malfunction caused by negative voltage applied to pins

When a large negative voltage is applied to a pin, a parasitic element in the IC may operate and cause a malfunction. Be sure that voltage applied to a pin shall not be -0.3V or less.

Voltage oscillation generated at turn-off of the MOSFET may be applied to the OUT pin via the parasitic capacitance of the MOSFET, resulting in the negative voltage applied to the OUT pin.

In such a case, connect a Shottky diode between each pin and GND. Forward voltage of the Shottky diode can suppress negative voltage at each pin. Use a Shottky diode with low forward voltage.

Fig.37 shows an example of a circuit with a Shottky diode connected to the OUT pin.

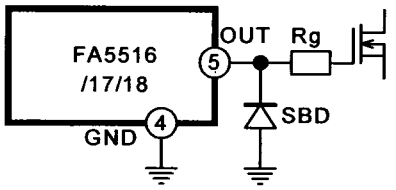


Fig.37 Negative voltage prevention circuit

(10) Gate circuit configuration

A resistor is generally inserted between the gate terminal of the MOSFET and the OUT pin of the IC for adjustment of switching speed, suppression of voltage oscillation at the gate terminal and other purposes.

Sometimes, the drive currents for turning-on and -off must independently determined.

In such a case, connect the gate terminal of the MOSFET and OUT pin of the IC as shown in **Fig.38** or **Fig.39**.

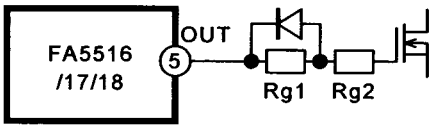


Fig.38 Gate circuit (1)

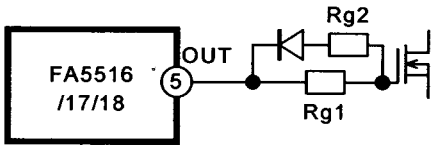


Fig.39 Gate circuit (2)

In **Fig.38**, the driving current is limited by Rg1+Rg2 at turn-on and by only Rg2 at turn-off

In **Fig.39**, the driving current is limited by only RG1 at turn-on and by parallel-connected Rg1 and Rg2 at turn-off.

(11) Loss calculation

IC loss shall be determined to use the IC within its rating. Since it is hard to directly measure IC loss, an example of calculating approximate IC loss is given below.

Total IC loss, Pd, is obtained by the following equation:

$$Pd \fallingdotseq Vcc \times (Iccop1 + Qg \times fsw) + V_{VH} \times IHrun$$

Where Vcc is the supply voltage to the IC, Iccop1 is consumption current of the IC, Qg is total gate charge of the MOSFET, fsw is switching frequency, V_{VH} is VH pin voltage and IHrun is a current flowing into the VH pin when the IC operates.

This equation gives an approximate value of Pd, which is normally a little greater than the actual loss. Take into consideration variation and temperature characteristics of each value

(Example)

When the VH pin is connected to half-wave rectification waveform at power supply of AC100V, average VH pin voltage is approximately 45V.

Under this condition, let us suppose Vcc=18V and Qg=80nC at Tj=25°C.

When using FA5518, according to the specifications IHrun = 20μA(typ.), Iccop1 = 1.2mA(typ.) and fsw = 60kHz(typ.).

Thus, typical IC loss Pd:

$$Pd \fallingdotseq 18V \times (1.2mA + 80nC \times 60kHz) + 45V \times 20\mu A$$
$$\fallingdotseq 109mW$$

(Reference)
Subharmonic oscillation and slope compensation

In a peak-value-control current mode, when the converter operates in an inductor-current continuous mode and at duty cycle of 50% or more, the current may oscillate at an integral multiple of switching frequency. This oscillation is called subharmonic oscillation.

Fig. 40 shows an example of inductor current waveform when a subharmonic oscillation occurs.

It is found that ON and OFF periods vary while the peak value of an inductor current, switching cycle and current slopes during ON and OFF periods remain unchanged.

The harmonic oscillation may increase ripple voltage contained in the output voltage or cause an unusual noise.

The subharmonic oscillation can be prevented by giving a certain gradient to the threshold of the peak current as shown in **Fig. 41**. This is called slope compensation.

Generally, the gradient of slope compensation required for preventing a subharmonic oscillation is given by the following relational expression:

$$Kc > \frac{Ld - Lu}{2}$$

Where

Lu : Gradient of an inductor current during the ON period

Ld : Gradient of an inductor current during the OFF period

Kc : Gradient of slope compensation

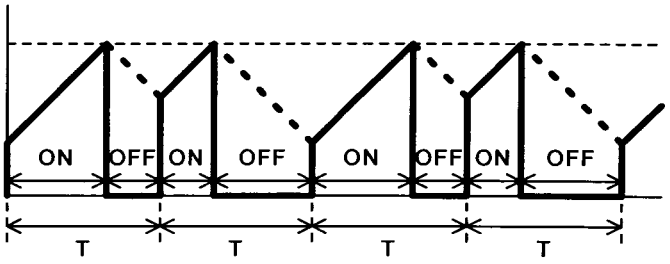


Fig.40 Inductor current without slope compensation

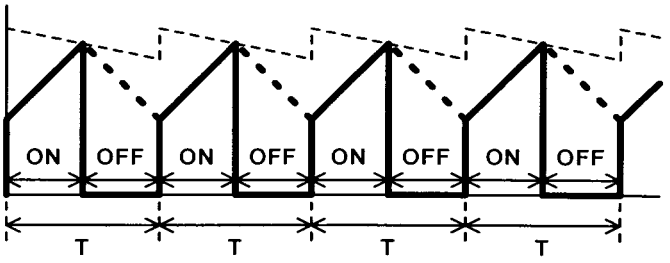


Fig.41 Inductor current with slope compensation

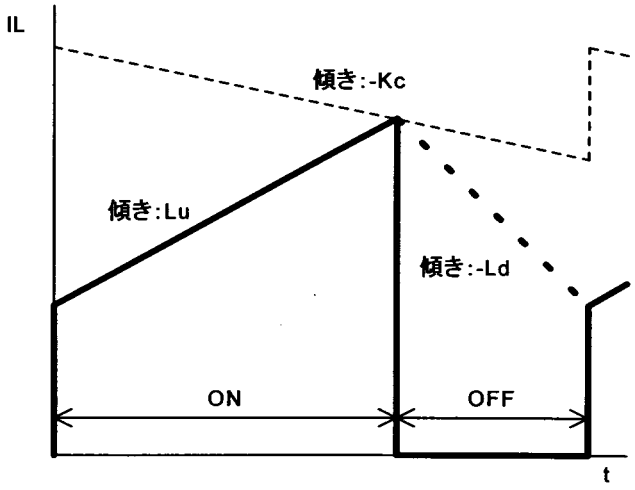
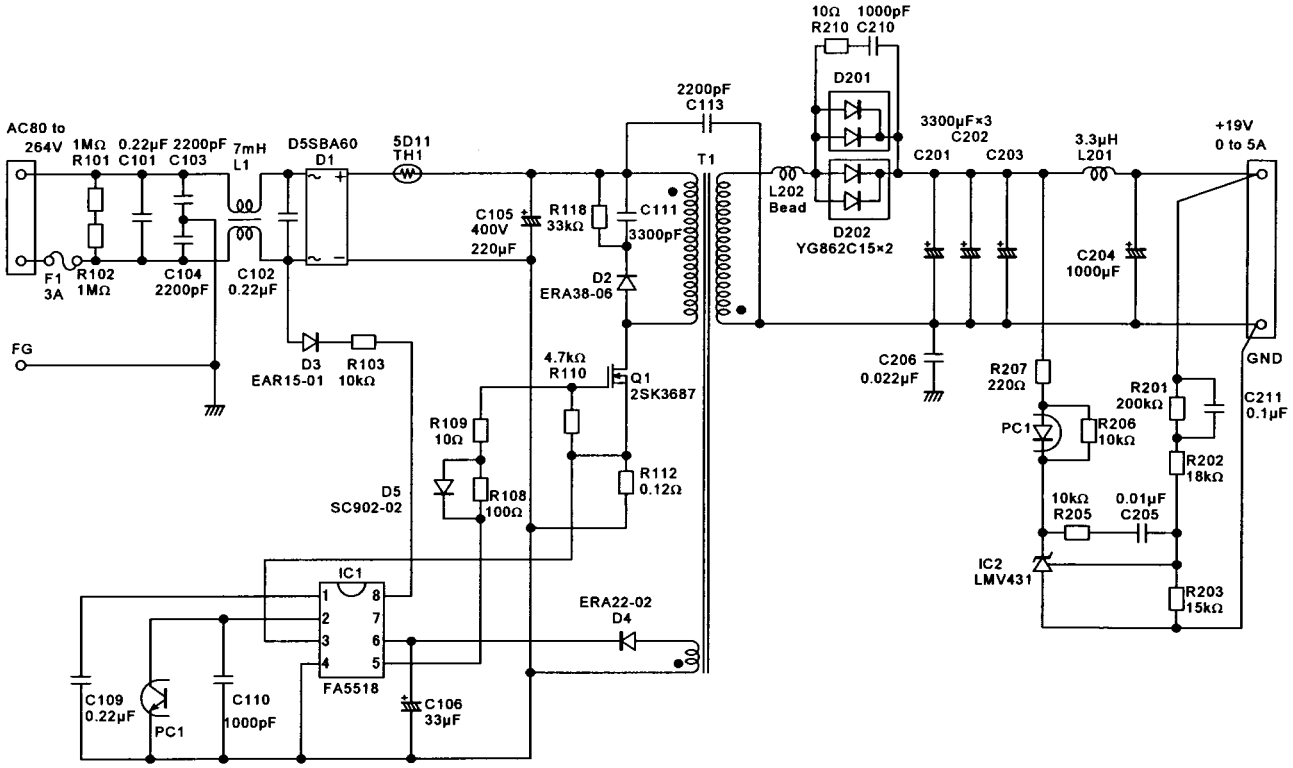


Fig.42 Inductor current without slope compensation

11. Example of an application circuit



Note

The example of an application circuit is intended to be used only for reference and not to guarantee performance or characteristics.