KMB054N40DA

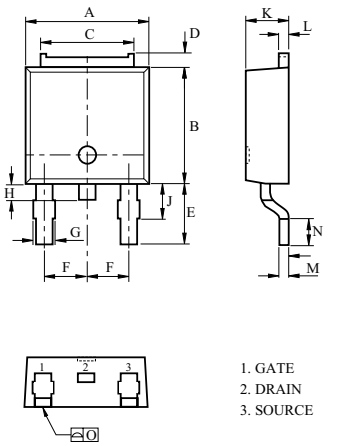
N-Ch Trench MOSFET

General Description

This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for Back-light Inverter and Power Supply.

FEATURES

- V_{DSS}=40V, I_D=54A.
- Low Drain-Source ON Resistance.
  : $R_{DS(ON)}$=8.5mΩ(Max.) @ V_{GS}=10V
  : $R_{DS(ON)}$=11mΩ(Max.) @ V_{GS}=4.5V
- Super High Dense Cell Design.
- High Power and Current Handling Capability.



DIM	MILLIMETERS
A	6.60 ± 0.20
B	6.10 ± 0.20
C	5.34 ± 0.30
D	0.70 ± 0.20
E	2.70 ± 0.15
F	2.30 ± 0.10
G	0.96 MAX
H	0.90 MAX
J	1.80 ± 0.20
K	2.30 ± 0.10
L	0.50 ± 0.10
M	0.50 ± 0.10
N	0.70 MIN
O	0.1 MAX

1. GATE
2. DRAIN
3. SOURCE

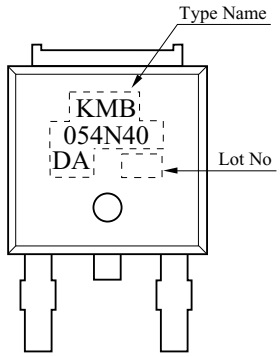
DPAK (1)

MAXIMUM RATING (Ta=25℃ Unless otherwise Noted)

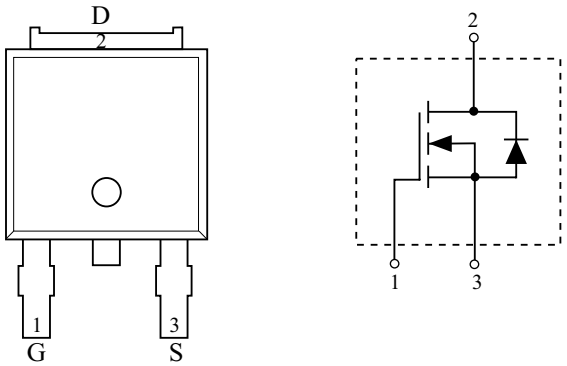
CHARACTERISTIC		SYMBOL	N-Ch	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	DC@T_C=25℃ (Note1)	I_D	54	A
	Pulsed (Note2)	I_{DP}	100	
Drain-Source-Diode Forward Current		I_S	100	A
Drain Power Dissipation	@T_C=25℃ (Note1)	P_D	45	W
	@Ta=25℃ (Note2)		3.1	
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55 150	℃
Thermal Resistance, Junction to Case (Note1)		R_{thJC}	2.8	℃/W
Thermal Resistance, Junction to Ambient (Note2)		R_{thJA}	40	℃/W

Note 1) R_{thJC} means that the infinite heat sink is mounted.
Note 2) Surface Mounted on 1 ×1 Pad of 2 oz copper.

Marking



PIN CONNECTION (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250 μA	40	-	-	V
Drain Cut-off Current		I_{DSS}	V_{GS}=0V, V_{DS}=32V	-	-	1	μA
Gate Leakage Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage		V_{th}	V_{DS}=V_{GS}, I_D=250 μA	1	1.9	3	V
Drain-Source ON Resistance		$R_{DS(ON)}$*	V_{GS}=10V, I_D=14A	-	7	8.5	mΩ
			V_{GS}=4.5V, I_D=11A	-	8.5	11	
			V_{GS}=10V, I_D=14A, T_j=125℃	-	10.4	14	
Forward Transconductance		g_{fs}*	V_{DS}=10V, I_D=20A	-	58	-	S
Dynamic							
Input Capacitance		C_{iss}	V_{DS}=20V, f=1MHz, V_{GS}=0V	-	2340	-	pF
Ouput Capacitance		C_{oss}		-	420	-	
Reverse Transfer Capacitance		C_{rss}		-	250	-	
Total Gate Charge	V_{GS}=10V	Q_g*	V_{DS}=20V, V_{GS}=10V, I_D=14A	-	50	-	nC
	V_{GS}=5V	Q_g*		-	30	-	
Gate-Source Charge		Q_{gs}*		-	8	-	
Gate-Drain Charge		Q_{gd}*		-	13	-	
Turn-On Delay Time		$t_{d(on)}$*	V_{DD}=20V, V_{GS}=10V, I_D=1A, R_G=6Ω	-	15	-	ns
Turn-On Rise Time		t_r*		-	20	-	
Turn-Off Delay Time		$t_{d(off)}$*		-	90	-	
Turn-Off Fall Time		t_f*		-	25	-	
Source-Drain Diode Ratings							
Source-Drain Forward Voltage		V_{SDF}*	V_{GS}=0V, I_S=14A	-	0.8	1.2	V
Note>* Pulse Test : Pulse width <300μs , Duty cycle < 2%							

Fig1. I_D - V_{DS}

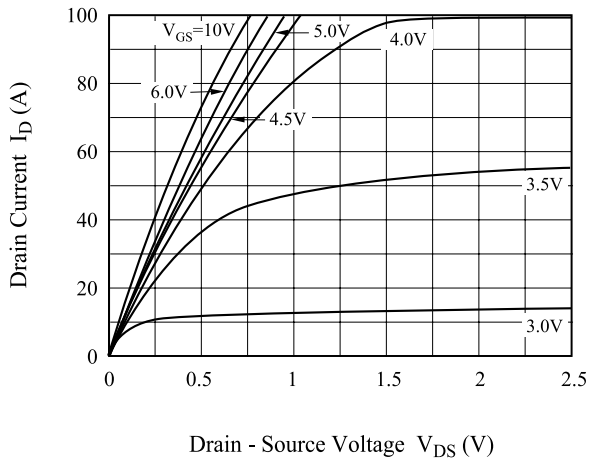


Fig2. $R_{DS(ON)}$-I_D

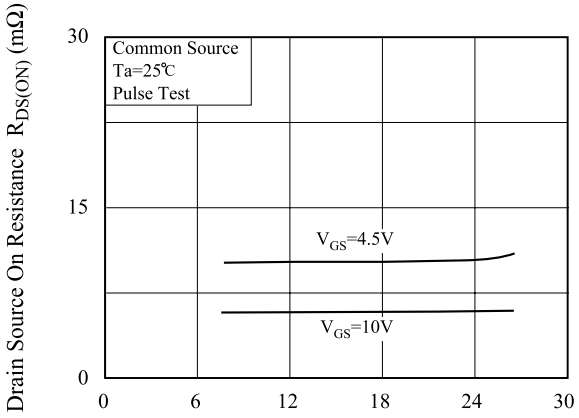


Fig3. I_D - V_{GS}

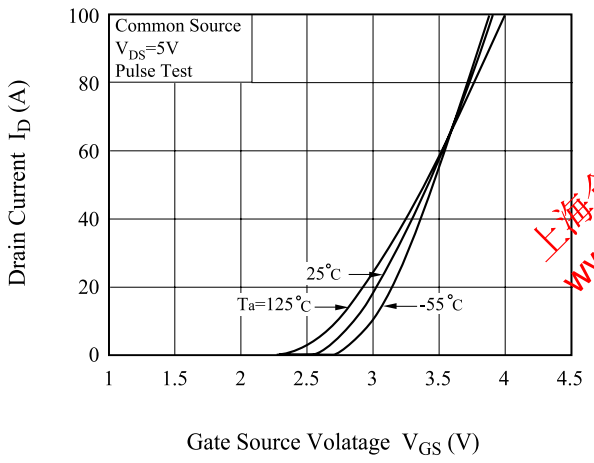


Fig4. $R_{DS(on)}$ - T_j

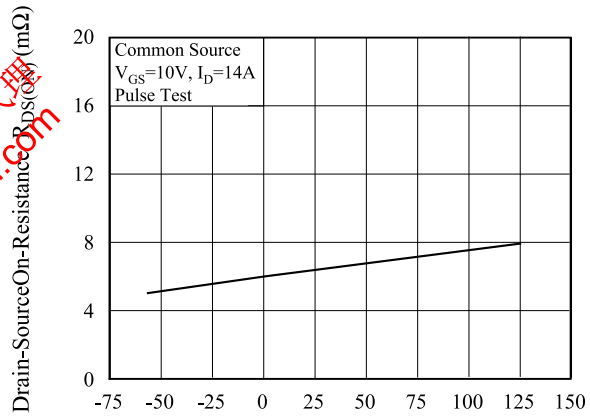


Fig5. V_{th} - T_j

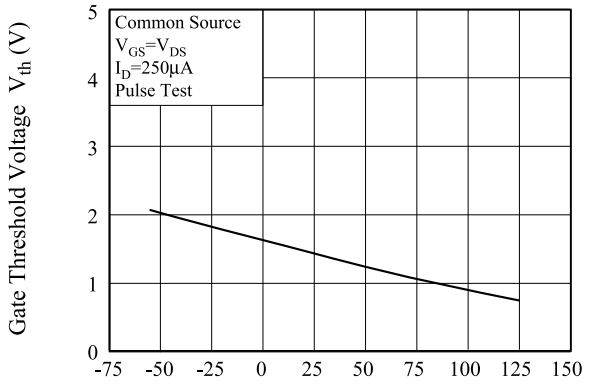


Fig6. I_S - V_{SDF}

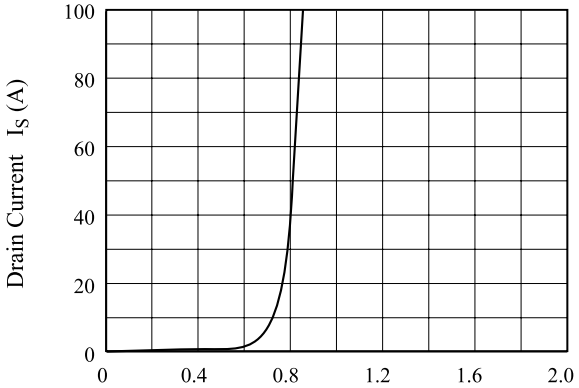


Fig 7. V_{GS} - Q_g

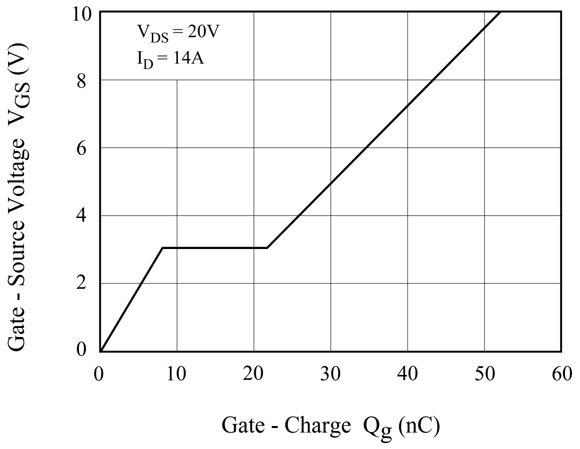


Fig 8. C - V_{DS}

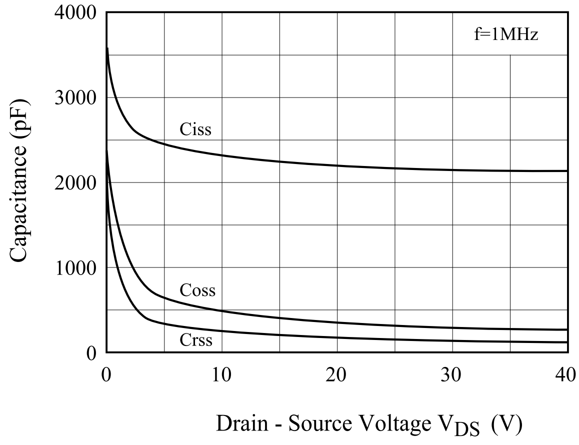


Fig9. Safe Operation Area

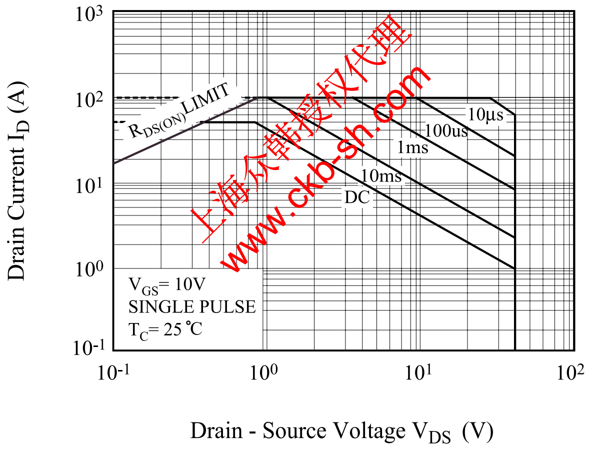


Fig10. Transient Thermal Response Curve

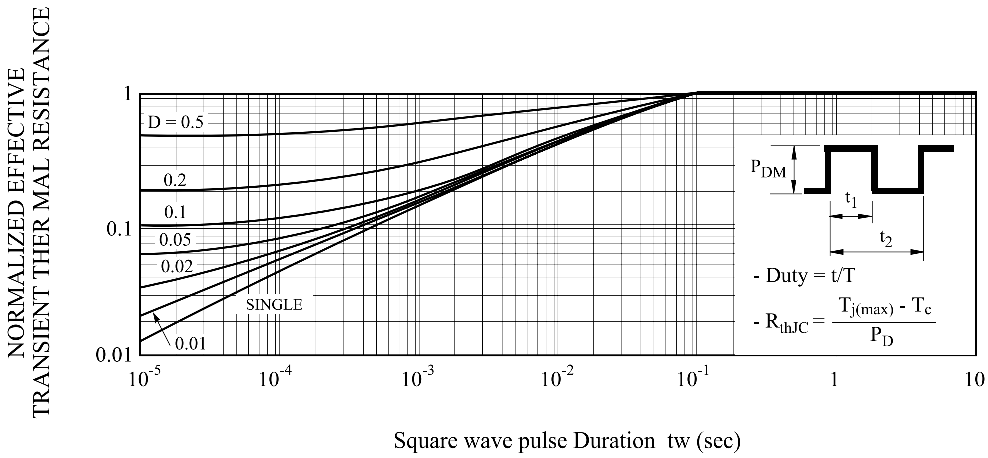


Fig11. Gate Charge Circuit and Wave Form

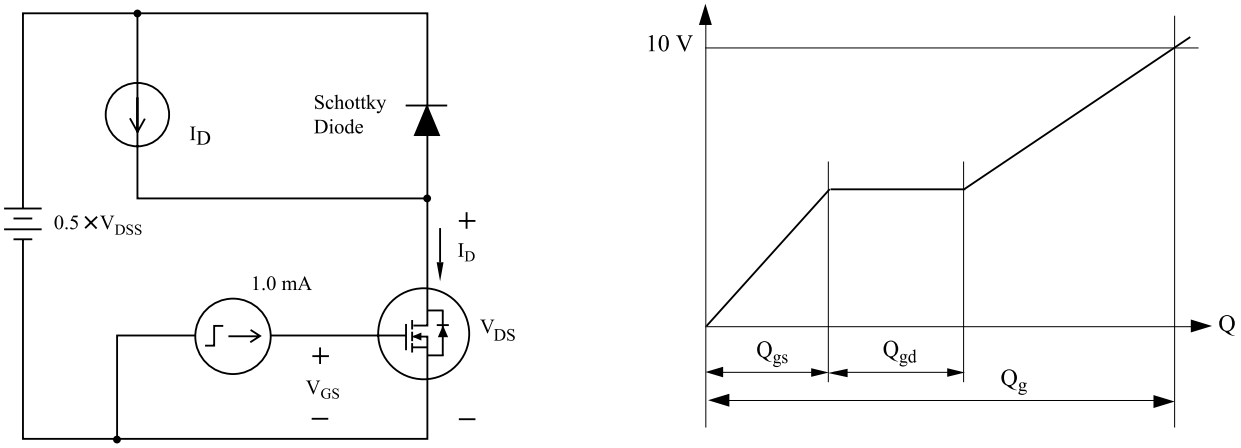


Fig12. Resistive Load Switching