SONY

AC-DC Controller

CXA3809M

Description

The CXA3809M has optimum configuration to realize various power supply circuits easily and compactly by including Power-factor correction, resonant controller and various protection function in one package. (Applications: Power supply circuit, etc.)

Features

- ◆ Power-factor correction
  - Multiplierless critical conduction mode (CRM) control
  - Supports W/W input
  - Restart timer
  - Maximum frequency limit (during overcurrent detection)
  - Continuous overcurrent detection protection function
- ◆ Resonant controller
  - Timer-latch over current protection
  - Soft start function
  - Adjustment minimum frequency limit
  - Pulse over current load detection
  - Out of resonance prevention function at start-up
- ◆ Common
  - Adjacent 2-pin short protection
  - Various protection functions including overvoltage and overcurrent
  - AC off detection
  - PFC-OK signal output

Structure

BiCMOS silicon monolithic IC

Package

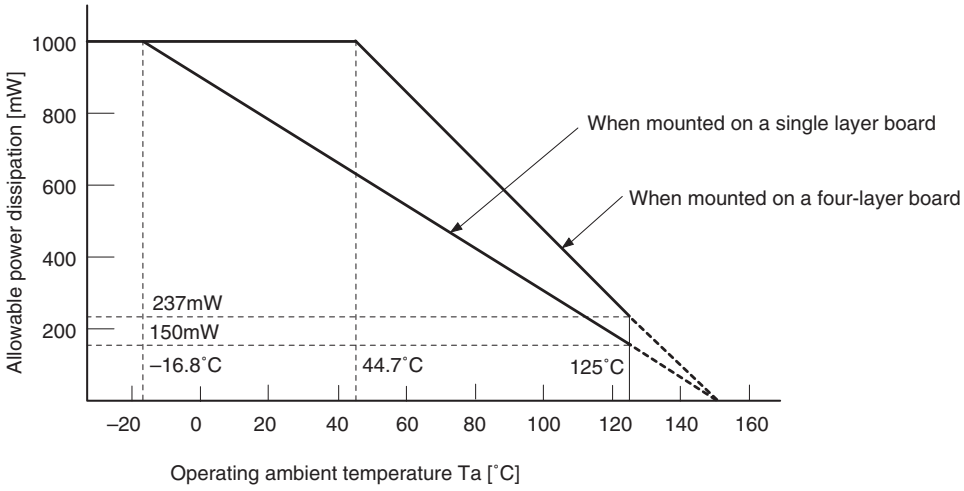
24-pin SOP

E09504

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Maximum supply voltage	VCC	24.0	V	VCC
VCC pin voltage	VCCIN	–0.3 to VCC + 0.3	V	AC_DETIN, AC_DETOUT, AC_VRMS, PFC_OK, MODE
Driver output pin voltage	VOUT	–0.3 to VCC + 0.3	V	PFC_OUT, RM_OUTP, RM_OUTN
Power supply pin voltage for internal circuit	VREF	–0.3 to +7.0	V	VREF
VREF pin voltage	VREFIN	–0.3 to +7.0	V	PFC_OVP, PFC_CS, PFC_VAO, PFC_TONMAX, PFC_VSENSE, RM_OFFADJ, RM_RT, RM_SS, RM_CS, RM_CSGND, RM_FMIN
ZCD current	I_{ZCD}	±7	mA	PFC_ZCD
Allowable power dissipation	P_D	*1	mW	(See the thermal derating curve.)
Operating ambient temperature range	Topt	–30 to +125	˚C	
Junction temperature	Tjmax	+150	˚C	
Storage temperature	Tstg	–55 to +150	˚C	

*1 Allowable power dissipation reduction characteristics

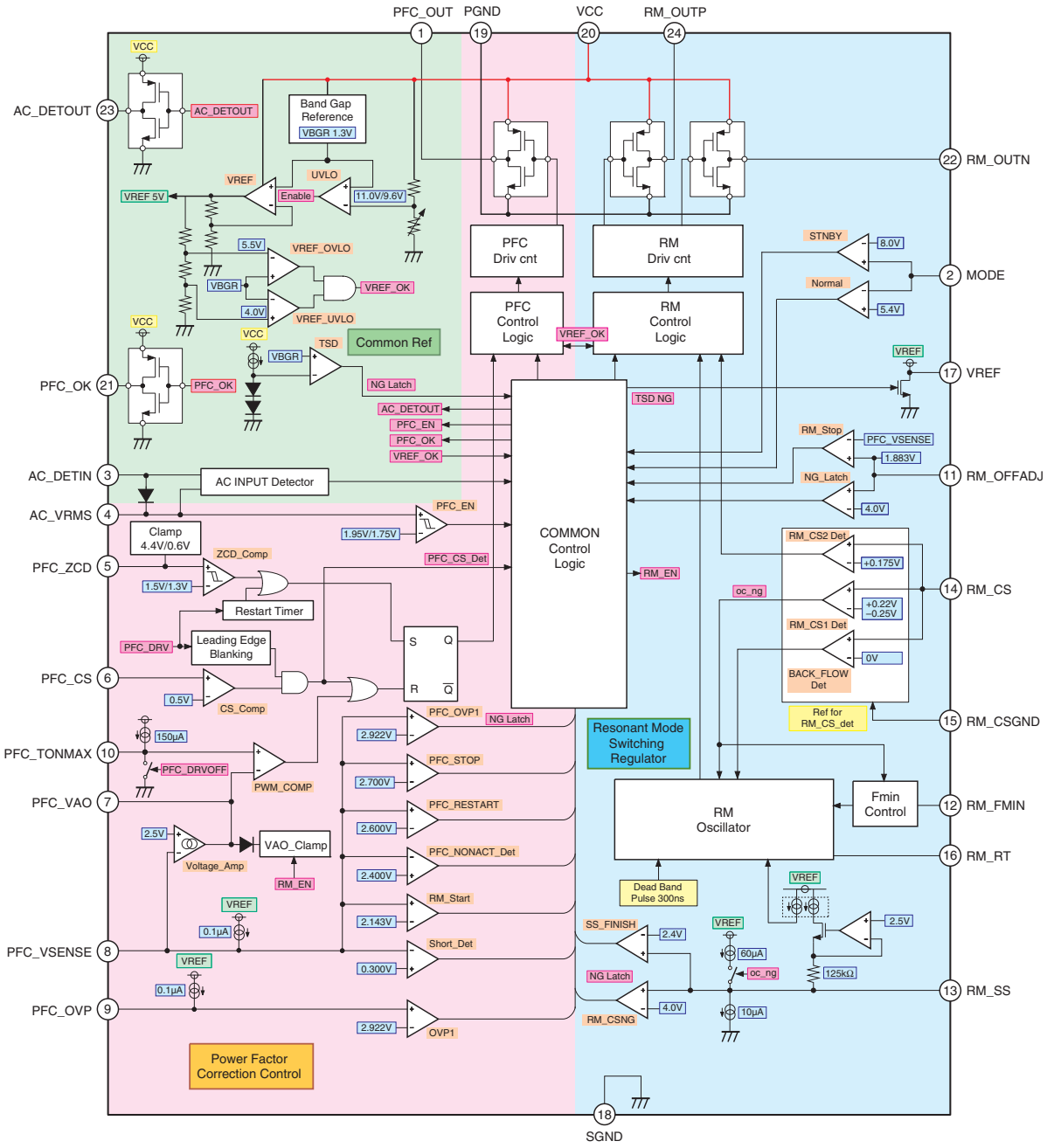


Glass fabric base epoxy board, 76mm × 114mm, t = 1.6mm

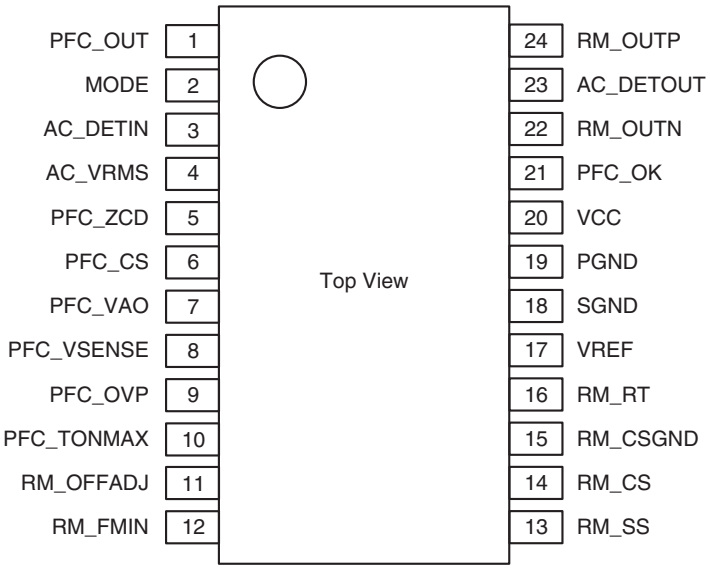
Recommended Operating Conditions

Item	Symbol	Rating	Unit	Remarks
Supply voltage (VCC system)	VCC	12.0 to 18.0	V	
Operating ambient temperature range	Topt	–25 to +85	˚C	
Junction temperature	Tj	–25 to +125	˚C	

Block Diagram



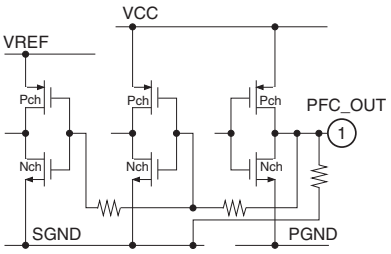
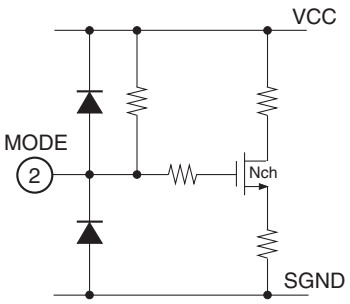
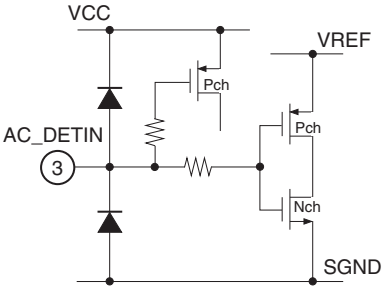
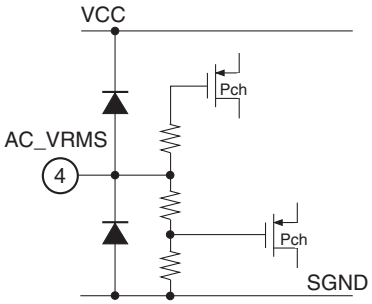
Pin Configuration

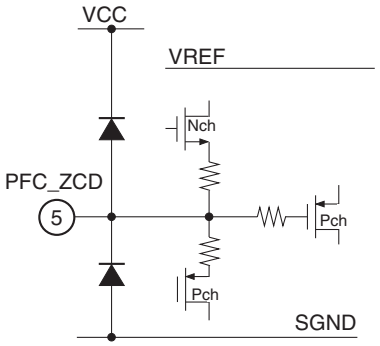
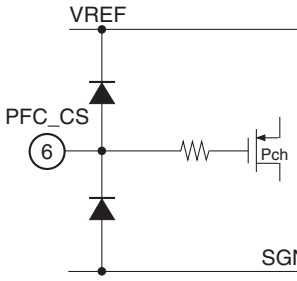
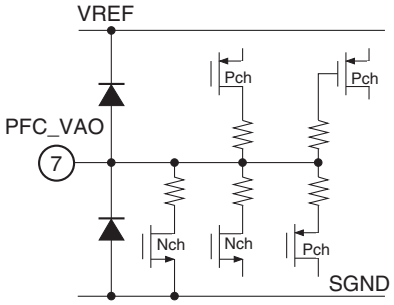
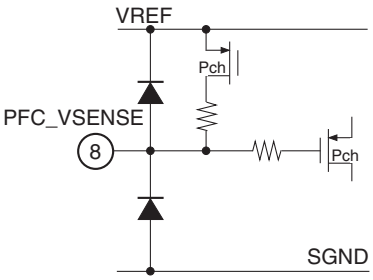
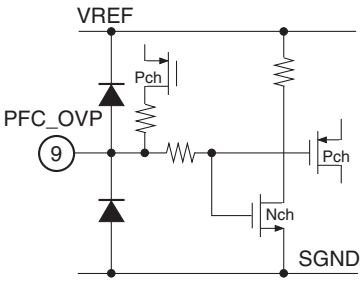


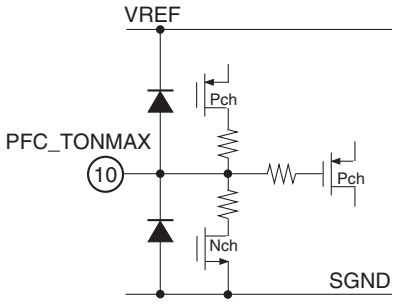
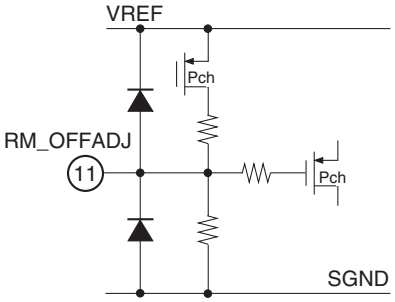
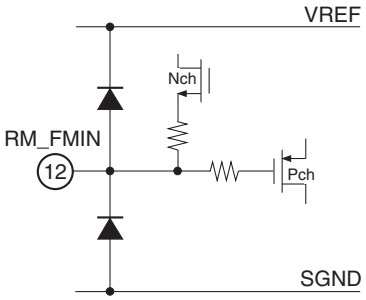
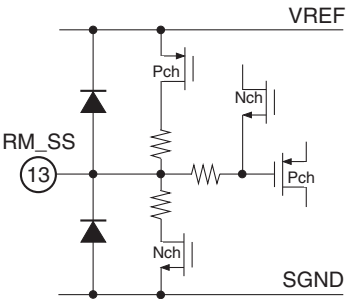
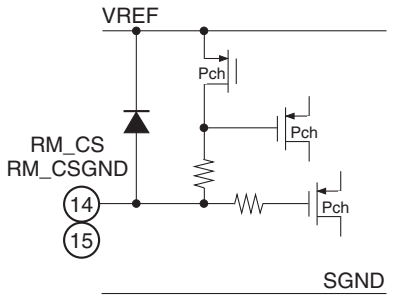
Pin Table

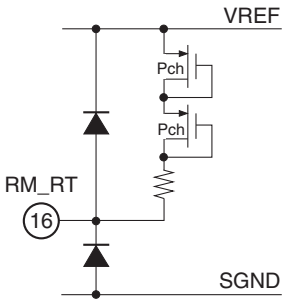
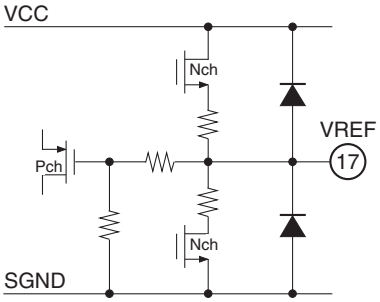
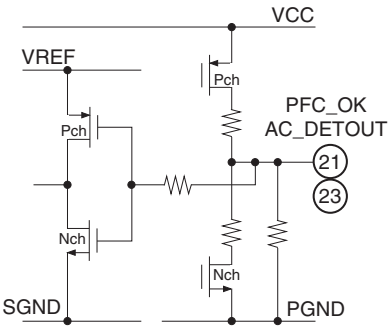
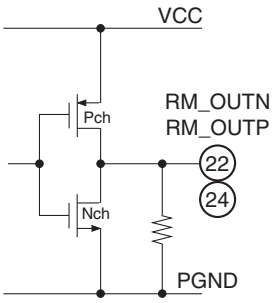
Pin No.	Pin name	Description	Connection end of protective element
1	PFC_OUT	PFC MOSFET gate driver output	—
2	MODE	Mode determination	VCC, SGND
3	AC_DETIN	AC voltage sense input	VCC, SGND
4	AC_VRMS	AC peak voltage sense and PFC enable	VCC, SGND
5	PFC_ZCD	PFC zero current detect input	VCC, SGND
6	PFC_CS	PFC current sense input	VREF, SGND
7	PFC_VAO	PFC voltage control error amplifier output	VREF, SGND
8	PFC_VSENSE	PFC output voltage sense input	VREF, SGND
9	PFC_OVP	PFC output overvoltage sense input	VREF, SGND
10	PFC_TONMAX	PFC maximum ON time control	VREF, SGND
11	RM_OFFADJ	Resonant controller stop voltage adjustment and abnormal latch input	VREF, SGND
12	RM_FMIN	Resonant controller minimum frequency setting	VREF, SGND
13	RM_SS	Resonant controller soft start and overcurrent timer-latch setting	VREF, SGND
14	RM_CS	Resonant controller current sense input	VREF
15	RM_CSGND	Resonant controller current sense ground	VREF
16	RM_RT	Resonant controller frequency control	VREF, SGND
17	VREF	Internal supply voltage	VCC, SGND
18	SGND	Signal ground	(PGND)
19	PGND	PFC, RM driver ground	(SGND)
20	VCC	Power supply input	SGND
21	PFC_OK	PFC-OK signal output	—
22	RM_OUTN	Resonant controller Low-side MOSFET driver output	—
23	AC_DETOUT	AC off detect signal output	—
24	RM_OUTP	Resonant controller High-side MOSFET driver output	—

Pin Description

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
1	PFC_OUT	O	VCC to GND		PFC MOSFET gate driver output (Connect to the NMOS gate for PFC)
2	MODE	I	VCC to GND		Mode select input (GND connection: Normal sequence VCC connection: Standby mode)
3	AC_DETIN	I	VCC to GND		AC voltage input (Connect to AC input detection resistor)
4	AC_VRMS	I/O	(VCC – 2.0V) to GND		AC peak voltage sense and PFC enable (Connect to peak voltage hold capacitor)

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
5	PFC_ZCD	I	4.4V to 0.6V		PFC zero current detect input (Connect to boost inductor of auxiliary winding)
6	PFC_CS	I	VREF to GND		PFC current sense input (Connect to the detection side of current sense resistor)
7	PFC_VAO	O	3.2V to GND		PFC voltage control error amplifier output (Connect a phase compensation circuit: between PFC_VAO and GND)
8	PFC_VSENSE	I	VREF to GND During steady-state: 2.5V		PFC output voltage sense input (Connect to PFC output detection resistor)
9	PFC_OVP	I	VREF to GND During steady-state: 2.5V		PFC output overvoltage sense input (Connect to PFC output detection resistor)

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
10	PFC_TONMAX	I/O	3.2V to GND		PFC maximum ON time control (Connect to ON time control capacitor)
11	RM_OFFADJ	I/O	VREF to GND		Resonant controller stop voltage adjustment and abnormal latch input
12	RM_FMIN	I	1.2V		Resonant controller minimum frequency setting (Connect to minimum frequency control resistor)
13	RM_SS	I/O	VREF to GND During steady-state: 2.5V		Resonant controller soft start and overcurrent timer-latch setting (Connect to the capacitor for soft start)
14	RM_CS	I	VREF to – 0.3V		Resonant controller current sense input (Connect to the resistor for current detection)
15	RM_CSGND				Resonant controller current sense ground (Connect to the resistor for current detection)

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
16	RM_RT	I	(3.5V)		Resonant controller frequency control (Connect to the photo coupler for output feedback)
17	VREF	O	5.0V		Internal supply voltage output (Connect to the capacitor for stabilization)
18	SGND	—	—	—	Signal ground
19	PGND	—	—	—	Driver ground
20	VCC	—	—	—	Power supply input
21	PFC_OK	O	VCC to GND		PFC-OK signal output
23	AC_DETOUT				AC off detect signal output
22	RM_OUTN	O	VCC to GND		Resonant controller Low-side MOSFET driver output (Connect to the drive transformer)
24	RM_OUTP				Resonant controller High-side MOSFET driver output (Connect to the drive transformer)

Electrical Characteristics

◆ Shared Blocks

(Unless otherwise specified, the conditions are Ta = 27℃, VCC = 12V, MODE = GND)

1. Current Consumption (VCC and PVCC pins)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption in standby mode	Istb	MODE = VCC	—	700	1000	μA
Operating current consumption	Iact	AC_DETIN = 1.0V, PFC_VSENSE = 1.0V * No Switching	—	3.0	3.5	mA

2. Under Voltage Lock Out Circuit Block (VCC pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Turn-on voltage	Vact		10.2	11.0	11.8	V
Turn-off voltage	Voff		9.0	9.6	10.2	V
Hysteresis	Vact-Voff	Vact – Voff	1.1	1.4	1.7	V

3. Reference Voltage Output Circuit Block (VREF pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output voltage	Vvref		4.85	5.00	5.15	V
Input stability	Vline	VCC = 10.5V to 18V	—	10	30	mV
Load stability	Vload	Iload = 0.1m to 5mA	—	20	50	mV
Pin voltage when NG latch (When TSD)	Vvrefng	Iout = 10mA (Design guarantee)	—	0.1	0.5	V

4. AC Input Detection Circuit Block (AC_DETIN pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
PFC operation start and stop voltage	Vpfcon	AC_DETIN peak voltage (rise)	1.85	1.95	2.05	V
	Vpfcoff	AC_DETIN peak voltage (fall)	1.65	1.75	1.85	V
Hysteresis	Vpfchys	Vpfcok – Vpfcoff	0.17	0.20	0.23	V
AC detection reference voltage High 1	Vthach1	AC_VRMS = 7.5V	4.675	4.875	5.075	V
AC detection reference voltage Low 1	Vthacl1	AC_VRMS = 7.5V	3.175	3.375	3.575	V
AC detection reference voltage High 2	Vthach2	AC_VRMS = 2.0V	1.1	1.3	1.5	V
AC detection reference voltage Low 2	Vthacl2	AC_VRMS = 2.0V	0.7	0.9	1.1	V
AC off detection delay time 1	Tdlyac1	AC_DETIN < AC_VRMS × 45% (State A)	4	5	6	ms
AC off detection delay time 2	Tdlyac2	AC_VRMS × 65% > AC_DETIN > AC_VRMS × 45% (State B1)	4	5	6	ms
AC off detection delay time 3	Tdlyac3	AC_VRMS × 65% > AC_DETIN > AC_VRMS × 45% (State B2)	6.4	8	9.6	ms
AC off detection delay time 4	Tdlyac4	AC_DETIN > AC_VRMS × 65% (State C)	20	25	30	ms

5. AC Off Detect Signal Output Circuit Block (AC_DETOUT pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vacoutl	VCC = 18V, Iout = 10mA	—	0.5	1.0	V
Output High voltage	Vacouth	VCC = 18V, Iout = –10mA	17.0	17.5	—	V

6. MODE Pin Voltage Detection Circuit Block (MODE pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
MODE detection voltage Low	Vmodel		5.2	—	5.6	V
MODE detection voltage High	Vmodeh		7.6	—	8.4	V
Internal pull-up resistor	Rmode	MODE = 0.1V	35	50	65	kΩ

7. Clock Timer

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
1ms clock	Tclock		972	1024	1075	μs

◆ PFC Block

(Unless otherwise specified, the conditions are Ta = 27°C, VCC = 12V, MODE = GND)

8. PFC Output Circuit Block (PFC_OUT pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vpoutl	VCC = 18V, Iout = 10mA	—	0.03	0.1	V
Output High voltage	Vpouth	VCC = 18V, Iout = –10mA	17.85	17.9	—	V
Rise time *1	Tpoutr	VCC = 18V, CLOAD = 1000pF	—	35	100	ns
Fall time *1	Tpoutf	VCC = 18V, CLOAD = 1000pF	—	25	100	ns

*1 Rise time and fall time use VCC × 0.1 to VCC × 0.9 as the judgment voltages.

9. PFC-OK Signal Circuit Block (PFC_OK pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vacoutl	VCC = 18V, Iout = 10mA	—	0.5	1.0	V
Output High voltage	Vacouth	VCC = 18V, Iout = –10mA	17.0	17.5	—	V

10. AC Peak Voltage Sense Circuit Block (AC_VRMS pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Internal pull-down resistor value	Rvrms	AC_VRMS = 1.0V	0.6	0.8	1.0	MΩ

11. PFC Overcurrent Detection Circuit Block (PFC_CS pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Input threshold voltage	Vthcs		0.45	0.50	0.55	V
Blanking time	Tleb	PFC_CS = 1.0V	200	250	300	ns
Delay time	Tcsdly	CS to DRV PFC_CS = 0V ⇒ 1V (Rectangular waveform input)	100	150	200	ns

12. PFC Zero Current Detection Circuit Block (PFC_ZCD pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Input threshold voltage	Vthzcd		1.2	1.3	1.4	V
Hysteresis	Vzcdhys		180	200	220	mV
Clamp High voltage	Vclph	I = 3mA	4.0	4.4	5.0	V
Clamp Low voltage	Vclpl	I = –3mA	0.3	0.6	1.0	V
Restart timer delay	Tstart		180	200	220	μs
Maximum oscillation frequency (During overcurrent detection)	Fpfcmax	PFC_CS = 1.0V	180	220	260	kHz

13. Error Amplifier Output Circuit Block for PFC Voltage Control (PFC_VAO pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Trans-conductance	Vvaogm	(Design guarantee)	—	(90)	—	μA/V
Output High clamp voltage	Vvaoh	PFC_VSENSE = 2.45V	2.85	3.0	3.15	V
Clamp voltage at start-up	Vvao1	PFC_VSENSE = 2.0V (When other than resonant operation)	1.2	1.3	1.4	V
Source current	Ivaosc	PFC_VSENSE = 2.2V, PFC_VAO = 0.5V	10	20	40	μA
Output Low voltage	Vvaol	PFC_VSENSE = 2.55V	0	—	0.2	V
Sink current	Ivaosk	PFC_VSENSE = 2.65V, PFC_VAO = 3.0V	5	15	25	μA

14. PFC Maximum ON Time Control Circuit Block (PFC_TONMAX pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Charge current	Itoncharge	PFC_TONMAX = 0.1V	144	150	156	μA
Discharge time	Tdischarge	Ct = 1500pF, PFC_TONMAX = 3.2V to 0.1V	—	—	150	ns
PFC output ON time	Ton	PFC_VSENSE = 2.45V, Ct = 1500pF	26	29	32	μs

15. PFC Output Voltage Detection Circuit Block (PFC_VSENSE pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
PFC overvoltage detection voltage	Vovp1		2.849	2.922	2.995	V
PFC stop voltage	Vovp2		2.646	2.7	2.754	V
PFC stop cancel voltage	Vovp2hys		2.548	2.6	2.652	V
PFC control voltage	Vpfccnt		2.475	2.5	2.525	V
PFC non-operating detection voltage	Vpfcnonact		2.280	2.4	2.520	V
Resonant controller operation start voltage	Vrmstart		2.036	2.143	2.250	V
Resonant controller operation stop voltage	Vrmstop	When RM_OFFADJ = open	1.789	1.883	1.977	V
Pin short-circuit detection	Vshort		0.2	0.3	0.4	V
Pull-up current	Ivs	PFC_VSENSE = 0.1V	0.05	0.1	0.2	μA

16. Resonant Controller Stop Voltage Adjustment Circuit Block (RM_OFFADJ pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output voltage	Vrmoff		1.789	1.883	1.977	V
Latch voltage for external error detection	Voffadjng		3.8	4.0	4.2	V

17. PFC Overvoltage Detection Circuit Block (PFC_OVP pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
PFC overvoltage detection voltage	Vovp11		2.849	2.922	2.995	V
Pull-up current	Iovp	PFC_VSENSE = 0.1V	0.05	0.1	0.2	μA

◆ Resonant Controller Block

(Unless otherwise specified, the conditions are Ta = 27℃, VCC = 12V, MODE = GND, RM_RT = OPEN, Rfmin = 20kΩ)

18. Resonant Controller Output Circuit Block (RM_OUTP, RM_OUTN pins)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vroutl	VCC = 18V, Iout = 10mA	—	0.05	0.1	V
Output High voltage	Vrouth	VCC = 18V, Iout = –10mA	17.9	17.95	—	V
Rise time	Vroutr	VCC = 18V, C_{LOAD} = 1000pF	—	35	100	ns
Fall time	Vroutf	VCC = 18V, C_{LOAD} = 1000pF	—	35	100	ns

Note) Rise time is judged at VCC × 0.1 and fall time is judged at VCC × 0.9 respectively.

19. Resonant Controller Soft Start Circuit Block (RM_SS pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Soft start current	Irmss	RM_SS = 0V	15	20	25	μA
Clamp voltage	Vrmss		2.3	2.5	2.7	V
Soft start end detection voltage	Vssok		2.2	2.4	2.6	V
Overcurrent timer latch detection voltage	Vtimerlatch		3.8	4.0	4.2	V
Charging current during overcurrent detection	Iocc	RM_CS = 0.3V, SS = 3.0V	32	50	68	μA

20. Resonant Controller Frequency Control Circuit Block (RM_RT pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Maximum oscillation frequency	Frmmax	Irt = 2mA, Rfmin = 15kΩ	550	—	—	kHz
Deadband width	Tdb		270	300	330	ns
Multiple number of clamp frequency when soft start	Fclamp	f0/f4 (f0: RM_SS = 0V, f4: RM_SS = 2.5V)	3.5	4.5	5	times

21. Resonant Controller Minimum Frequency Adjustment Circuit Block (RM_FMIN pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Setting frequency 1	Fmin1	Rfmin = 30kΩ	(–3%)	41	(+3%)	kHz
Setting frequency 2	Fmin2	Rfmin = 20kΩ	(–3%)	60	(+3%)	kHz
Setting frequency 3	Fmin3	Rfmin = 15kΩ	(–3%)	79.5	(+3%)	kHz
Output voltage	Vfmin		1.0	1.2	1.4	V

22. Resonant Controller Current Detection Circuit Block (RM_CS pin, RM_CSGND pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Positive side detection	Vcs1p	When RM_OUTP = High	0.209	0.220	0.231	V
Negative side detection	Vcs1n	When RM_OUTN = High	–0.285	–0.250	–0.225	V
Detection delay time	Tcsdly	CS to DRV RM_CS = –0.3V ↔ 0.3V (Rectangular input)	100	150	200	ns
Detection mask time	Tcsmask	RM_CS = 0.3V	384	480	576	ns
Continuous load detection voltage	Vcs2	When RM_OUTP = High	0.158	0.175	0.193	V
Continuous load detection time	Tcs2	(When the time corresponds to 2.1s × 5 times)		(10)		s
Out of resonance prevention detection voltage	Vcsbfdet	When resonance start-up	–0.02	0	0.02	V
RS_CS pin offset current	Icspos	RM_CS = 0.1V	7	10	13	μA
RS_CSGND pin offset current	Icsneg	RM_CSGND = 0.1V	7	10	13	μA

Note) ◆ The shipping inspection is performed at room temperature. (The design is guaranteed with respect to temperature fluctuation.)

◆ The notation "±" of application current shown in the measurement conditions indicates that "–" is outflow current from the IC and "+" is inflow current to it.

23. List of Electrical Characteristics

Item	Specification ratings (Ta = 27˚C)			Design guarantee ratings (Ta = –25 to +85˚C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (VCC, PVCC pins)							
Current consumption in standby mode	—	700	1000	—	700	1000	μA
Current consumption in operation mode	—	3	3.5	—	3	3.5	mA
Low voltage misoperation prevention circuit block (VCC pin)							
Operation start voltage	10.2	11	11.8	10.2	11	11.8	V
Operation stop voltage	9	9.6	10.2	9	9.6	10.2	V
Hysteresis width	1.1	1.4	1.7	1.1	1.4	1.7	V
Reference voltage output block (VREF pin)							
Output voltage	4.85	5	5.15	4.85	5	5.15	V
Input stability	—	10	30	0	10	30.5 (*2)	mV
Load stability	—	20	50	—	20	50	mV
Pin voltage when NG latch (When TSD)	—	0.1	0.5	—	0.1	0.5	V
AC input detection circuit block (AC_DETIN pin)							
PFC operation start voltage	1.85	1.95	2.05	1.85	1.95	2.05	V
	1.65	1.75	1.85	1.65	1.75	1.85	V
Hysteresis width	0.17	0.2	0.23	0.17	0.2	0.23	V
AC detection reference voltage High 1	4.675	4.875	5.075	4.675	4.875	5.075	V
AC detection reference voltage Low 1	3.175	3.375	3.575	3.175	3.375	3.575	V
AC detection reference voltage High 2	1.1	1.3	1.5	1.1	1.3	1.5	V
AC detection reference voltage Low 2	0.7	0.9	1.1	0.7	0.9	1.1	V
AC off detection delay time 1	4	5	6	4	5	6	ms
AC off detection delay time 2	4	5	6	4	5	6	ms
AC off detection delay time 3	6.4	8	9.6	6.4	8	9.6	ms
AC off detection delay time 4	20	25	30	20	25	30	ms
AC input error detection output circuit block (AC_DETOUT pin)							
Output Low voltage	—	0.5	1	—	0.5	1	V
Output High voltage	17	17.5	—	17	17.5	—	V
Mode pin determination circuit block (MODE pin)							
MODE detection voltage Low	5.2	—	5.6	5.2	—	5.6	V
MODE detection voltage High	7.6	—	8.4	7.6	—	8.4	V
Internal pull-up resistor value	35	50	65	35	50	65	kΩ
Clock timer							
1ms clock	972	1024	1075	972	1024	1075	μs
PFC output circuit block (PFC_OUT pin)							
Output Low voltage	—	0.03	0.1	—	0.03	0.1	V
Output High voltage	17.85	17.9	—	17.85	17.9	—	V
Rise time	—	35	100	—	35	100	ns
Fall time	—	25	100	—	25	100	ns

Item	Specification ratings (Ta = 27˚C)			Design guarantee ratings (Ta = –25 to +85˚C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PFC-OK signal circuit block (PFC_OK pin)							
Output Low voltage	—	0.5	1	—	0.5	1	V
Output High voltage	17	17.5	—	17	17.5	—	V
AC peak voltage monitor circuit block (AC_VRMS pin)							
Internal pull-up resistor value	0.6	0.8	1	0.6	0.8	1	MΩ
PFC overcurrent detection circuit block (PFC_CS pin)							
Input threshold voltage	0.45	0.5	0.55	0.45	0.5	0.55	V
Blanking time	200	250	300	200	250	300	ns
Delay time	100	150	200	100	150	200	ns
PFC zero current detection circuit block (PFC_ZCD pin)							
Input threshold voltage	1.2	1.3	1.4	1.2	1.3	1.4	V
Hysteresis width	180	200	220	180	200	220	mV
Clamp High voltage	4	4.4	5	4	4.4	5	V
Clamp Low voltage	0.3	0.6	1	0.3	0.6	1	V
Restart timer delay	180	200	220	180	200	220	μs
Maximum oscillation frequency (When overcurrent is detected)	180	220	260	180	220	260	kHz
Error amplifier output circuit block for PFC voltage control (PFC_VAO pin)							
Trans-conductance	—	(90)	—		(90)		μA/V
Output High voltage	2.85	3	3.15	2.85	3	3.15	V
Clamp voltage at startup	1.2	1.3	1.4	1.2	1.3	1.4	V
Output source current	10	20	40	10	20	40	μA
Output Low voltage	0	—	0.2	0	—	0.2	V
Output sink current	5	15	25	5	15	25	μA
PFC maximum ON time control circuit block (PFC_TONMAX pin)							
Pin charging current	144	150	156	144	150	158 (*2)	μA
Pin discharging current	—	—	150	—	—	150	ns
On time	26	29	32	26	29	32	μs
PFC output voltage detection circuit block (PFC_VSENSE pin)							
PFC overvoltage detection	2.849	2.922	2.995	2.849	2.922	2.995	V
PFC stop voltage	2.646	2.7	2.754	2.646	2.7	2.754	V
PFC stop cancel voltage	2.548	2.6	2.652	2.548	2.6	2.652	V
PFC control voltage	2.475	2.5	2.525	2.475	2.5	2.526 (*2)	V
PFC non-operating detection voltage	2.28	2.4	2.52	2.28	2.4	2.52	V
Resonant controller operation start voltage	2.036	2.143	2.25	2.036	2.143	2.25	V
Resonant controller operation stop voltage	1.789	1.883	1.977	1.789	1.883	1.977	V
Pin short-circuit detection	0.2	0.3	0.4	0.2	0.3	0.4	V
Pin pull-up current	0.05	0.1	0.2	0.05	0.1	0.2	μA

Item	Specification ratings (Ta = 27˚C)			Design guarantee ratings (Ta = –25 to +85˚C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Resonant controller stop voltage adjustment circuit block (RM_OFFADJ pin)							
RM_OFFADJ pin output voltage	1.789	1.883	1.977	1.789	1.883	1.977	V
Latch voltage for external error detection	3.8	4	4.2	3.8	4	4.2	V
PFC overvoltage detection circuit block (PFC_OVP pin)							
PFC overvoltage detection voltage	2.849	2.922	2.995	2.849	2.922	2.995	V
Pin pull-up current	0.05	0.1	0.2	0.05	0.1	0.2	μA
Resonant controller output circuit block (RM_OUTP, RM_OUTN pins)							
Output Low voltage	—	0.05	0.1	—	0.05	0.1	V
Output High voltage	17.9	17.95	—	17.9	17.95	—	V
Rise time	—	35	100	—	35	100	ns
Fall time	—	35	100	—	35	100	ns
Resonant controller soft start circuit block (RM_SS pin)							
Soft start current	15	20	25	15	20	25	μA
Clamp voltage	2.3	2.5	2.7	2.3	2.5	2.7	V
Soft start end detection voltage	2.2	2.4	2.6	2.2	2.4	2.6	V
Overcurrent timer latch detection voltage	3.8	4	4.2	3.8	4	4.2	V
Charge current when overcurrent is detected	32	50	68	32	50	68	μA
Resonant controller soft start circuit block (RM_RT pin)							
Maximum oscillation frequency	550	—	—	550	—	—	kHz
Deadband width	270	300	330	270	300	330	ns
Clamp frequency magnification during soft start	3.5	4.5	5	3.5	4.5	5	times
Resonant controller minimum frequency adjustment circuit block (RM_FMIN pin)							
Setting frequency 1	39.77	41	42.23	39.46 (*2)	41	42.68 (*2)	kHz
Setting frequency 2	58.2	60	61.8	58.20	60	61.80	kHz
Setting frequency 3	77.12	79.5	81.88	76.13 (*2)	79.5	81.88	kHz
Pin output voltage	1	1.2	1.4	1	1.2	1.4	V
Resonant controller current detection circuit block (RM_CS pin, RM_CSGND pin)							
Positive side detection	0.209	0.22	0.231	0.209	0.22	0.231	V
Negative side detection	–0.285	–0.25	–0.225	–0.285	–0.25	–0.225	V
Detection delay time	100	150	200	100	150	200	ns
Detection mask time	384	480	576	384	480	576	ns
Continuous load detection voltage	0.158	0.175	0.193	0.158	0.175	0.193	V
Continuous load detection time	—	(10)	—		(10)		s
Out of resonance prevention detection voltage	–0.02	0	0.02	–0.02	0	0.02	V
RM_CS pin offset current	7	10	13	7	10	13	μA
RM_CSGND pin offset current	7	10	13	7	10	13	μA

*1 Ratings are design guarantee values within this temperature range.

*2 Specification values at room temperature may not be satisfied because of temperature dependence.

Detailed Description of Each Block

◆ Common Circuit Block

1. Misdetection Prevention Circuit

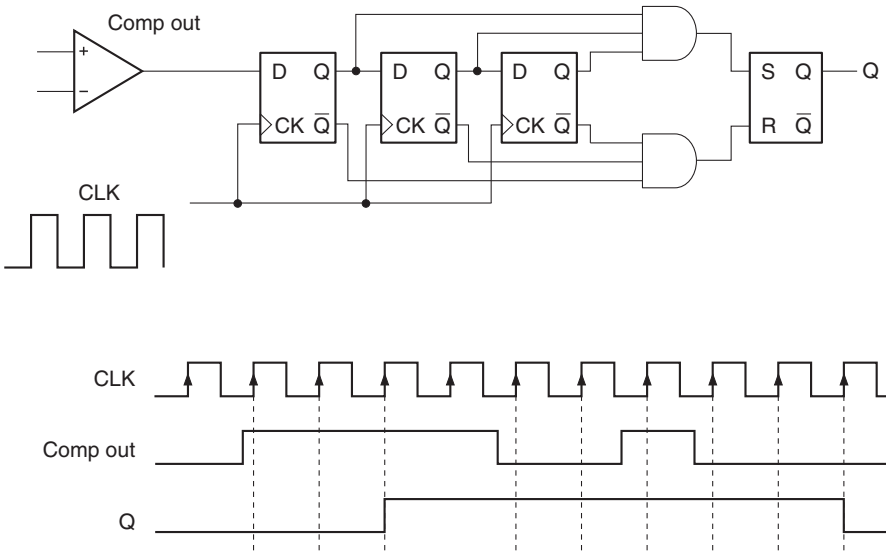


Fig. 1. Equivalent Circuit Corresponded to 1ms × 3 Times

Fig. 1 above shows the equivalent circuit corresponded to 1ms × 3 times.
When CLK has a 1ms cycle, comp out is monitored at the rising edge of every 1ms, and the output Q is defined when it reaches three times. The 5 times-corresponded circuit also operates using a similar system, so the approach is the same.

The clocks used for each setup time are generated by frequency dividing the 1MHz clock. The setup variance time of the 1ms × 3 times correspondence circuit in the example above is as follows. Variance of 2ms < setup time < 3ms occurs due to the comp out inversion timing. In addition, taking into account the basic clock 1kHz variance, the 1ms (1024μs) clock has variance of 0.972ms to 1.075ms (±5%), so at the maximum variance the setup variance time is 1.944ms < setup time < 3.225ms.

Setup time of misdetection prevention counter (when the basic clock of 1MHz has no variance) used for this IC is shown below.

- Corresponds to 1μs × 4 times ..... 3μs to 4μs
- Corresponds to 1μs × 16 times ..... 15μs to 16μs
- Corresponds to 128μs × 3 times ..... 256μs to 384μs
- Corresponds to 128μs × 5 times ..... 512μs to 640μs
- Corresponds to 1ms × 3 times ..... 2ms to 3ms (Converted by 1ms for 1.024ms)
- Corresponds to 1ms × 5 times ..... 4ms to 5ms
- Corresponds to 4.1ms × 3 times ..... 8.2ms to 12.3ms (Converted by 4.1ms for 4.096ms)
- Corresponds to 16ms × 4 times ..... 48ms to 64ms (Converted by 16ms for 16.4ms)
- Corresponds to 66ms × 8 times ..... 462ms to 528ms (Converted by 66ms for 65.5ms)
- Corresponds to 2.1s × 3 times ..... 4.2s to 6.3s (Converted by 2.1s for 2.097s)
- Corresponds to 2.1s × 5 times ..... 8.4s to 10.5s

2. AC Detection Circuit Block

Fig. 2-1 shows the AC detection block equivalent circuit.

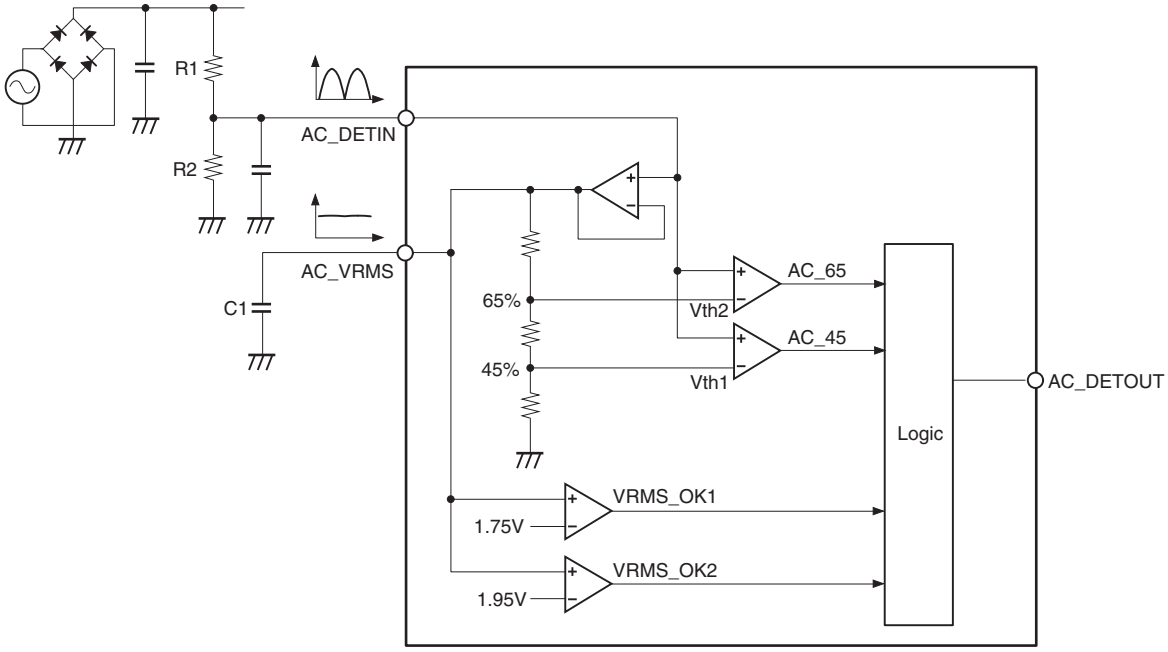


Fig. 2-1. AC Detection Block Equivalent Circuit

The AC detection circuit block detects the AC input voltage by directly monitoring the full-wave rectified AC input waveform.
The wave input to the AC_DETIN pin is peak-held at the AC_VRMS pin by a buffer circuit, and reference voltages equivalent to 45% (Vth1) and 65% (Vth2) of the peak value are generated internally. The AC input is constantly monitored to determine the voltage range by comparing these reference voltages and the AC_DETIN pin voltage.
The AC_VRMS pin voltage is compared with the internal reference voltages, and AC input is detected when the AC_VRMS pin voltage is 1.95V or more, or AC OFF when 1.75V or less. When R1 = 1000kΩ and R2 = 18kΩ in Fig. 2-1, AC input is detected when VAC = 78Vrms or more.
In addition, connect a capacitor of at least 0.47μF or more to the AC_VRMS pin. An internal resistor is provided to generate the 65% and 45% voltages of the AC_VRMS pin voltage, and when this external capacitance value is too small, discharge may make peak hold impossible.

Fig. 2-2 shows the state transition diagram for the AC OFF detection circuit. The state transition conditions are related to the POR, AC65, AC45, VRMSOK1 and VRMSOK2 input signals, and the timer values in each state. POR is the IC reset signal, and AC65, AC45, VRMSOK1 and VRMSOK2 are the outputs of each comparator shown in Fig. 2-1. 1μs × 16 times filter processing is applied to these signals. The state transition logic operating frequency is 7.8kHz.
In addition, regardless of the state transitions shown in Fig. 2-2, VRMSOK2 = High (AC_VRMS pin voltage > 1.95V) must be set up to obtain AC_DETOUT = High output at start-up. After VRMSOK2 = High is detected (1ms × 3 times), AC_DETOUT goes High.

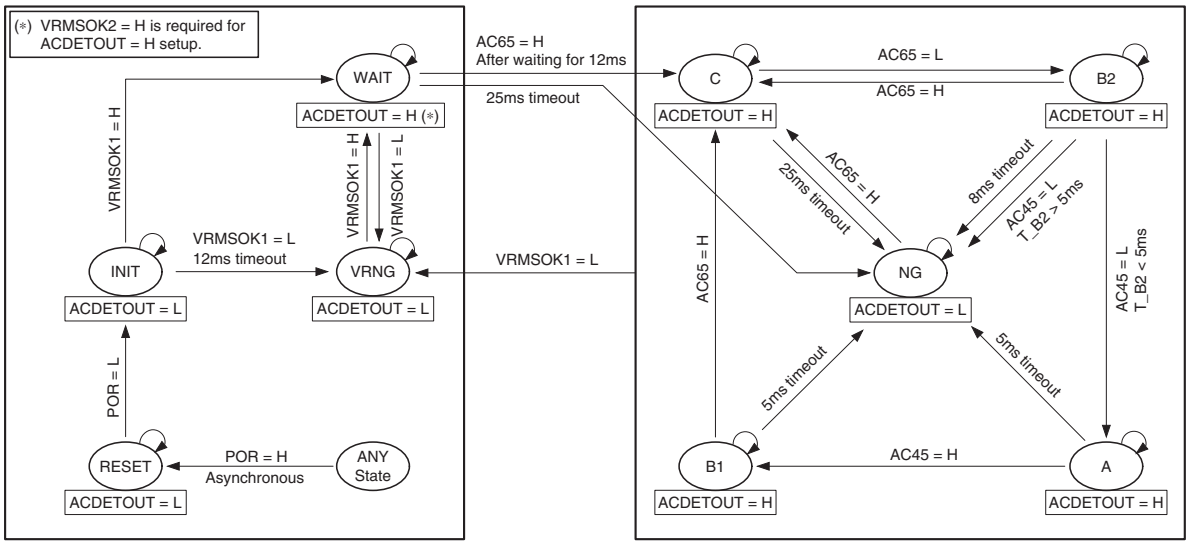


Fig. 2-2. AC Detection State Transition Diagram

The AC_DETOUT pin is the output signal for this function, and outputs High when the AC input state is normal, or Low when AC OFF or other abnormal state is detected. Fig. 3 shows an image of the state transitions when normal AC input continues.

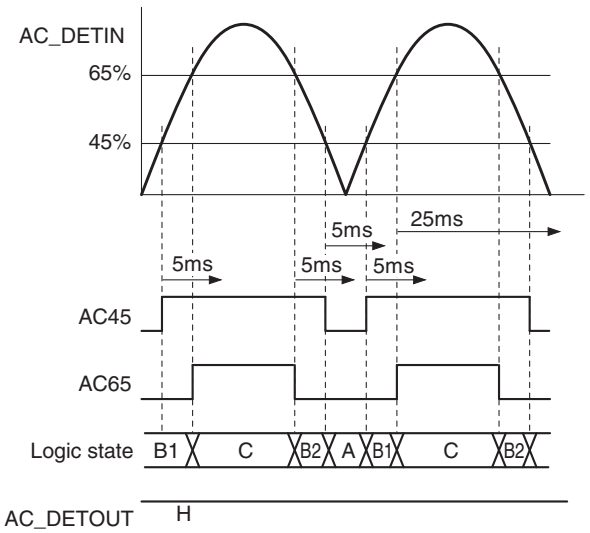


Fig. 3. AC_DETIN Input Waveform and State Transitions

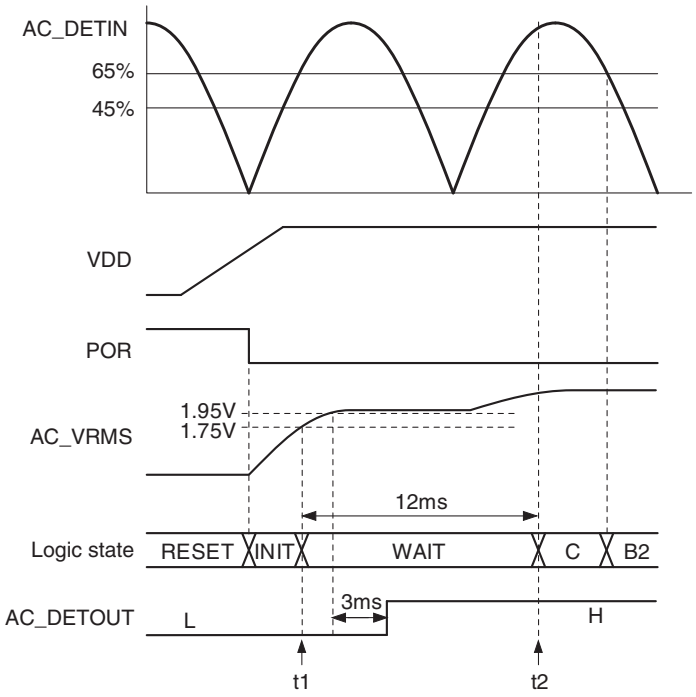
In Fig. 3, the internal logic signal transitions as follows.

- When the AC input rises to 65% or more within 5ms after the state transitions to “B1”, the state transitions to “C”.
- When the AC input falls to 65% or less within 25ms after the state transitions to “C”, the state transitions to “B2”.
- When the AC input falls to 45% or less within 5ms after the state transitions to “B2”, the state transitions to “A”.
- When the AC input rises to 45% or more within 5ms after the state transitions to “A”, the state transitions to “B1”.

When the above cycle repeats, AC_DETOUT continues to output High.

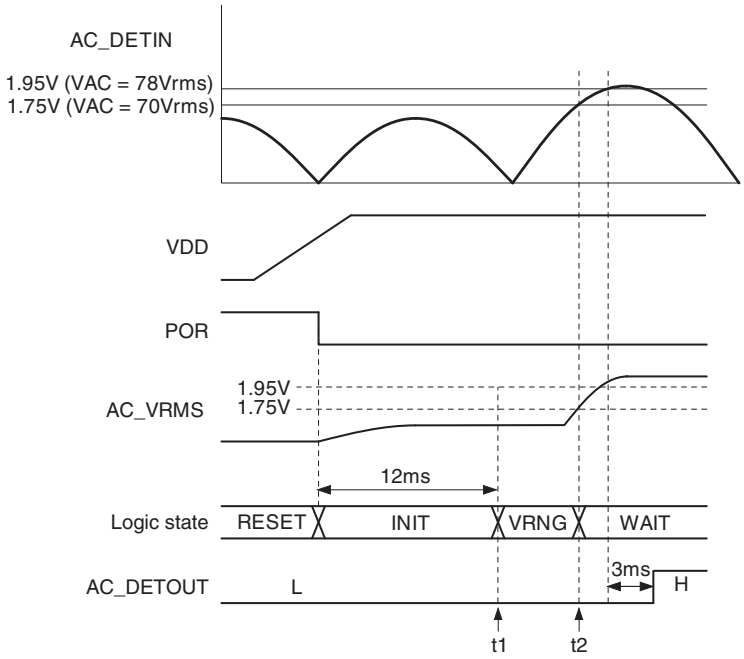
Other behaviors during start-up or AC voltage OFF are described on the following pages.

◆ **During normal start-up**



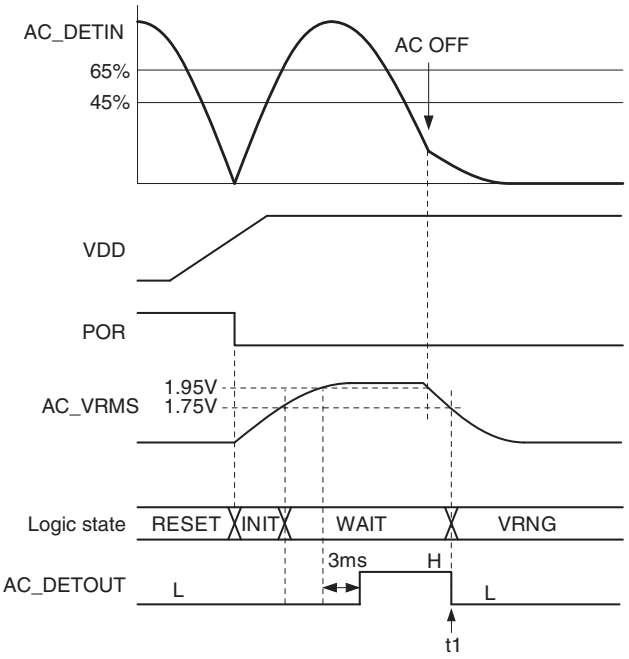
- When POR is canceled after power-on, the state transitions to “INIT”. AC_DETOUT is Low output in the “RESET” and “INIT” states.
- When the AC_VRMS pin voltage rises to 1.75V or more in the “INIT” state, the state transitions to “WAIT” (t1), but AC_DETOUT continues to output Low until the AC_VRMS pin voltage reaches 1.95V.
- When the AC_VRMS pin voltage rises to 1.95V after the state transitions to “WAIT”, VRMSOK2 goes High, and then AC_DETOUT outputs High 3ms after that.
- When the AC_DETIN pin voltage exceeds 65% of the AC_VRMS pin voltage after 12ms have elapsed in the “WAIT” state, the state transitions to “C” (t2) and the normal state judgment cycle starts.

◆ **Start-up when the AC voltage is low**



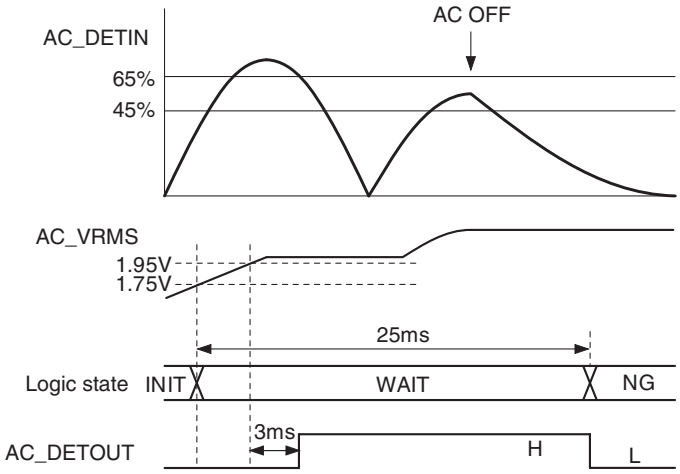
- When the AC_VRMS pin voltage does not reach 1.75V within 12ms in the “INIT” state after POR is canceled, an AC input error is judged, the state transitions to “VRNG”, and AC_DETOUT continues to output Low (t1).
- When the IC detects that the AC_VRMS pin voltage has risen to 1.75V or more in the “VRNG” state, the state transitions to “WAIT” (t2). Then, AC_DETOUT outputs High 3ms after the AC_VRMS pin voltage rises to 1.95V or more.

◆ **When AC OFF occurs in the “WAIT” state (1)**



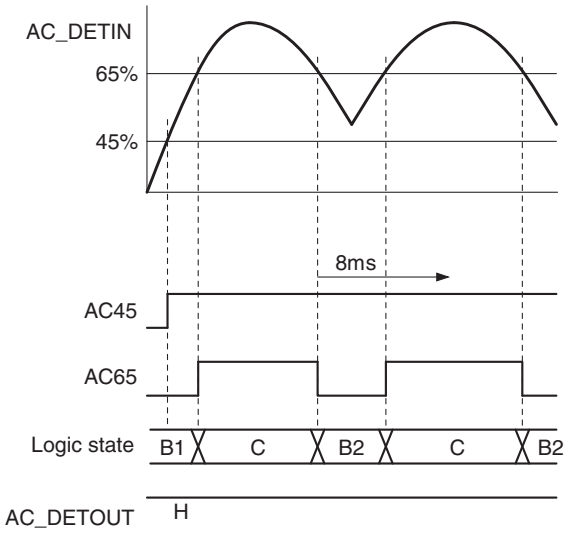
- When the AC_VRMS pin voltage falls to 1.75V or less in the “WAIT” state, AC OFF is judged, the state transitions to “VRNG”, and AC_DETOUT outputs Low (t1).

◆ **When AC OFF occurs in the “WAIT” state (2)**



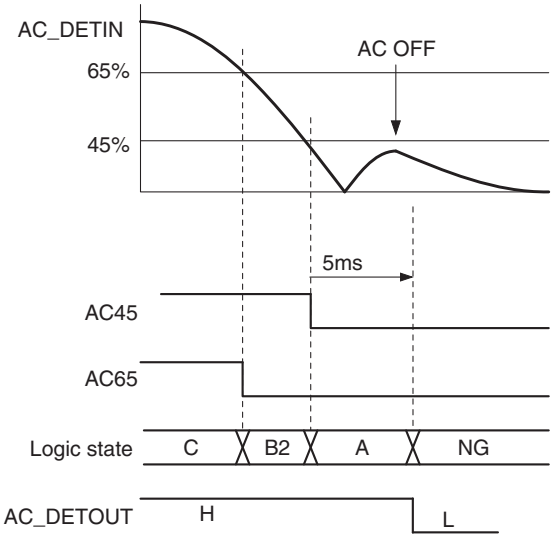
- When the AC_VRMS pin voltage is 1.95V or more but the AC_DETIN pin voltage has not reached 65% of the AC_VRMS pin voltage (the state has not transitioned to “C”) within 25ms after the state transitions to “WAIT”, AC OFF is judged, the state transitions to “NG”, and AC_DETOUT outputs Low.

◆ **During normal AC input**



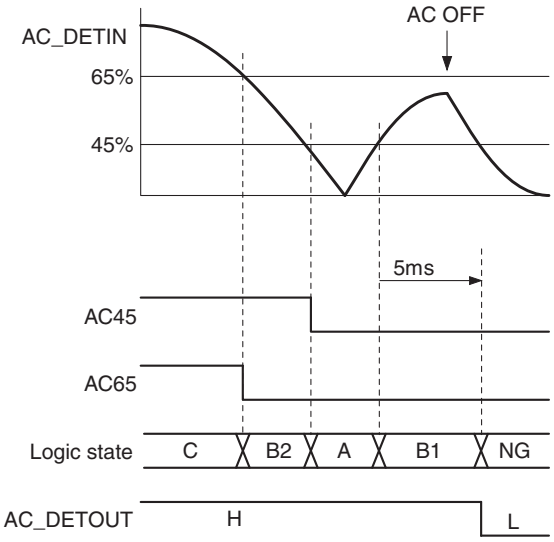
- When the AC_DETIN pin voltage rises to 65% or more of the AC_VRMS pin voltage within 8ms after the state transitions to “B2”, the state transitions to “C”.
- AC_DETOUT continues to output High even when the “C” → “B2” → “C” cycle repeats.

◆ **AC OFF in the “A” state**



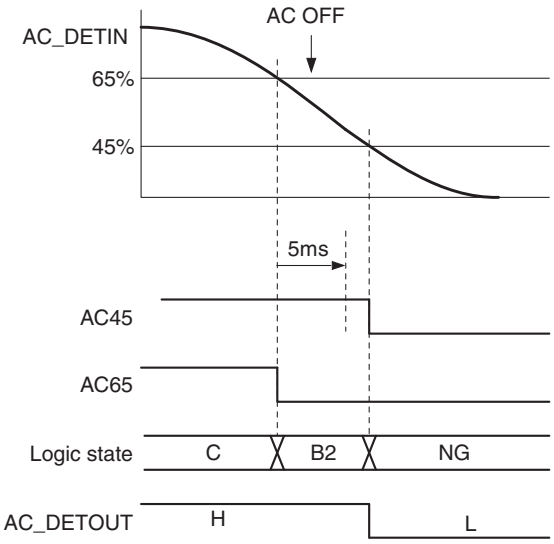
- When the AC_DETIN pin voltage does not rise to 45% or more of the AC_VRMS pin voltage within 5ms after the state transitions to “A”, AC OFF is judged, the state transitions to “NG”, and AC_DETOUT outputs Low.

◆ **AC OFF in the “B1” state**



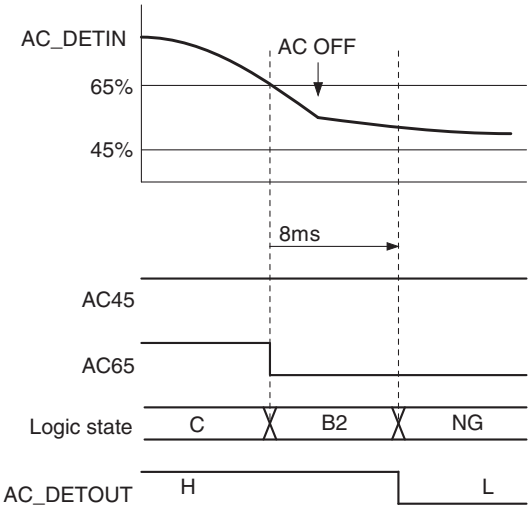
- When the AC_DETIN pin voltage does not rise to 65% or more of the AC_VRMS pin voltage within 5ms after the state transitions to “B1”, AC OFF is judged, the state transitions to “NG”, and AC_DETOUT outputs Low.

◆ **AC OFF in the “B2” state (1)**



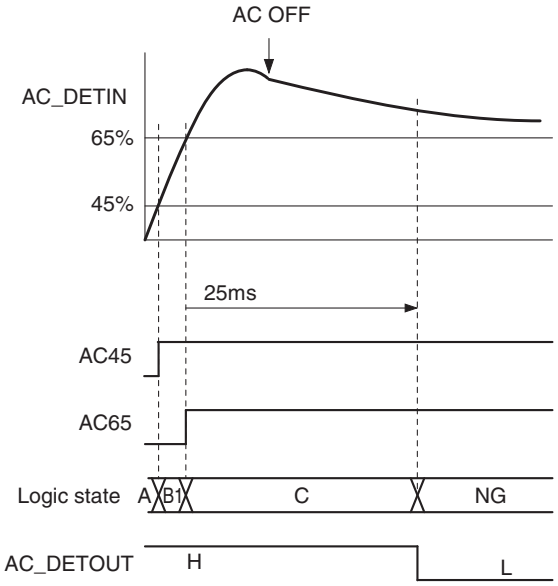
- When 5ms or more have elapsed by the time the AC_DETIN pin voltage falls to 45% or less of the AC_VRMS pin voltage after the state transitions to “B2”, AC OFF is judged, the state transitions to “NG”, and AC_DETOUT outputs Low.

◆ **AC OFF in the “B2” state (2)**



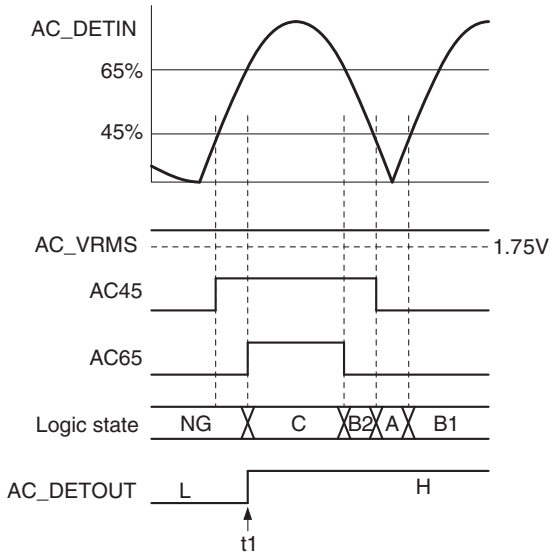
- When the AC_DETIN pin voltage does not rise to 65% or more or fall to 45% or less of the AC_VRMS pin voltage within 8ms after the state transitions to “B2”, AC OFF is judged, the state transitions to “NG”, and AC_DETOUT outputs Low.

◆ **AC OFF in the “C” state**



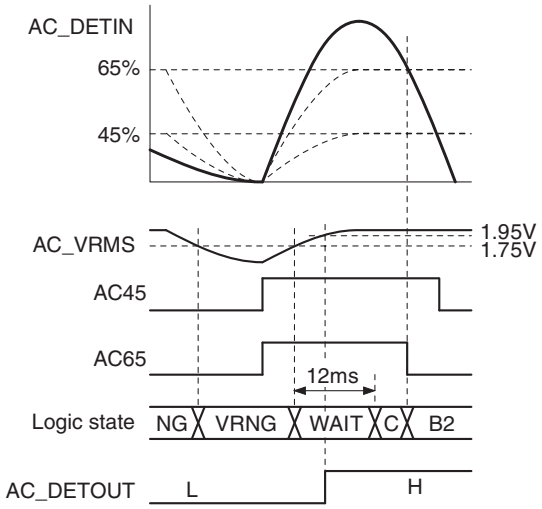
- When the AC_DETIN pin voltage does not fall to 65% or less of the AC_VRMS pin voltage within 25ms after the state transitions to “C”, AC OFF is judged, the state transitions to “NG”, and AC_DETOUT outputs Low.

◆ **Return to the normal cycle from the “NG” state (1)**



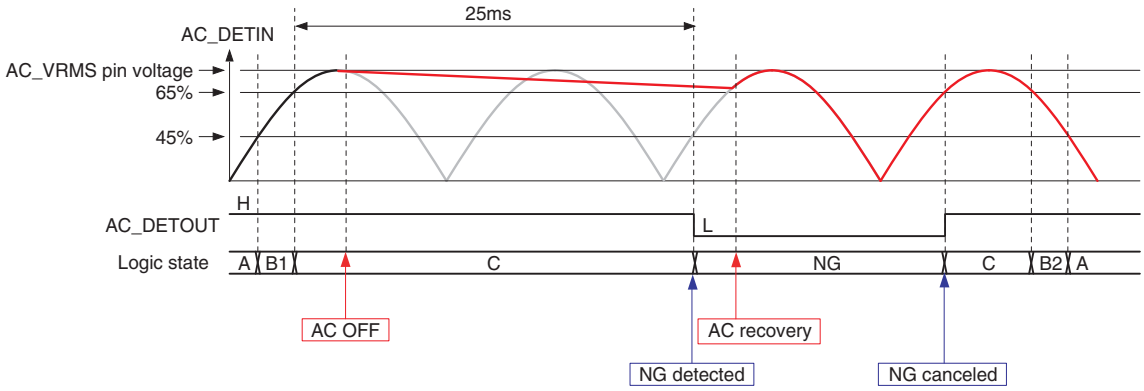
- When the AC_DETIN pin voltage rises to 65% or more of the AC_VRMS pin voltage while the AC_VRMS pin voltage is 1.75V or more in the “NG” state, the state transitions to “C”, AC_DETOUT outputs High, and the normal state judgment cycle starts. (t1)

◆ **Return to the normal cycle from the “NG” state (2)**



- When the AC_VRMS pin voltage falls to 1.75V or less in the “NG” state, the state transitions to “VRNG”.
- When AC is input again and the AC_VRMS pin voltage rises to 1.75V or more, the state transitions to “WAIT”, Then, when the AC_VRMS pin voltage rises further to 1.95V, AC_DETOUT outputs High. After that, when the AC input rises to 65% or more, the state transitions to “C” and the normal state judgment cycle starts.

◆ **Return to the normal cycle after the state transitions from “C” to “NG”**



- The return sequence from the “NG” state when the “C” state has continued for 25ms or more is as follows. Operation returns to the normal cycle when the AC_DETIN pin voltage falls below 65% of the AC_VRMS pin voltage, and then exceeds 65% of the AC_VRMS pin voltage again after that.

3. MODE Pin Voltage Detection Circuit Block

Normal sequence mode and standby mode can be set in accordance with the MODE pin input voltage. Normal sequence mode can be set by short-circuiting the MODE pin to GND, and standby mode can be set by short-circuiting the MODE pin to VCC or leaving the pin open.
Note that this IC has a test mode used to set the minimum resonant controller. It is possible to operate only the resonant controller by setting the MODE pin voltage to the following voltage range.

5.6V < MODE pin voltage < 7.6V

In addition, the mode transition setup times when the MODE pin voltage is switched are as follows.

- Normal sequence mode ⇒ Standby mode : 128μs × 2 times
- Standby mode ⇒ Normal sequence mode : 128μs × 2 times + internal logic setup time of 320μs to 448μs
- Normal sequence mode ⇒ Test mode : 128μs × 3 times
- Standby mode ⇒ Test mode : 128μs × 3 times
- Test mode ⇒ Normal sequence mode : 128μs × 3 times
- Test mode ⇒ Standby mode : 128μs × 3 times

4. PFC_OK Signal Output Circuit Block

When the PFC output voltage (+B) rises to 330V or more, the resonant circuit operates, and the end of resonant soft start is detected, the PFC_OK signal goes to High output. In this IC the PFC_OK signal is controlled to High output by detecting that the RM_SS pin voltage is 2.4V (typ.) or more (4.1ms × 3 times). In addition, when the IC detects that the PFC output voltage has fallen to the voltage set by the RM_OFFADJ pin (default: 290V) or less (1ms × 3 times), the PFC_OK signal is Low output.
Fig. 4 shows the PFC_OK signal output timing chart.
In addition, the PFC_OK signal is also Low output during the following operations.

- During NG latch
- When transition to standby mode
- When the PFC circuit is stopped (after AC_VRMS < 1.75V, 66ms × 8 times is set up)

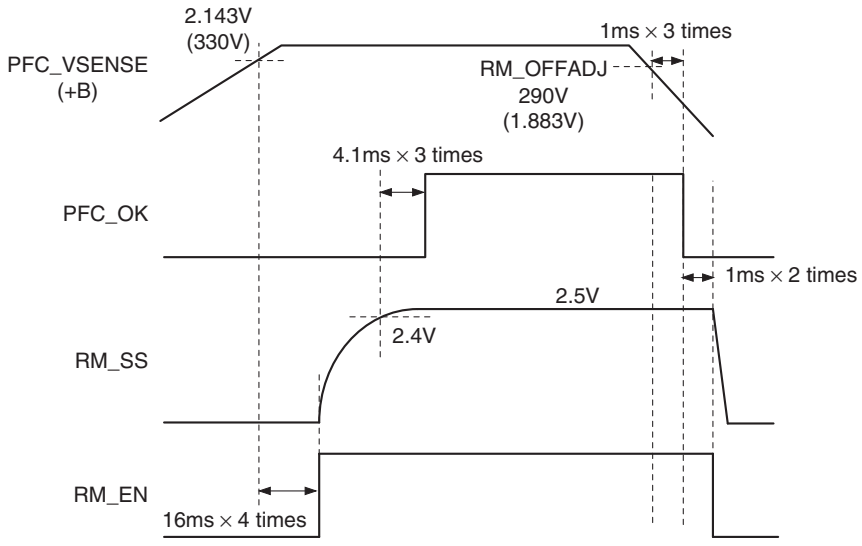


Fig. 4. PFC_OK Signal Output Sequence

◆ **PFC Block**

5. PFC Control Circuit Block

This IC has a Power-factor Correction (PFC) controller using a boost converter circuit that operates in multiplierless Critical Conduction Mode (CRM). Fig. 5 describes an overview of operation.

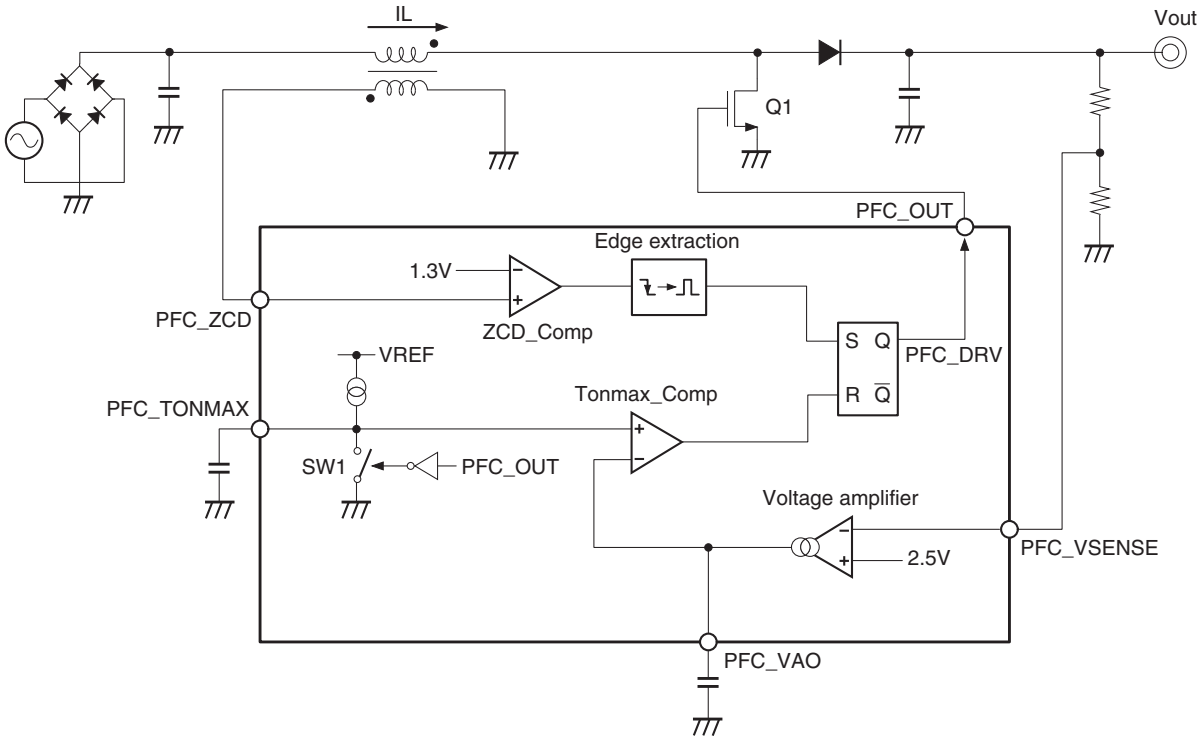


Fig. 5. Operation Circuit Block Diagram

This IC performs critical conduction mode switching operation that applies self-oscillation without using an oscillator. Fig. 6 shows the output waveform of each block in the steady state.

t1: When MOSFET Q1 goes ON, SW1 goes OFF, and the inductor current (IL) rises from zero at the slope Vin/L.
At the same time charging starts to the PFC_TONMAX pin external capacitor, and continues until the PFC_TONMAX pin voltage reaches the PFC_VAO pin voltage. The PFC_VAO pin voltage value corresponds to the PFC output voltage (Vout).

t2: When the PFC_TONMAX pin voltage reaches the PFC_VAO pin voltage, Tonmax_Comp inverts and a High signal is output, the RESET signal is input to the RS latch circuit, and Q1 goes OFF. When Q1 goes OFF, the inductor voltage inverts, and current is supplied to the output side via the diode. In addition, during this period the inductor current decreases at the slope (Vout – Vin)/L, and a positive voltage is generated in the auxiliary winding (PFC_ZCD pin voltage).
The charge stored on the PFC_TONMAX pin is discharged instantly by setting SW1 to ON.

t3: When the inductor current reaches 0A, the inductor voltage drops rapidly, and at the same time the PFC_ZCD pin voltage also drops. When the IC detects that the PFC_ZCD pin voltage has fallen to 1.3V or less, the SET signal is input to the RS latch circuit, Q1 is turned back ON, and operation shifts to the next switching cycle.

Critical conduction mode switching is continued by repeating the above operations.
Note that PFC control circuit in critical conduction mode, the switching frequently changes constantly according to the instantaneous value of the AC input voltage.

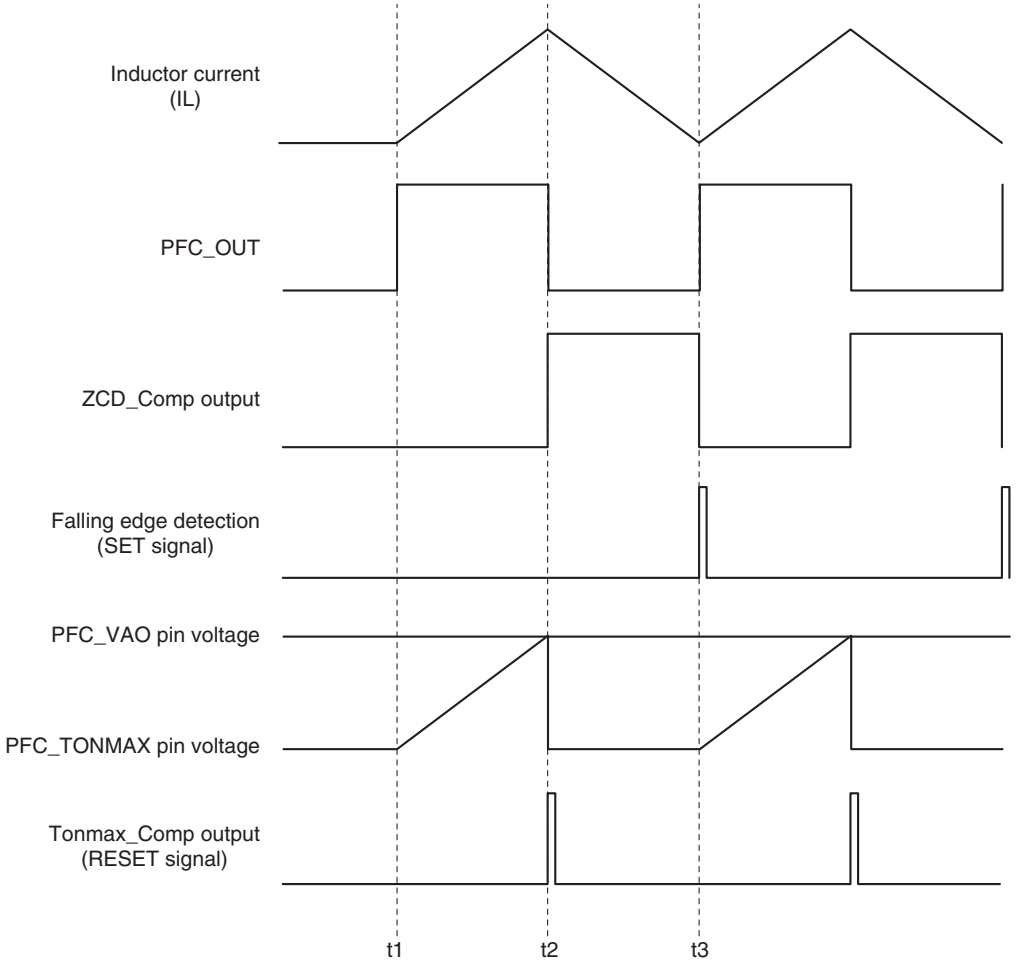


Fig. 6. Switching Operation Block Waveforms

6. PFC Zero Current Detection Circuit Block

The zero current detection circuit performs critical conduction mode operation, so this circuit detects that the inductor current has become 0A. When the voltage of the inductor auxiliary winding connected to the PFC-ZCD pin is set at the polarity shown in Fig. 7, a positive voltage is generated in the auxiliary winding when MOSFET_Q1 is OFF, and a negative voltage is generated in the auxiliary winding l when MOSFET_Q1 is ON. This auxiliary winding voltage varies greatly according to the input voltage and the circuit configuration, so internal upper limit and lower limit clamp circuits are provided. A resistor (Rzcd) is required to limit the outflow and inflow current to the clamp circuit to ensure normal IC operation. Set the Rzcd value so that this clamp circuit current is ±3mA or less.

Threshold mode control that uses self-oscillation requires a trigger signal to realize stable operation during start-up or under light load conditions. This IC has a restart timer, and when the PFC_OUT output is continuously OFF for 200μs (typ.) or more, the trigger signal is automatically generated and MOSFET_Q1 is turned ON.

In addition, an internal maximum oscillation frequency limit function (Fpfcmax) is provided to prevent the PFC oscillation frequency from rising excessively during abnormal operation when an output diode short-circuit or other overcurrent state is detected. After an overcurrent is detected, the PFC output is forcibly turned OFF using pulse-by-pulse control. In this case, a counter (T_offmin: 4μs (typ.)) that temporarily fixes the PFC output Low operates by overcurrent detection signal. The signal from PFC_ZCD is masked during that period, and a High output pulse is generated after counter operation ends.

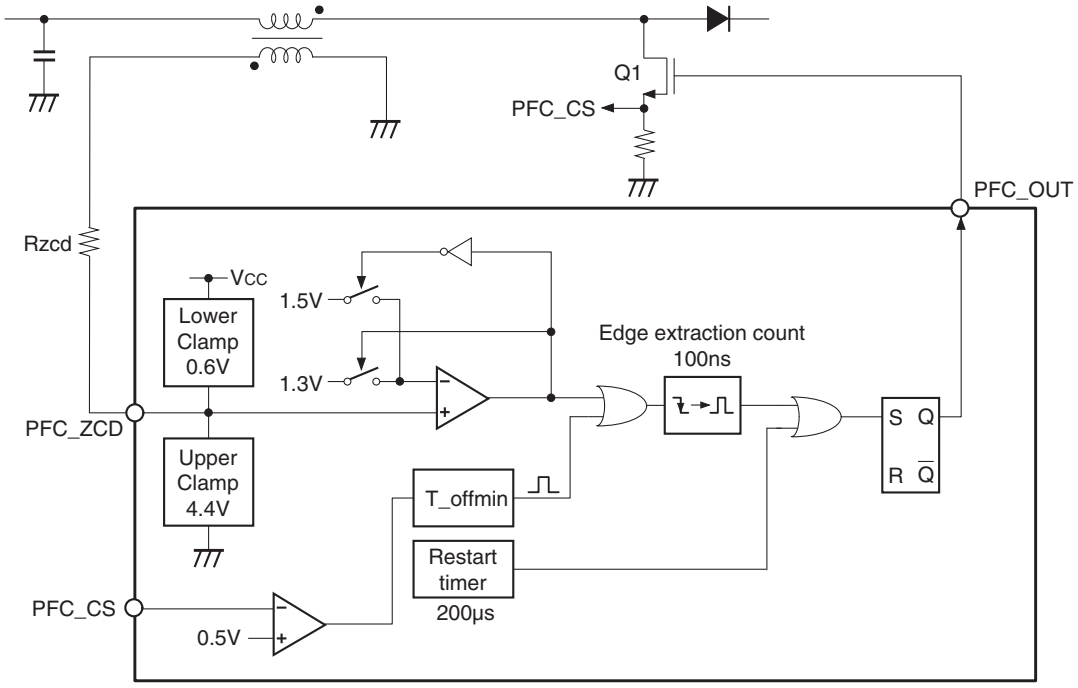


Fig. 7. ZCD Control Block Equivalent Circuit

7. PFC Maximum ON Time Control Circuit Block

The PFC_OUT ON time (Ton) is determined by the capacitor (Ct) connected to the PFC_TONMAX pin, the charging current (Icharge) from inside the IC, the PFC_VAO pin voltage (Vamp), and the detection comparator offset voltage (Voffset).
The charging current to the PFC_TONMAX pin is 150μA (typ.), and the detection comparator offset voltage is 180mV (typ.), so the ON time relative to the external capacitor is obtained by the following equation.

$$Ton = \frac{(Vamp - Voffset) \times Ct}{Icharge}$$

Example) When Ct = 1500pF, Vamp = 3.0V, Voffset = 0.18V, Icharge = 150μA

Ton = 28.2μs

Fig. 8 shows the equivalent circuit for the area around the PFC_TONMAX pin.

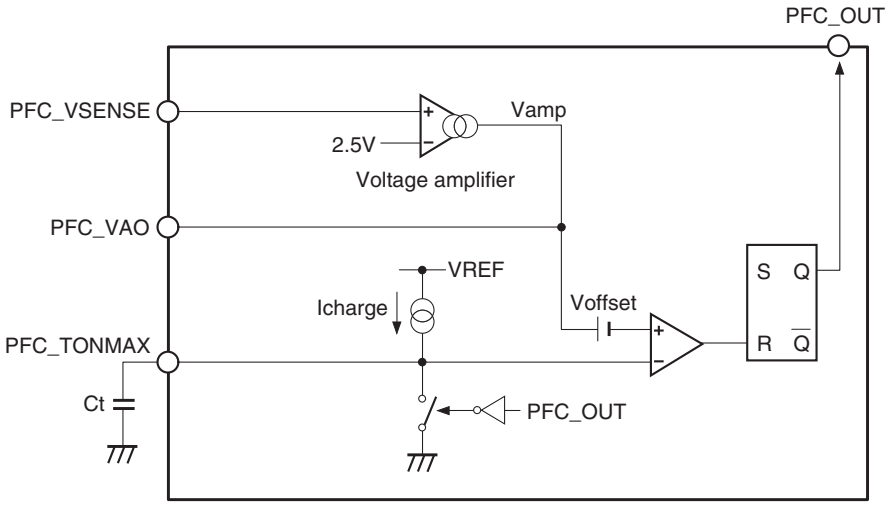


Fig. 8. Maximum ON Time Control Block Equivalent Circuit

8. PFC_VAO Clamp Voltage Control Circuit Block

This IC has a function that limits the power according to the PFC/resonance start-up as a countermeasure against choke winding and film capacitor squealing due to overcurrent control during startup.
During start-up, the PFC_VAO output voltage is clamped to 1.3V when the PFC_VSENSE voltage is low, and the clamp voltage is switched as the resonant circuit starts up. The clamp voltage switching timing is as follows.

- ◆ 1.3V ⇒ 3.2V: After PFC_VSENSE > 2.143V is detected, and 16ms × 4 times is set up (when resonant circuit operation starts)
- ◆ 3.2V ⇒ 1.3V: After PFC_VSENSE < RM_OFFADJ (default: 1.883V) is detected, and 1ms × 5 times is set up (when resonant circuit operation stops)

During start-up, the PFC_VAO pin voltage is clamped to 1.3V, and voltage step-up operation is performed until PFC_VSENSE reaches 2.143V (+B = 330V). After PFC_VSENSE > 2.143V is detected and a 16ms × 4 times delay, resonant circuit operation starts, and the PFC_VAO clamp voltage is switched from 1.3V to 3.2V.
The CXA3809M when the PFC_VSENSE voltage falls by AC input sag (AC momentary stop) is different in sequence from the CXA3790M. It controls with the clamp voltage of 3.2V even if the PFC_VSENSE voltage is less than 2.4V (AC SAG1).
When the AC input sag time is long and the PFC_VSENSE voltage falls to the resonant circuit stop voltage (RM_OFFADJ pin setting voltage) or less (AC SAG2), the voltage step-up sequence restarts from the state with the clamp voltage lowered to 1.3V in the same manner as during start-up. Fig. 9 shows the PFC_VAO clamp voltage sequence.

Note) The +B voltage shows an example of setting that PFC_VSENSE = 2.5V when +B = 385V.

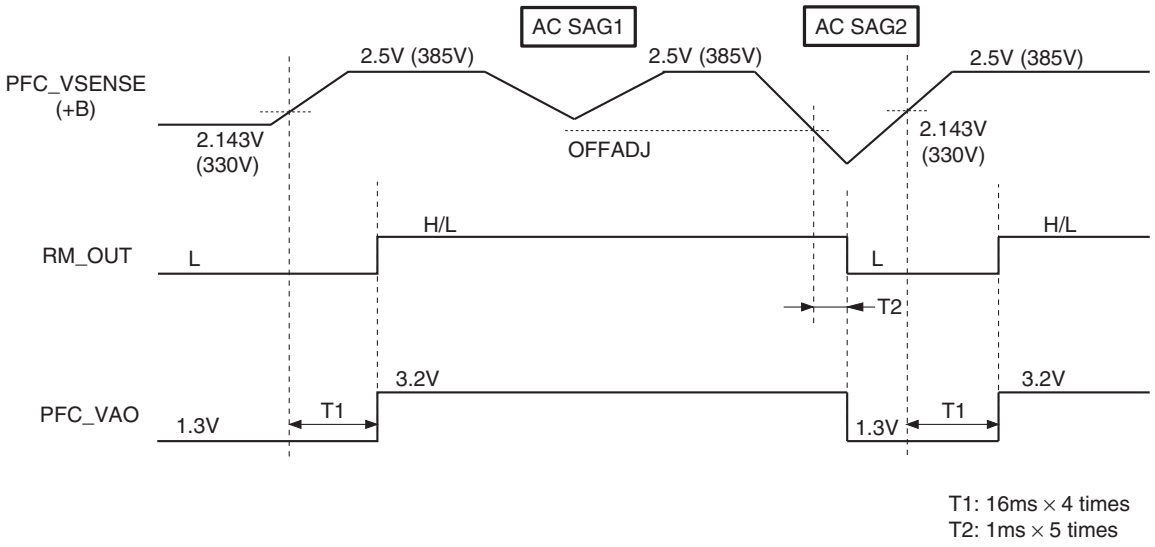


Fig. 9. PFC_VAO Clamp Voltage Cancel Sequence

9. PFC Output Voltage Detection Circuit Block

Fig. 10 shows the equivalent circuit for the area around the PFC_VSENSE and PFC_OVP pins.

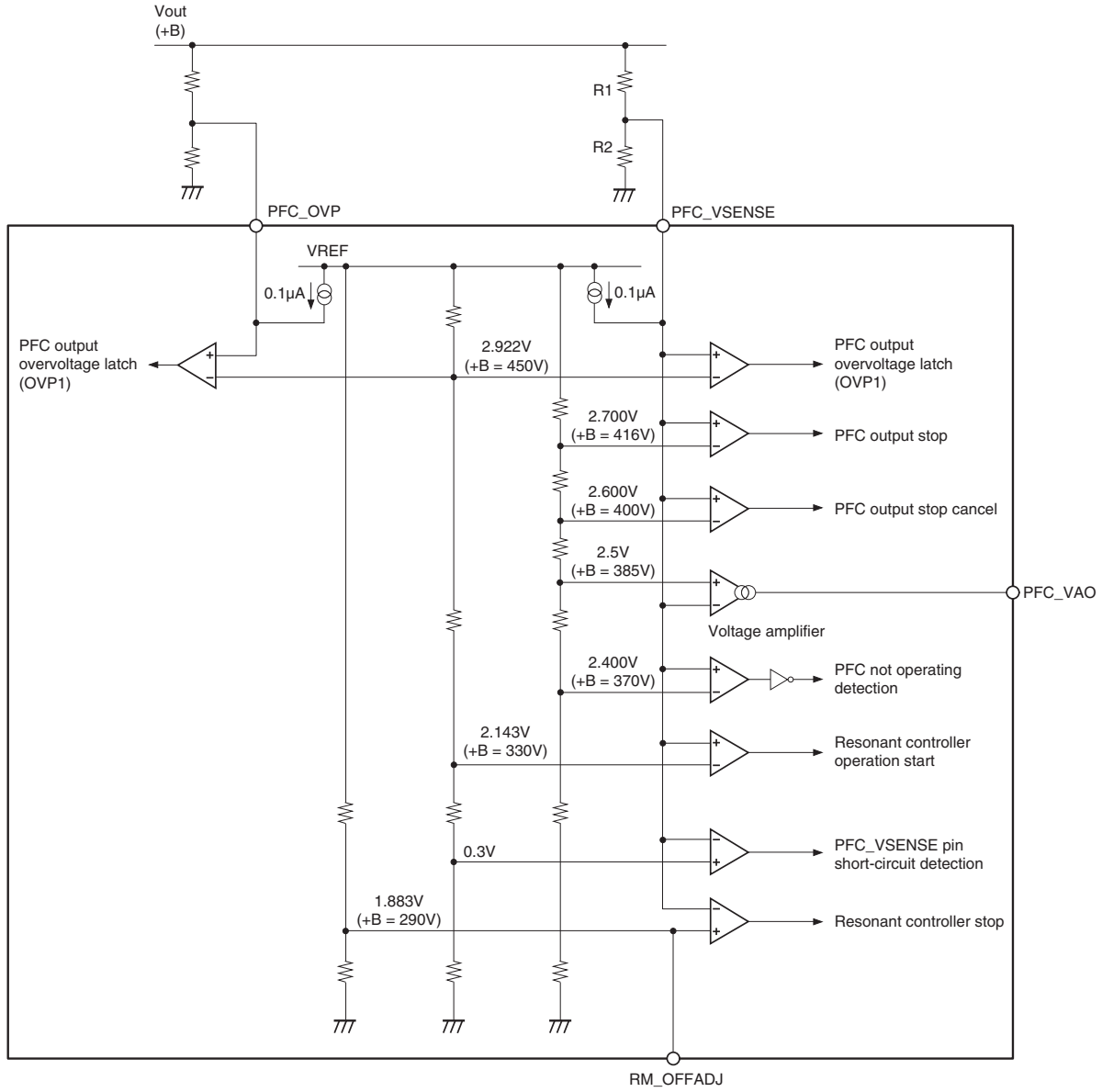


Fig. 10. PFC Output Voltage Detection Block Equivalent Circuit

The PFC_VSENSE pin detects the PFC output voltage, and is also the circuit that performs rise sequence control during start-up, and protects against output voltage fluctuations due to rapid load changes.

- **PFC overvoltage latch (OVP1)**

  IC latch operation results when PFC_VSENSE > 2.922V (+B > 450V) is detected.

- **PFC overvoltage output stop**

  PFC_OUT output is stopped when PFC_VSENSE > 2.7V (+B > 416V) is detected.
  PFC_OUT output stop is canceled when PFC_VSENSE < 2.6V (+B < 400V) is detected.

- **PFC not operating detection**

  IC latch operation results when PFC_VSENSE < 2.4V (+B < 370V) is detected for 10s (2.1s × 5 times) or more.

- **Resonant controller operation start**

  Resonant controller operation is started when PFC_VSENSE > 2.143V (+B > 330V) is detected.

- **Resonant controller stop**

  Resonant controller operation is stopped when PFC_VSENSE < 1.883V (+B < 290V) is detected. (When the RM_OFFADJ pin is open)

- **PFC_VSENSE pin open/short-circuit detection**

  It stops PFC_OUT output when PFC_VSENSE < 0.3V is detected by open of resistor R1, short-circuit of resistor R2, etc. In addition, when the PFC_VSENSE pin is open, the pin voltage is forcibly pulled up by the internally supplied 0.1μA constant current, and the IC is latched when PFC_VSENSE > 2.922V is detected.

The PFC_OVP pin is a protective pin for when a PFC_VSENSE pin abnormality occurs. Like the PFC_VSENSE pin, the PFC_OVP pin detects the PFC output voltage, and has only an overvoltage protection function. The PFC_OVP pin detection voltage is the same as the PFC_VSENSE pin detection voltage, and sets the reference voltages from the same resistor ladder.

- **PFC overvoltage latch (PFC_OVP pin)**

  IC latch operation results when PFC_OVP > 2.922V (+B > 450V) is detected.

- **PFC_OVP pin open detection**

  When the PFC_VSENSE pin is open, the pin voltage is forcibly pulled up by the internally supplied 0.1μA constant current, and the IC is latched when PFC_VSENSE > 2.922V is detected as well as the PFC_VSENSE pin.

◆ **Resonant Controller Block**

10. Resonant Oscillator Block

10-1. Resonant Oscillator Circuit Block

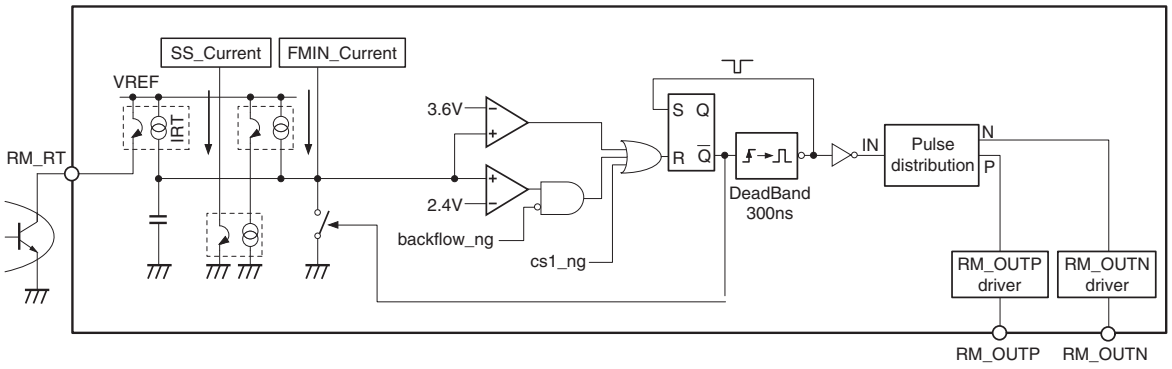


Fig. 11. Resonant Oscillator Equivalent Circuit

Fig. 11 shows the resonant oscillator circuit block equivalent circuit.
This circuit is the current mirror output of the current led from a photo-coupler or other device. The resonant oscillation frequency is determined by the current led from the RM_RT pin, the current from the minimum frequency setting circuit block, and the current from the soft start circuit block. The deadband width is fixed internally to 300ns.
The Fig. 12 graph shows the resonant oscillation frequency characteristics at a minimum frequency setting of 60kHz, relative to the current led from the RM_RT pin.

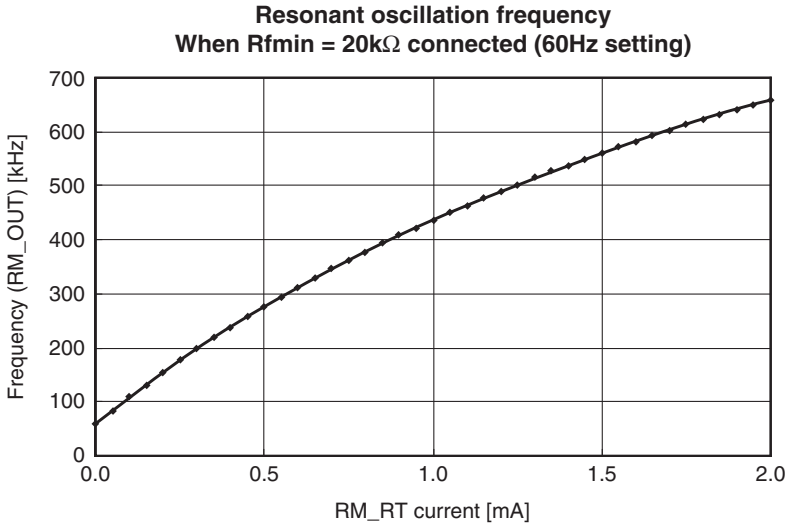


Fig. 12. Resonant Oscillation Frequency

10-2. Minimum Resonant Frequency Setting Circuit Block

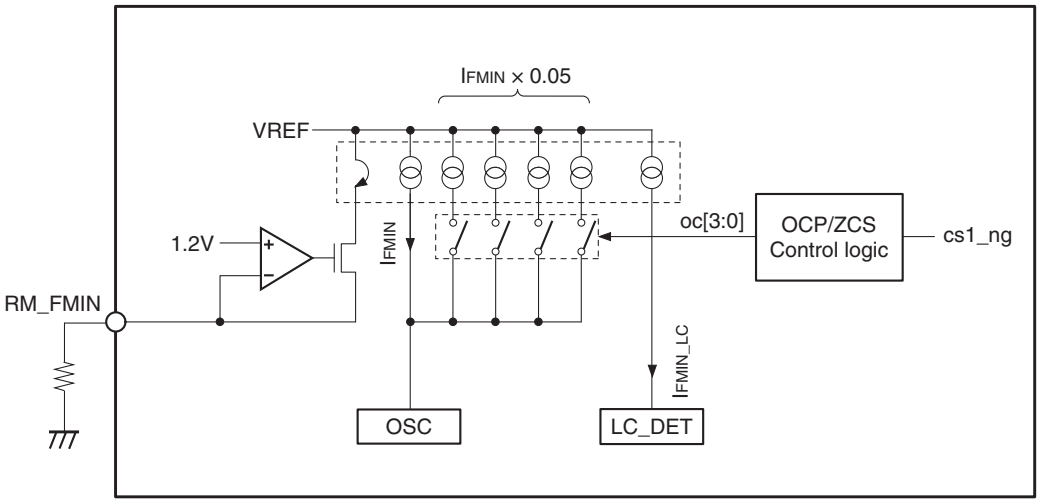


Fig. 13. Minimum Resonant Frequency Control Block Equivalent Circuit

Fig. 13 shows the minimum resonant frequency control block equivalent circuit.
The minimum resonant frequency can be set by externally connecting a resistor to the RM_FMIN pin.
The Fig. 14 graph shows the minimum frequency characteristics relative to the external resistor value.

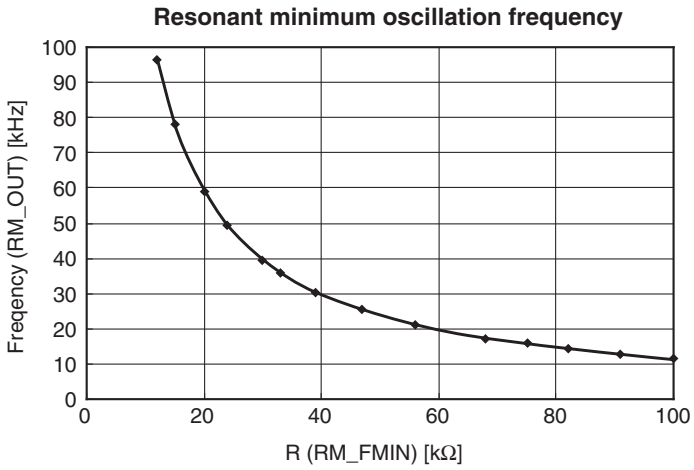


Fig. 14. Minimum Oscillation Frequency Setting

The minimum oscillation frequency decreases when the RM_FMIN pin is left open or the current led from the pin decreases. IC latch operation forcibly results when the current led from the pin is detected as being continuously 10μA or less (LC_DET) for 6s (2.1s × 3 times).

10-3. Resonant Soft Start Circuit Block

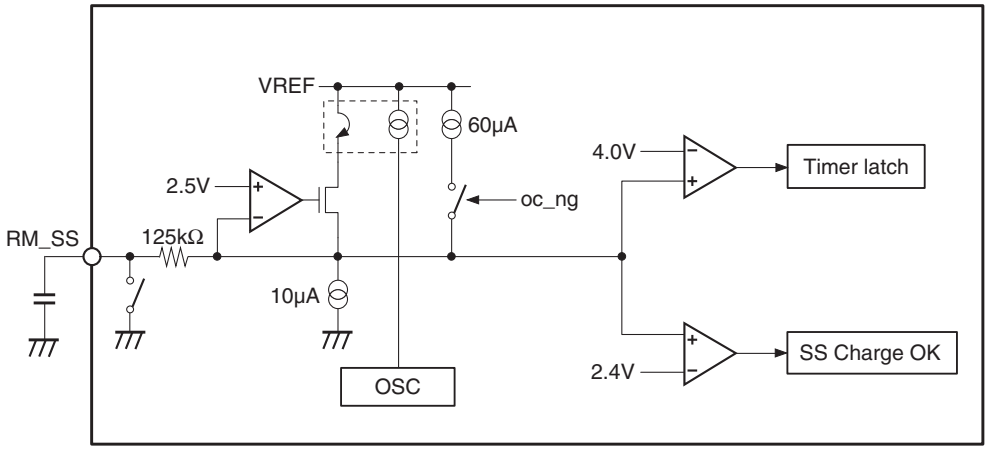


Fig. 15. Resonant Soft Start Circuit Block Equivalent Circuit

Fig. 15 shows the resonant soft start block equivalent circuit.
The resonant controller soft start circuit feeds back the current, determined by the internal 2.5V output, the internal 125kΩ resistor, and the time constant that corresponds to the external capacitor, to the oscillator of the resonant controller. This enables to start oscillation from a high frequency during resonant start-up. In addition, the maximum frequency during soft start is limited to 5 times (max.) the minimum frequency determined by the RM_FMIN pin external resistor.
Note that the frequency other than during soft start is not limited to 5 times the minimum frequency. In these cases the frequency is controlled according to the current led from the RM_RT pin.
The Fig. 16 graph shows the resonant oscillation frequency characteristics during soft start.

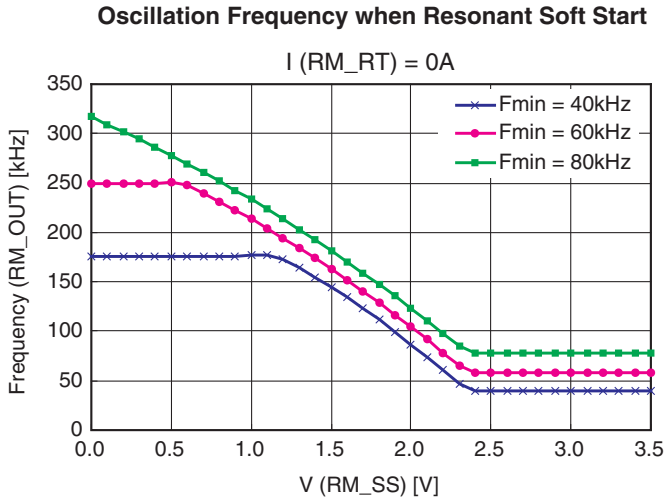


Fig. 16. Resonant Oscillation Frequency during Soft Start

11. Resonant Overcurrent Detection Circuit Block

11-1. Resonant Overcurrent Detection Circuit Block

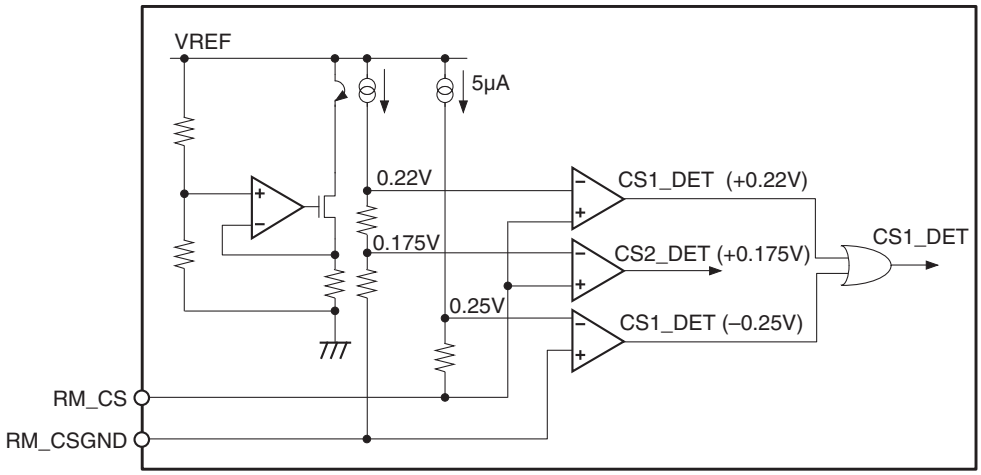


Fig. 17. Overcurrent Detection Block Equivalent Circuit

Fig. 17 shows the resonant overcurrent detection block equivalent circuit.
The voltage between the RM_CS and RM_CSGND pins is monitored, and overcurrents in both the positive (+0.22V) and negative (–0.25V) directions are detected according to RM_OUTP and RM_OUTN pin operation.
Operation in overcurrent detection mode is as shown in Fig. 18. When an overcurrent is detected, regardless of positive or negative direction, the output pulse is forcibly turned off by pulse-by-pulse control. In addition, when an overcurrent is detected, the minimum oscillation frequency is controlled to 1.2 times the setting value.
Thereafter, the minimum oscillation frequency limit changes in the order of 1.2 times → 1.15 times → 1.1 times → 1.05 times → 1.0 times the setting value with each dead band pulse, and control is performed to return to the original setting frequency with each pulse (4 steps). The minimum oscillation frequency is controlled to 1.2 times the setting value in this manner each time an overcurrent is detected again during the frequency limit period.
In addition, in overcurrent detection mode, the capacitor connected to the RM_SS pin is charged by approximately 50µA, and when the RM_SS pin voltage reaches 4.0V (128µs × 5 times), the IC is NG latched and the output goes off (both the RM_OUTP and RM_OUTN pins output Low). (Timer latch operation) 10µA is constantly discharged from the RM_SS pin to the inside of the IC, so when the overcurrent is canceled partway, the RM_SS pin is discharged until the clamp voltage is reached.

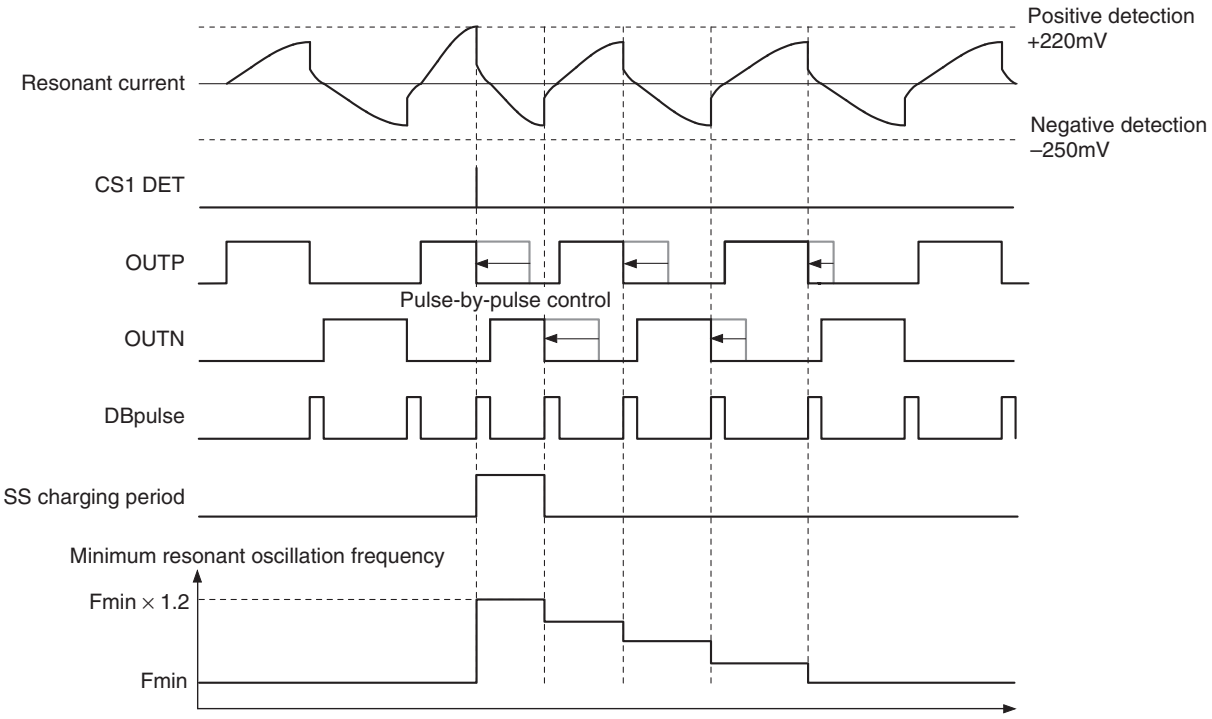


Fig. 18. Operating Waveform in Overcurrent Detection Mode

Continuous pulse overcurrent detection (CS2_DET: +0.175V detection) has the same circuit configuration as CS1_DET except for the negative side detector (Fig. 17). However, continuous overcurrent detection mode operation differs from the operation shown in Fig. 18, and instead normal operation continues. When CS2 overcurrent detection continues for approximately 10s (set up by 2.1s × 5 times), NG latch results and the IC forcibly stopped. When CS2 overcurrent is not detected for even one cycle during the approximately 10s count, the counter is reset. Then, when an overcurrent is detected again, the 10s counter starts from zero.

11-2. Resonant Reverse Current Detection Circuit Block

To prevent out of resonance during resonant converter start-up, the CXA3809M performs control to widen the output pulse width up to 1.5 times (max.) the normally controlled pulse width until the resonant current inverts. (See “Fig. 11. Resonant Oscillator Equivalent Circuit”.) For example, when the resonant current is negative while RM_OUTP is High output, the backflow_ng signal is High output, and is limited at a peak value of up to 3.6V (max.) instead of the normal 2.4V peak value limit cycle.
This function shifts to the next cycle after the resonant current reaches the positive side when RM_OUTP is High output, or the negative side when RM_OUTN is High output. The out of resonance prevention detection (rise) function is valid only during resonant converter start-up, and goes OFF after 4 RM_OUTP pulses and 4 RM_OUTN pulses (8 dead band pulses) have been output. Fig. 19 shows the resonant reverse current detection circuit block equivalent circuit.

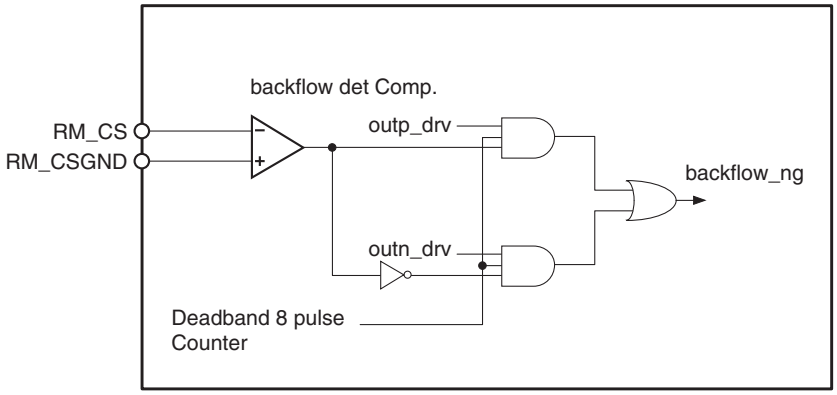


Fig. 19. Resonant Back Flow Detection Block Equivalent Circuit

12. Resonant Circuit Stop Voltage Detection Block

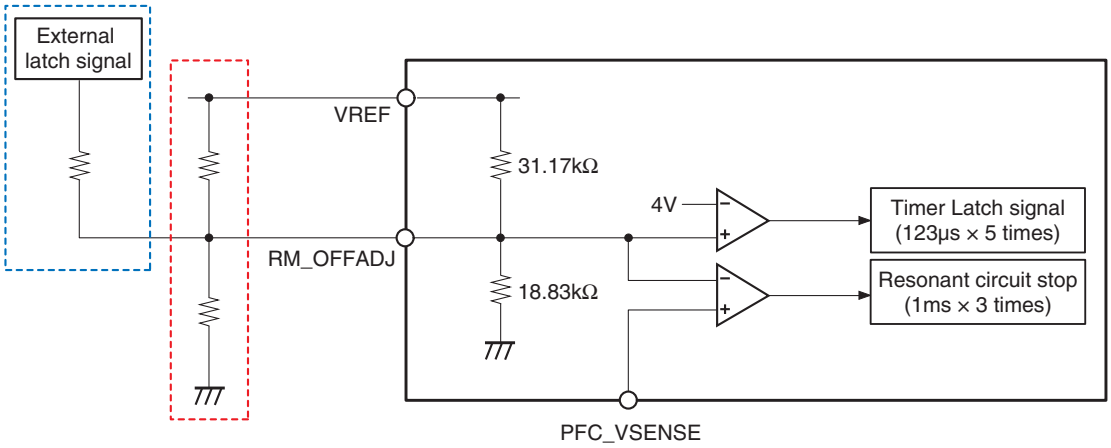


Fig. 20. RM_OFFADJ Pin Internal Equivalent Circuit

Fig. 20 shows the RM_OFFADJ pin internal equivalent circuit.
The RM_OFFADJ pin normally outputs 1.883V. Resonant circuit stop is controlled by comparing the PFC_VSENSE pin with the RM_OFFADJ pin, so the resonant circuit stop voltage can be changed by adding the circuit enclosed by the red dotted line in Fig. 20, and changing the RM_OFFADJ pin voltage.

Note) When the PFC output voltage is set to 385V (PFC_VSENSE = 2.5V) and the RM_OFFADJ pin is open, the resonant circuit is stopped when the PFC output voltage falls to 290V or less (1ms × 5 times).

The RM_OFFADJ pin has an error latch detection function that activates at 4.0V or more, so the IC can be forcibly set to latch operation using the secondary side overvoltage detection or other signal by externally adding the circuit enclosed by the blue dotted line in Fig. 20.

13. NG Latch Operation

◆ PFC overvoltage latch

Latch operation results after PFC_VSENSE > 2.922V (+B > 450V) is detected and set up by 1ms × 3 times.

Note) PFC_VSENSE > 2.700V (+B > 416V) overvoltage detection does not result in latch operation, and PFC output stops.

The PFC_OVP pin also performs overvoltage latch operation using the same detection sequence as PFC_VSENSE.

◆ PFC continuous overcurrent detection latch

IC latch operation results when a pin abnormality such as PFC_VAO pin open or PFC_TONMAX pin short-circuited to GND occurs, and the overcurrent detection state is continuously detected due to abnormal PFC oscillation. When a PFC overvoltage outside the C range is detected 4 times or more per commercial half cycle during AC detection operation, this is counted as one NG time. Latch operation results when the 2.1s counter detects this NG state 5 consecutive times.

◆ PFC not operating detection latch

When a pin abnormality such as PFC_OUT pin open occurs, the AC input voltage is high, and the load is light, the PFC output voltage (+B voltage) maintains the high state, and the resonant circuit continues to operate. To avoid this phenomenon, latch operation results when PFC_VSENSE < 2.4V (+B < 370V) is continuously detected for 2.1s × 5 times.

◆ Resonant overcurrent timer latch

When RM_CS > 0.22V or RM_CS < –0.25V is detected, the RM_SS pin is charged by a charging current of 50μA. Latch operation results after RM_SS > 4.0V is detected and set up by 128μs × 5 times.

◆ Resonant continuous overcurrent latch

Latch operation results after RM_CS > 0.175V is detected continuously and set up by 2.1s × 5 times.

◆ TSD (IC overheat) latch

Latch operation results after a chip temperature of approximately 140°C is detected and set up by 128μs × 5 times.

◆ RM_OFFADJ latch

Latch operation results after RM_OFFADJ > 4.0V is detected and set up by 128μs × 5 times.

◆ Other latch

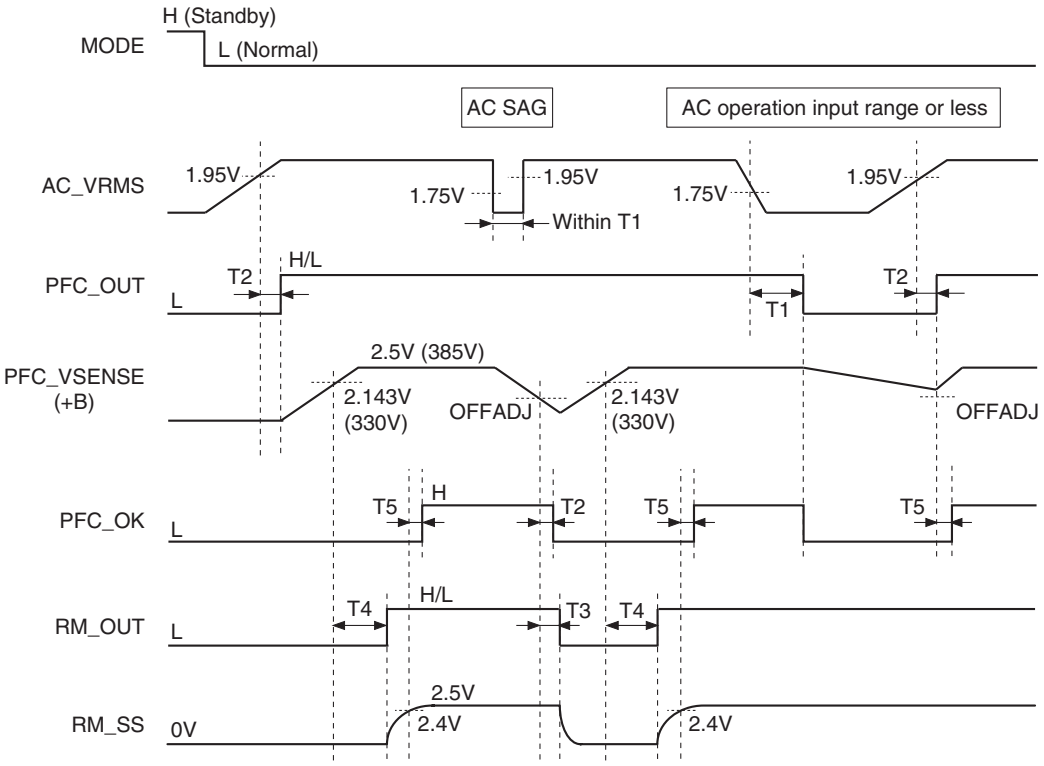
Latch operation results after any of the following operations are detected and set up by 2.1s × 3 times.

- VREF_OVLO detection: 5.5V or more
- PFC_VAO pin overcurrent detection: 80μA or more
- PFC_ZCD clamp circuit overcurrent detection: +6.0mA or more, –6mA or less
- PFC_VSENSE short-circuit detection: 0.3V or less
- RM_FMIN pin low current: 10μA or less

Circuit operation stops after NG latch, but the VREF pin continues to output High, and the AC detection function remains enabled. In addition, PFC_OK outputs Low. NG latch is canceled by transitioning to standby mode. However, during TSD latch the VREF pin outputs Low, and the TSD latch state is canceled only by turning the IC power off and on again, or by detecting VCC UVLO (VCC < 9.6V).

Timing Chart

1. PFC → Resonant controller startup sequence



T1: Corresponds to 66ms × 8 times
T2: Corresponds to 1ms × 3 times
T3: Corresponds to 1ms × 5 times
T4: Corresponds to 16ms × 4 times
T5: Corresponds to 4.1ms × 3 times

Fig. 21. Startup Waveform

Note) The +B voltage shows an example of setting that PFC_VSENSE = 2.5V when +B = 385V.

2. Overvoltage detection

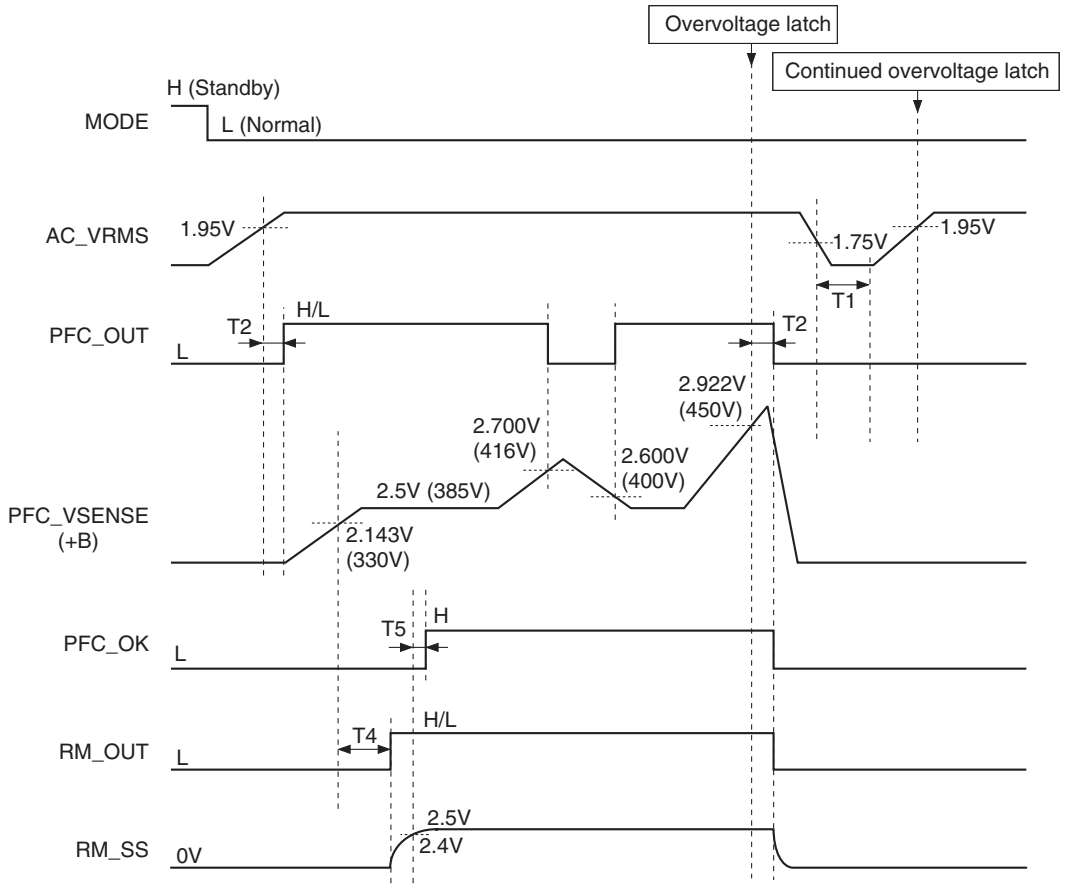
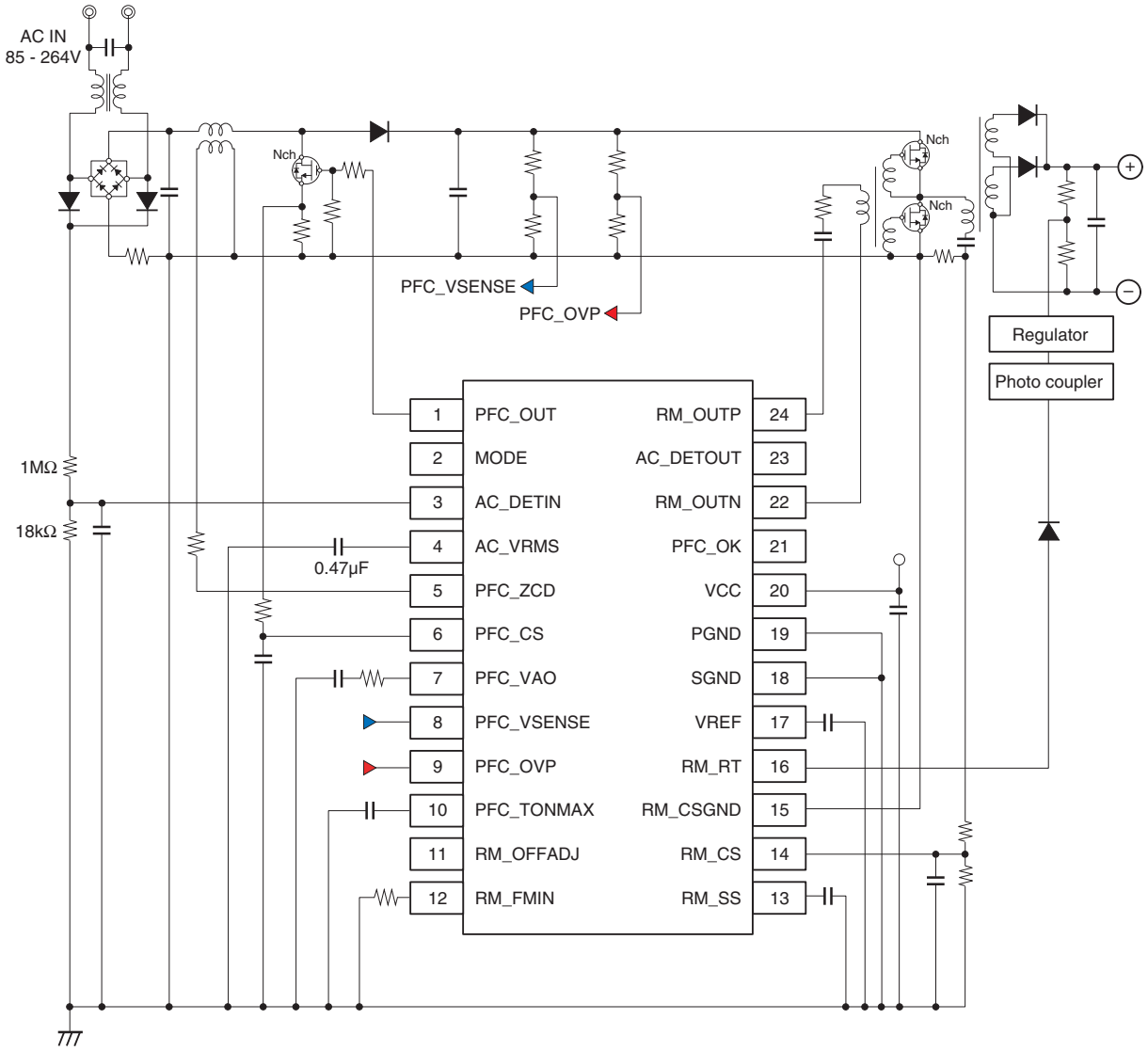


Fig. 22. Operating Waveform with Overvoltage

Note) The +B voltage shows an example of setting that PFC_VSENSE = 2.5V when +B = 385V.

Application Circuit

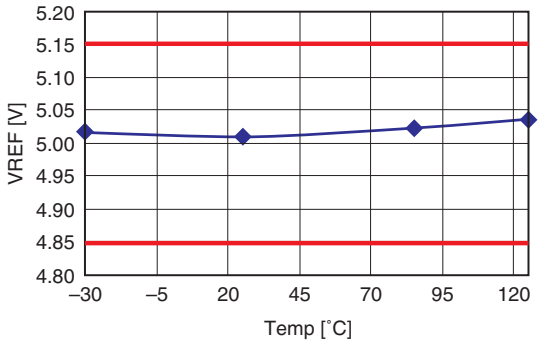


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

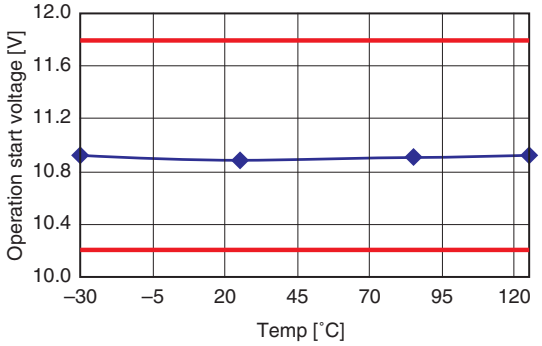
Fig. 23. Application Circuit

Example of Representative Characteristics

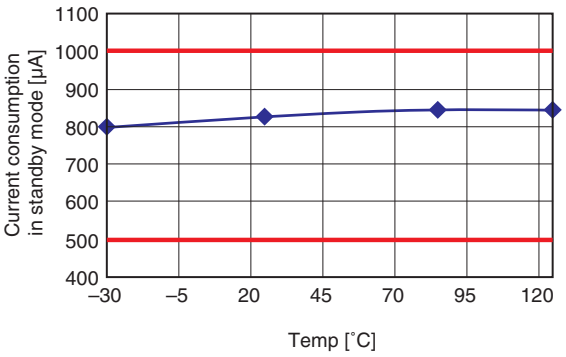
VREF output voltage
VCC = 12V



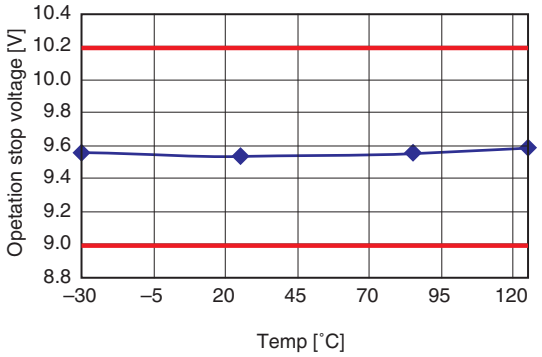
VCC_UVLO opetation start voltage



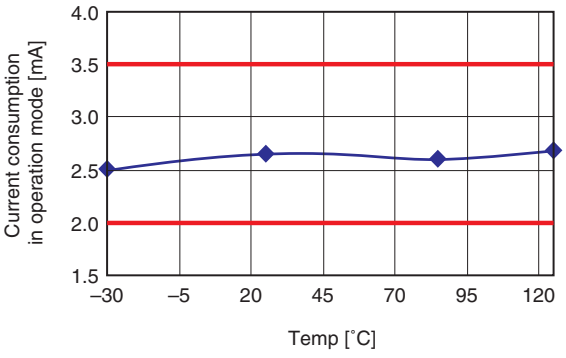
Current comsumption in standby mode
VCC = 12V



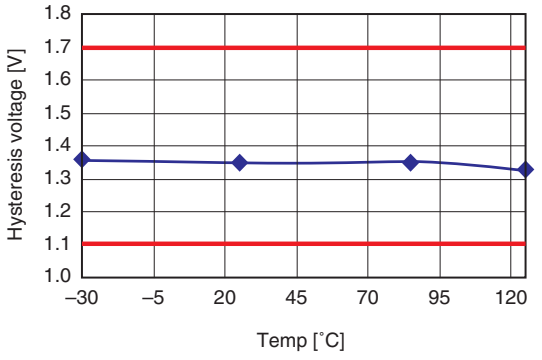
VCC_UVLO opetation stop voltage



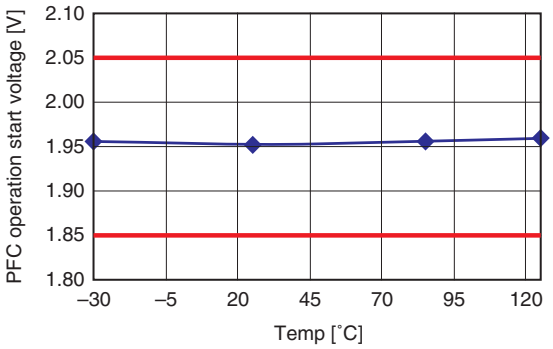
Current comsumption in operation mode
VCC = 12V No Switching



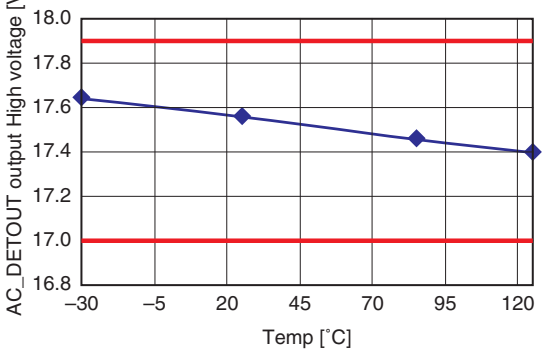
VCC_UVLO hysteresis voltage



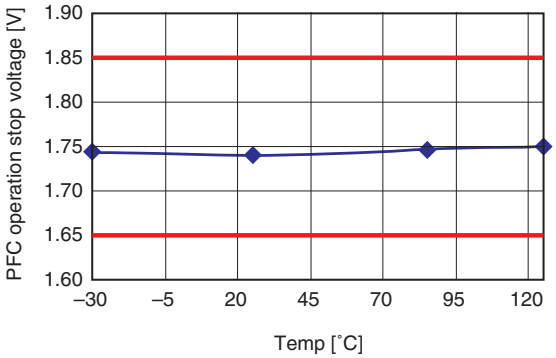
PFC operation start voltage



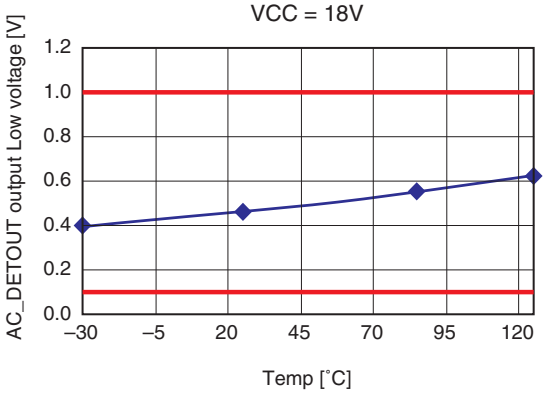
AC_DETOUT output High voltage
VCC = 18V



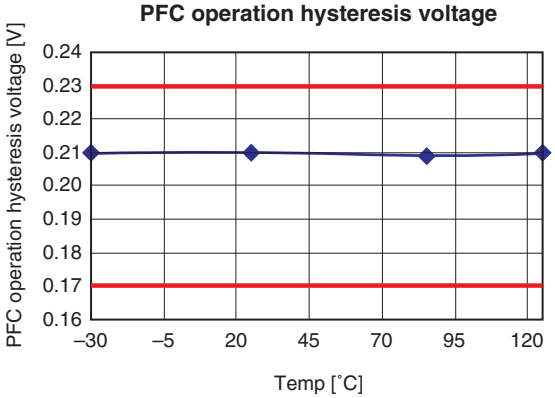
PFC operation stop voltage



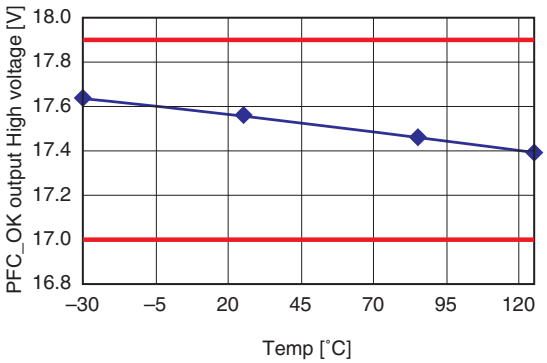
AC_DETOUT output Low voltage
VCC = 18V



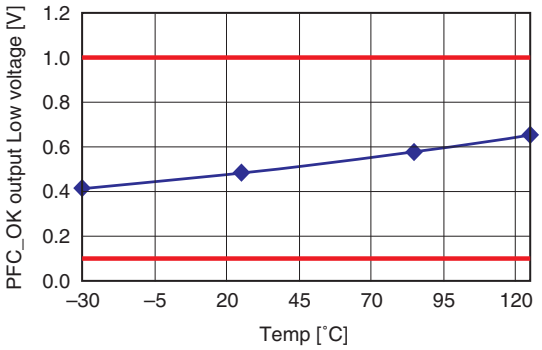
PFC operation hysteresis voltage



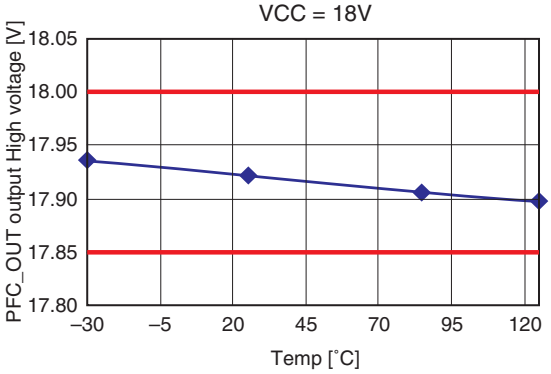
PFC_OK output High voltage
VCC = 18V



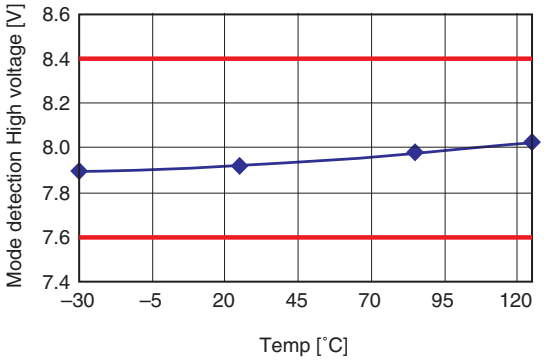
PFC_OK output Low voltage
VCC = 18V



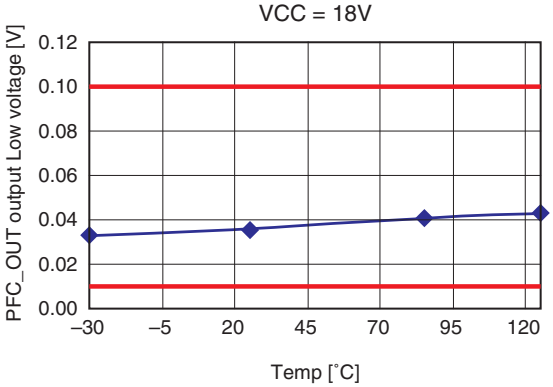
PFC_OUT output High voltage
VCC = 18V



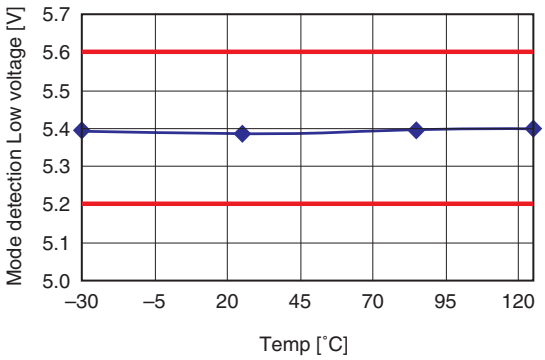
Mode detection High voltage



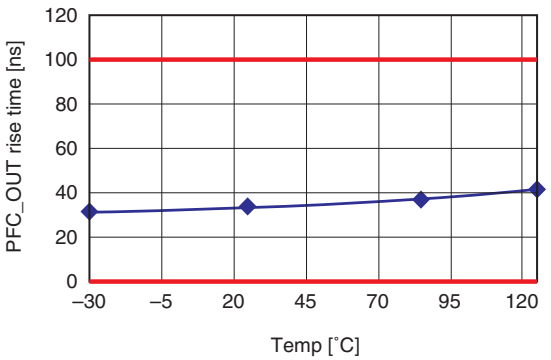
PFC_OUT output Low voltage
VCC = 18V



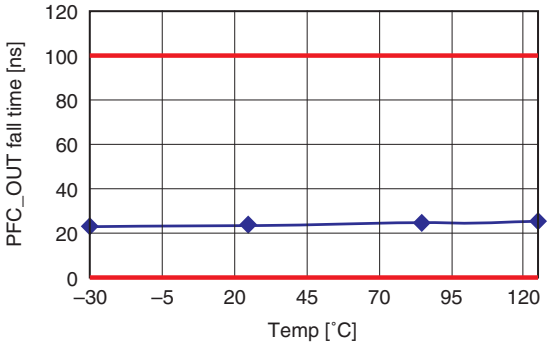
Mode detection Low voltage



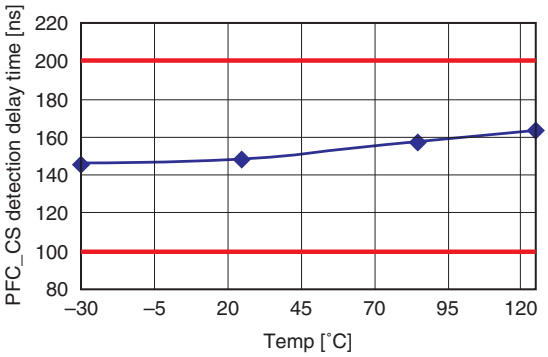
PFC_OUT rise time
VCC = 18V



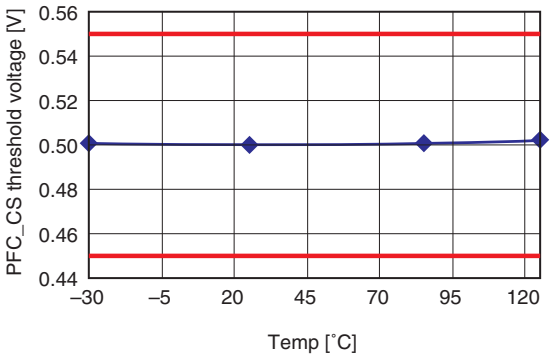
PFC_OUT fall time
VCC = 18V



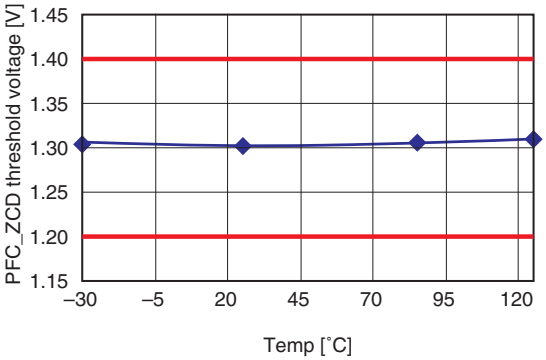
PFC_CS detection delay time



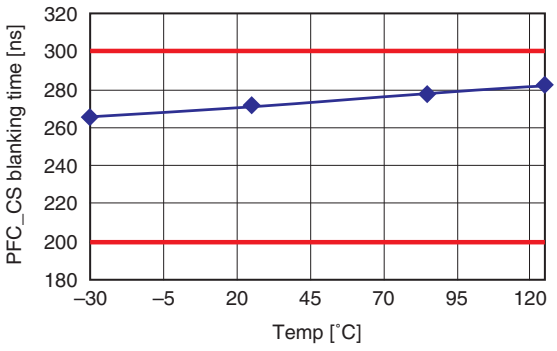
PFC_CS threshold voltage



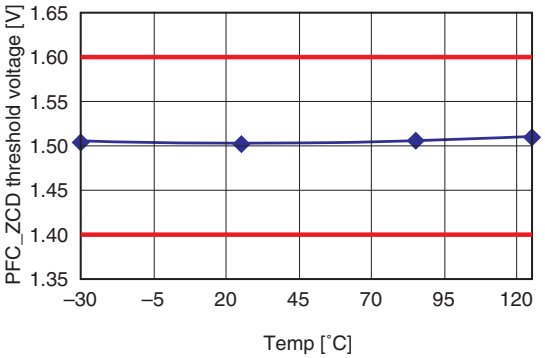
PFC_ZCD threshold voltage 1.3V



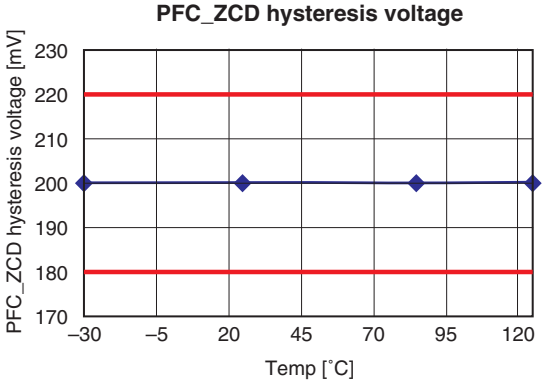
PFC_CS blanking time



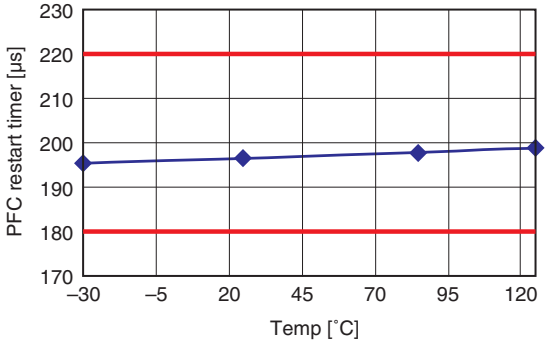
PFC_ZCD threshold voltage 1.5V



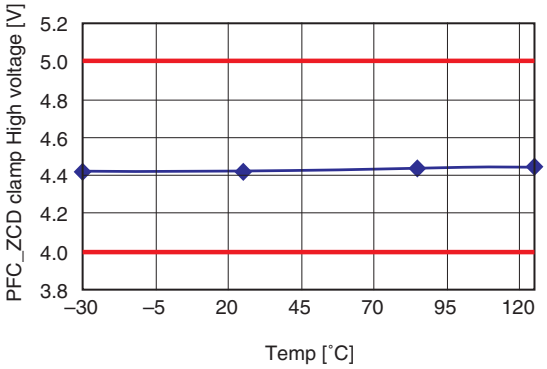
PFC_ZCD hysteresis voltage



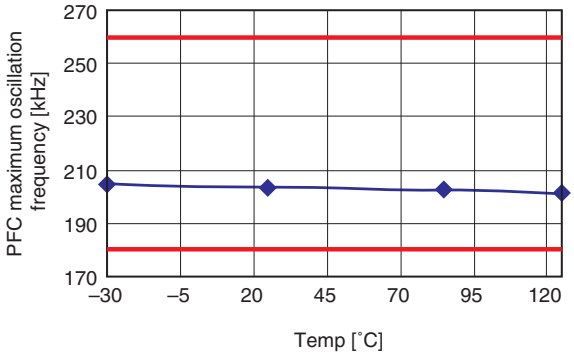
PFC restart timer



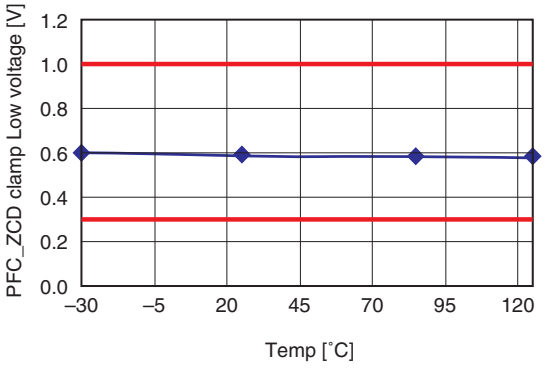
PFC_ZCD clamp High voltage



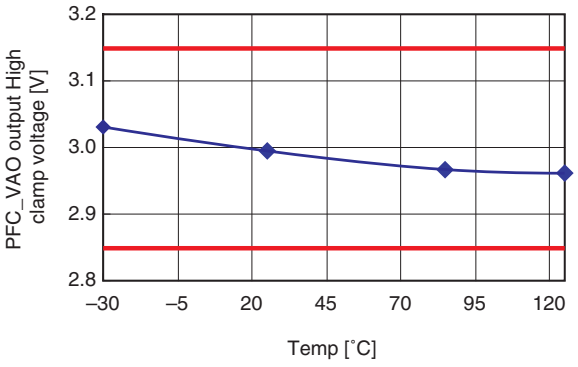
PFC maximum oscillation frequency



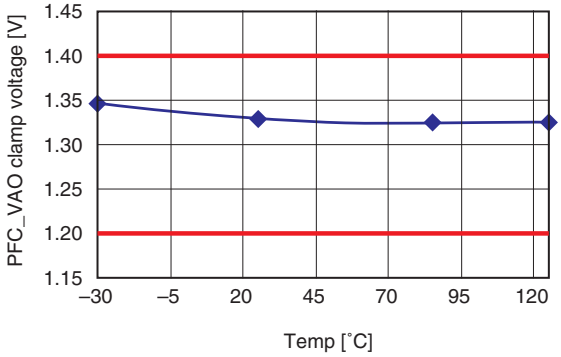
PFC_ZCD clamp Low voltage



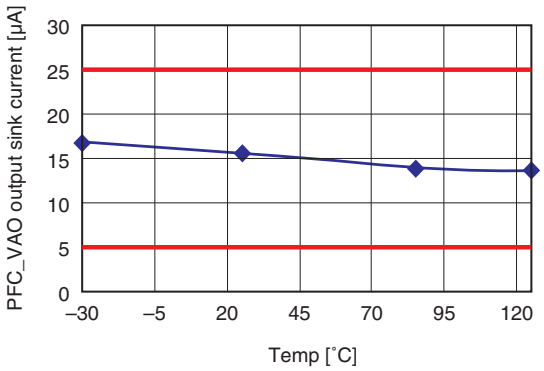
PFC_VAO output High clamp voltage



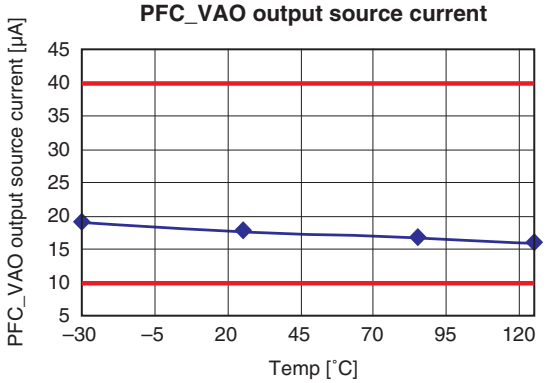
PFC_VAO clamp voltage



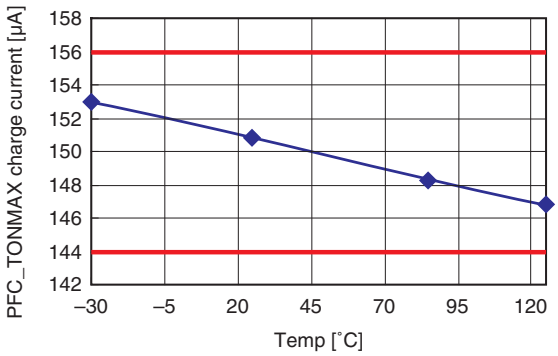
PFC_VAO output sink current



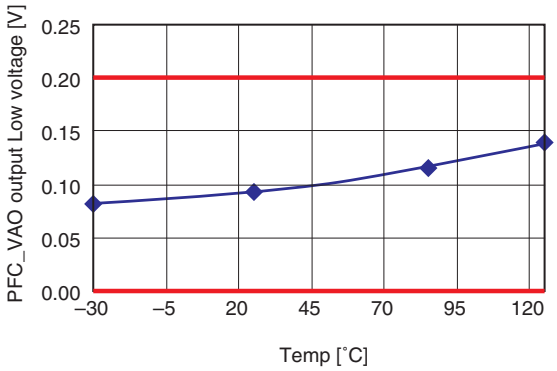
PFC_VAO output source current



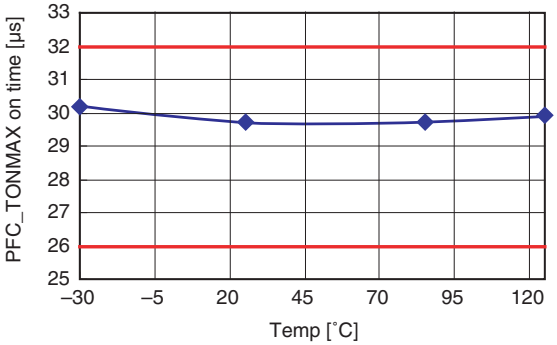
PFC_TONMAX charge current



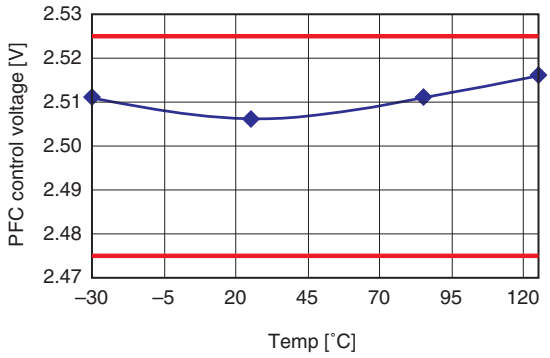
PFC_VAO output Low voltage



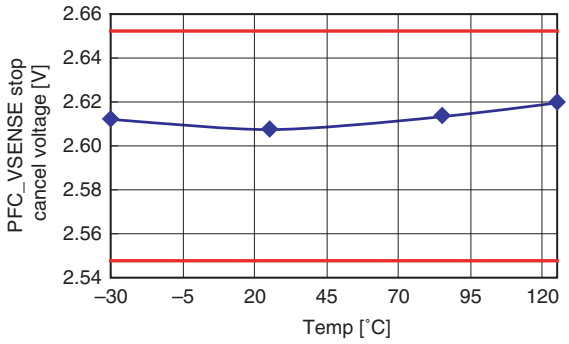
PFC_TONMAX on time



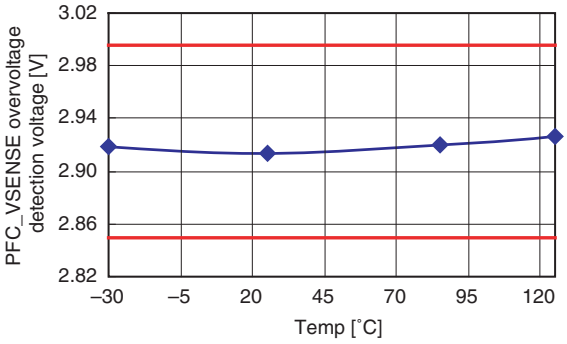
PFC control voltage



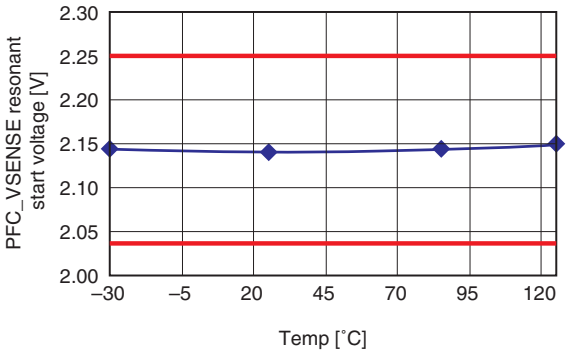
PFC_VSENSE stop cancel voltage



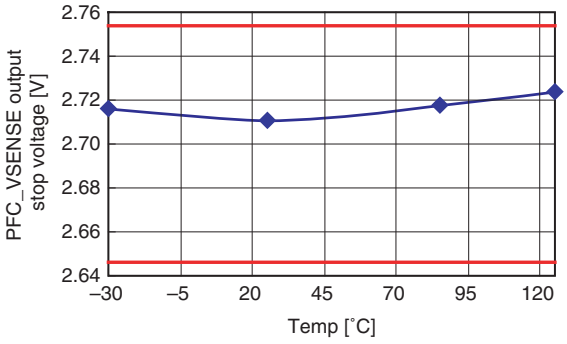
PFC_VSENSE overvoltage detection voltage



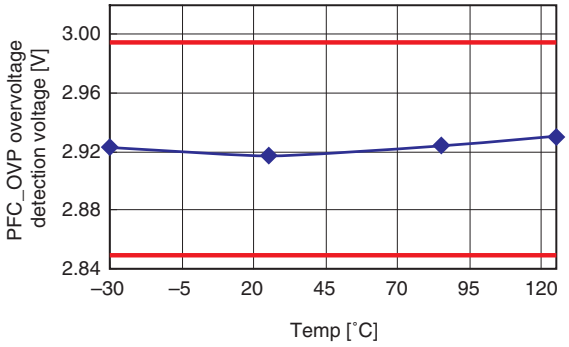
PFC_VSENSE resonant start voltage



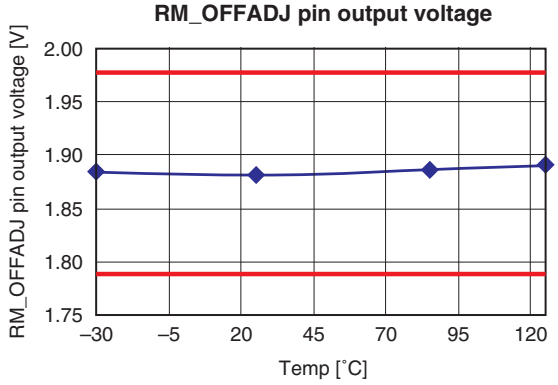
PFC_VSENSE output stop voltage



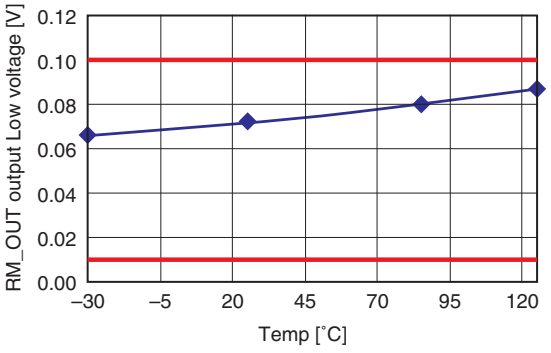
PFC_OVP overvoltage detection voltage



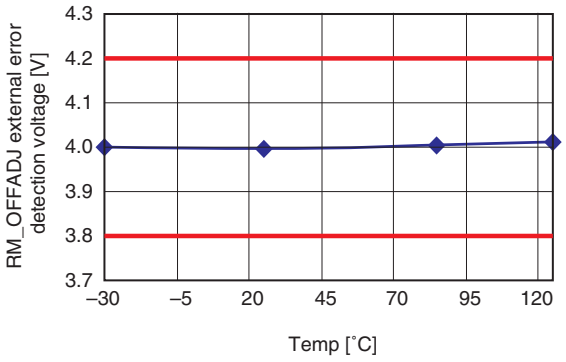
RM_OFFADJ pin output voltage



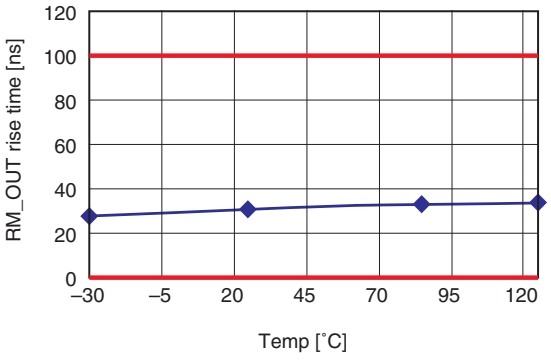
RM_OUT output Low voltage
VCC = 18V



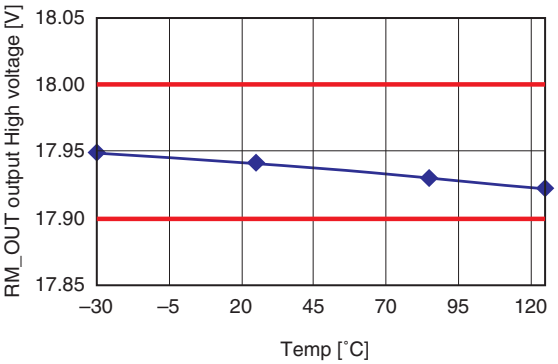
RM_OFFADJ external error detection voltage



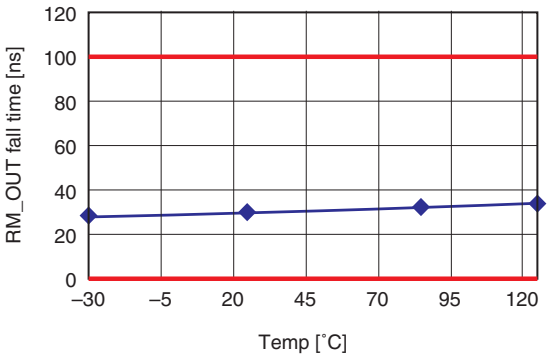
RM_OUT rise time
VCC = 18V



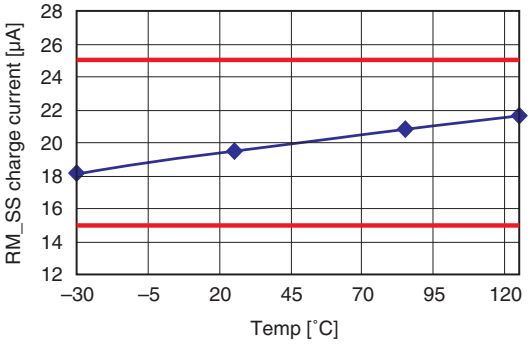
RM_OUT output High voltage
VCC = 18V



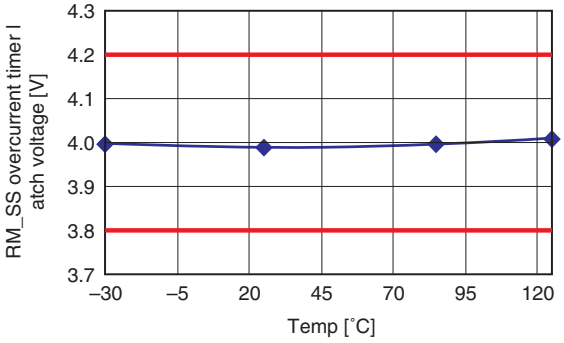
RM_OUT fall time
VCC = 18V



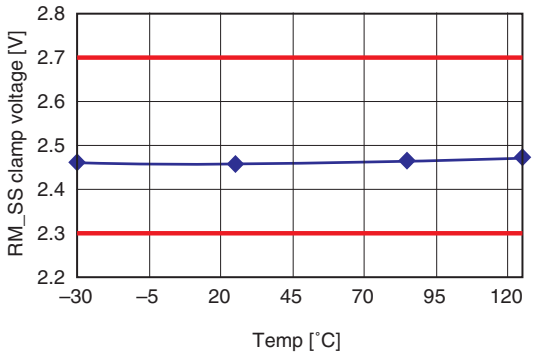
RM_SS charge current



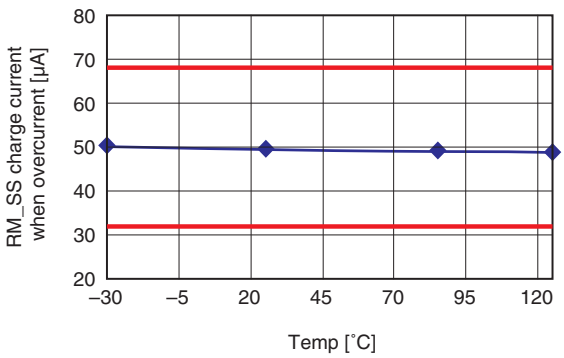
RM_SS overcurrent timer latch voltage



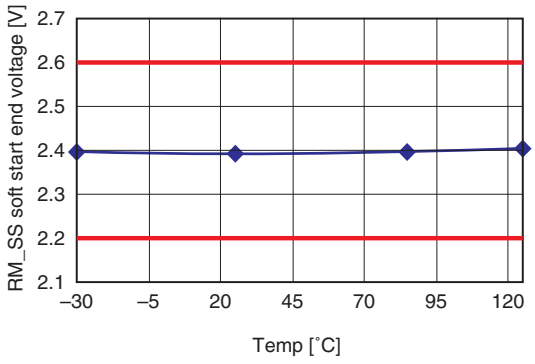
RM_SS clamp voltage



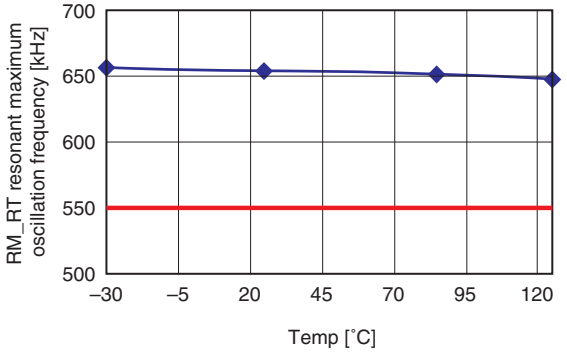
RM_SS charge current when overcurrent



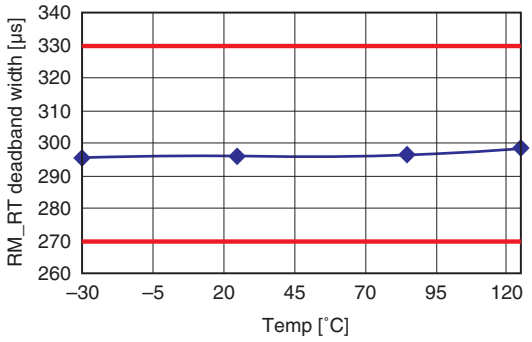
RM_SS soft start end voltage



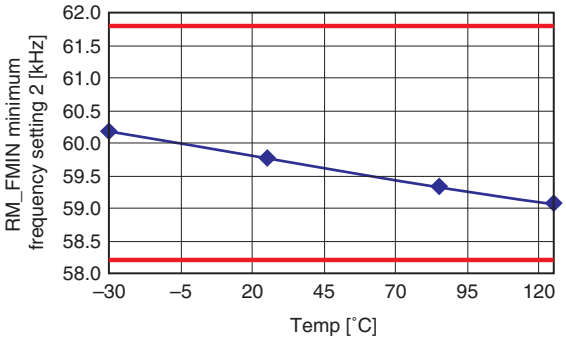
RM_RT resonant maximum oscillation frequency



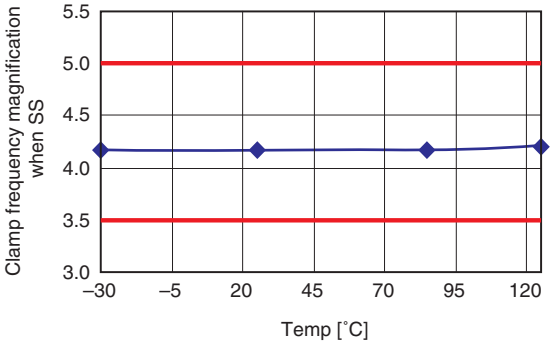
RM_RT deadband width



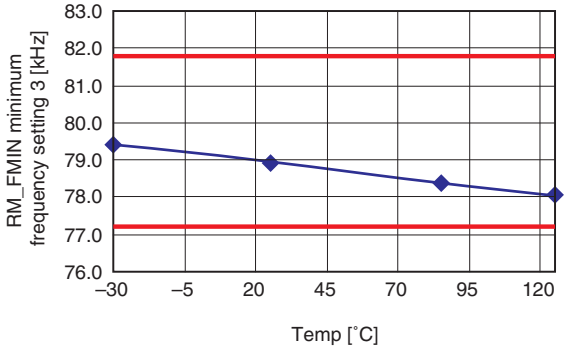
RM_FMIN minimum oscillation frequency setting 2



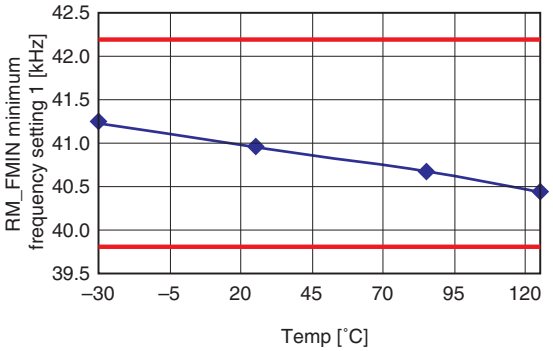
Clamp frequency magnification when RM_RT soft start



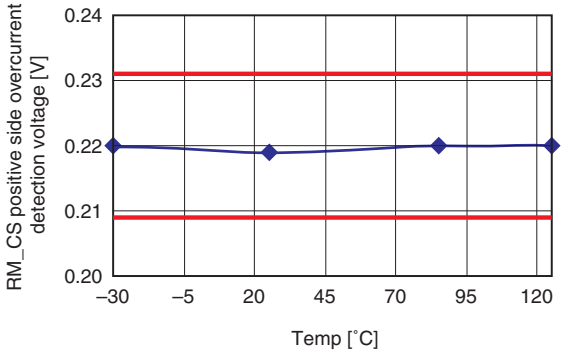
RM_FMIN minimum oscillation frequency setting 3



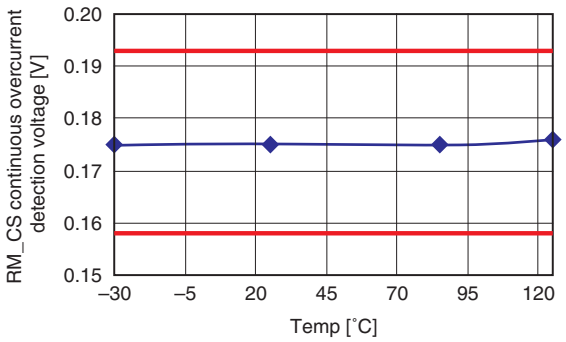
RM_FMIN minimum oscillation frequency setting 1



RM_CS positive side overcurrent detection voltage

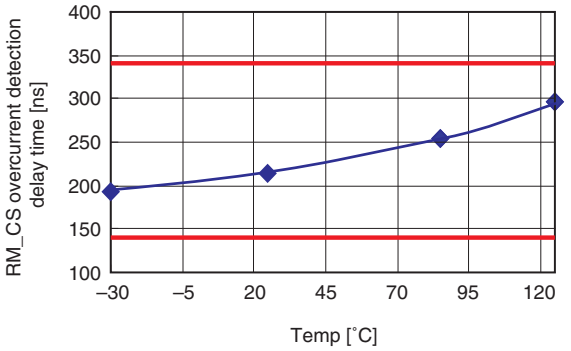


RM_CS continuous overcurrent detection voltage

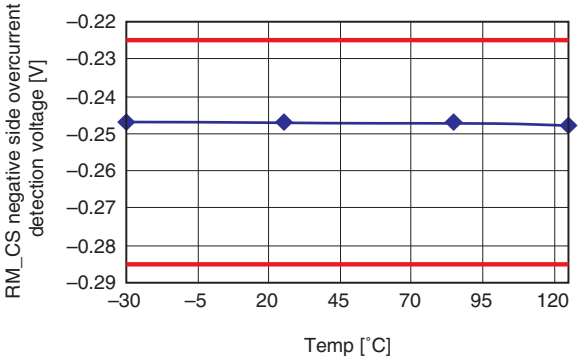


RM_CS overcurrent detection delay time (sine wave input: 90kHz)

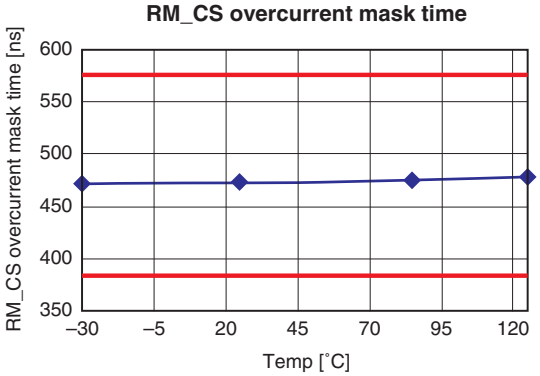
Reference data (design assurance)



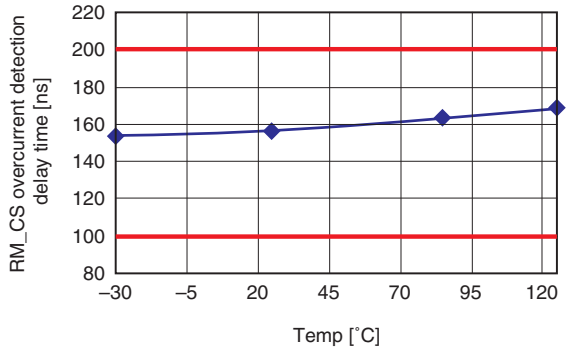
RM_CS negative side overcurrent detection voltage



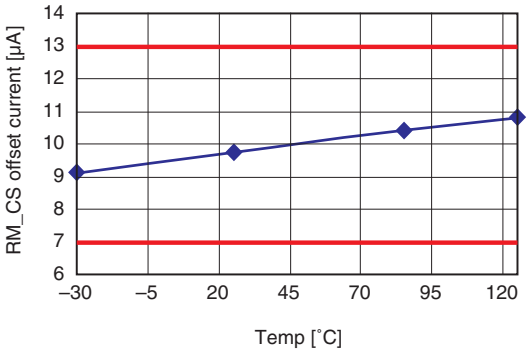
RM_CS overcurrent mask time



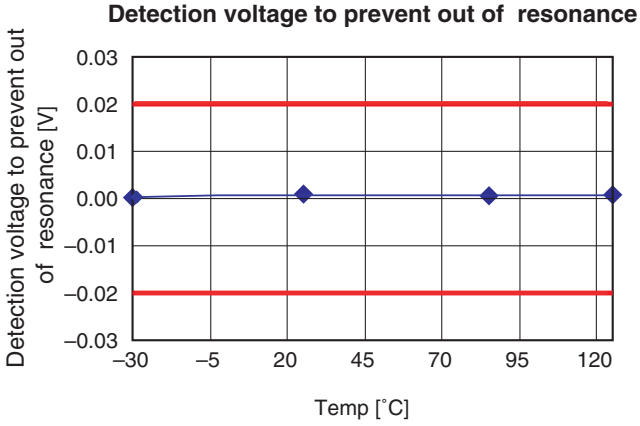
RM_CS overcurrent detection delay time (rectangular wave input)



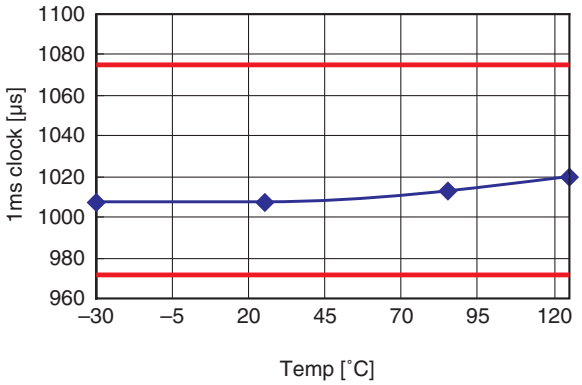
RM_CS offset current



Detection voltage to prevent out of resonance



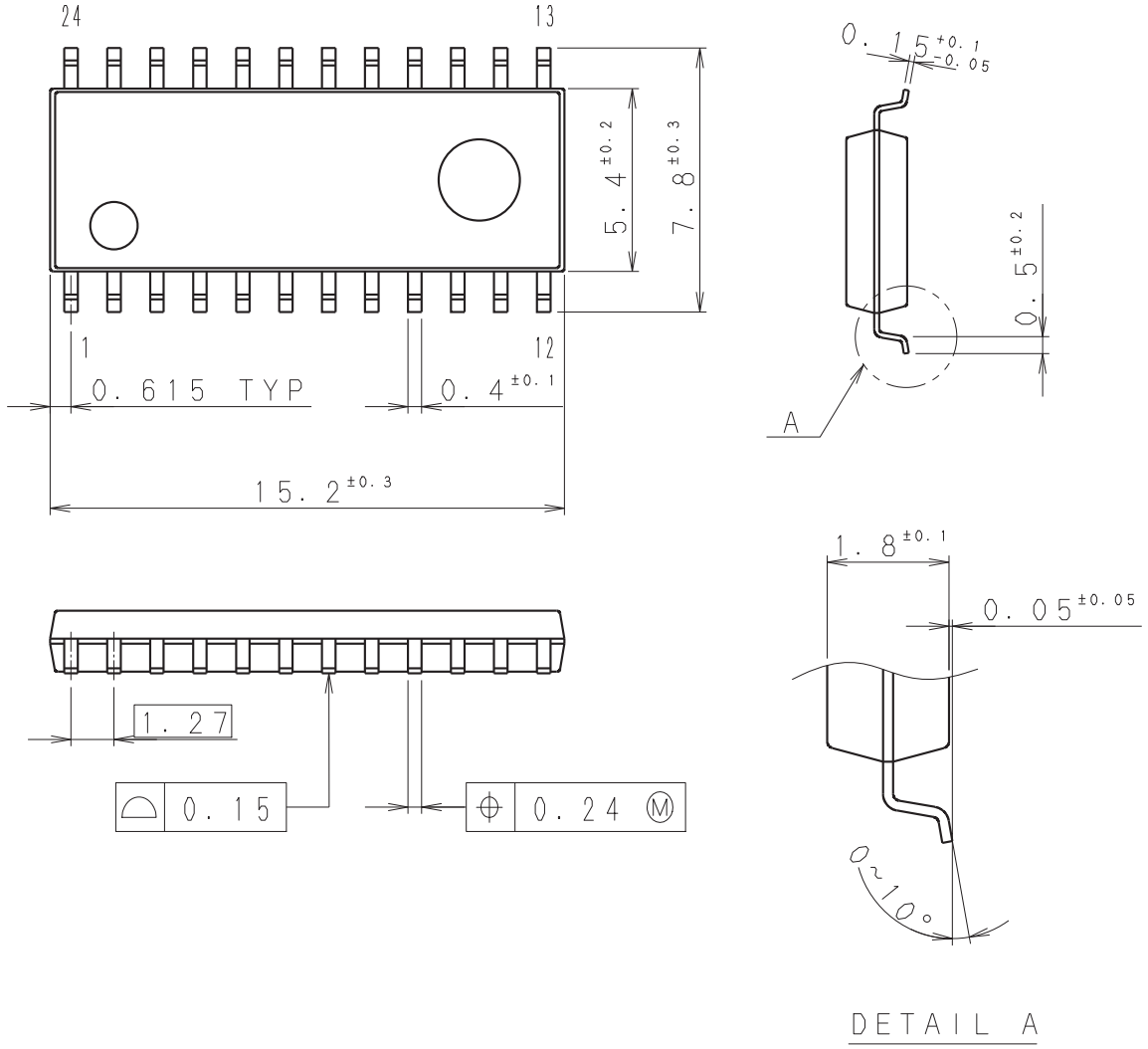
1ms clock



Package Outline

(Unit: mm)

24PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-24P-L391
JEITA CODE	P-SOP24-15X7.9-1.27
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	0.32g

AP-2000-24MAN1 Rev. 0