Dual N-Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4948 is the Dual N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 53\ m\Omega$ @VGS=10V
- $R_{DS(ON)} \leqq 78\ m\Omega$ @VGS=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

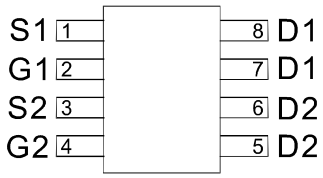
APPLICATIONS

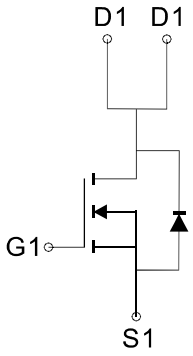
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

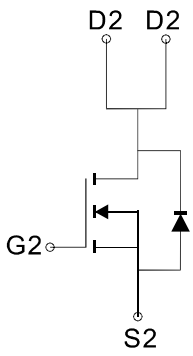
(SOP-8)

Top View





N-Channel MOSFET



N-Channel MOSFET

Ordering Information: ME4948 (Pb-free)

ME4948-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		V_{DSS}	60		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current(Tj=150℃)	T_A=25℃	I_D	4.5		A
	T_A=70℃		3.6		
Pulsed Drain Current		I_{DM}	18		A
Single Pulse Avalanche Energy (L=0.1mH,I_{AS}=8A)		E_{AS}	3.2		mJ
Maximum Power Dissipation	T_A=25℃	P_D	1.67		W
	T_A=70℃		1.07		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	Steady State	75	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

Dual N-Channel 60-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

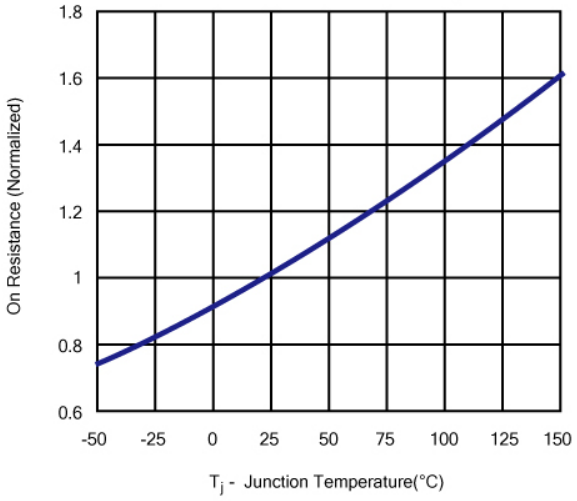
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
		V_{DS}=60V, V_{GS}=0V,T_J=55℃			10	
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 4.5A		45	53	mΩ
		V_{GS}=4.5V, I_D= 3.6A		60	78	
V_{SD}	Diode Forward Voltage	I_S=2.0A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_D=4.5A		16		nC
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=4.5V, I_D=4.5A		8.7		
Qgs	Gate-Source Charge			4.4		
Qgd	Gate-Drain Charge			3.6		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		560		pF
Coss	Output Capacitance			73		
Crss	Reverse Transfer Capacitance			22		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, R_L =15Ω, V_{GEN}=10V, R_G=1Ω		12		ns
tr	Turn-On Rise Time			16		
$t_{d(off)}$	Turn-Off Delay Time			34		
tf	Turn-Off Fall Time			4		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

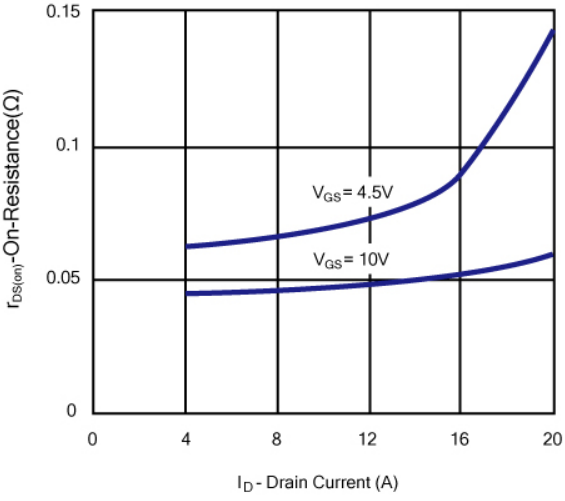
b. Matsuki reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J =25℃ Noted)

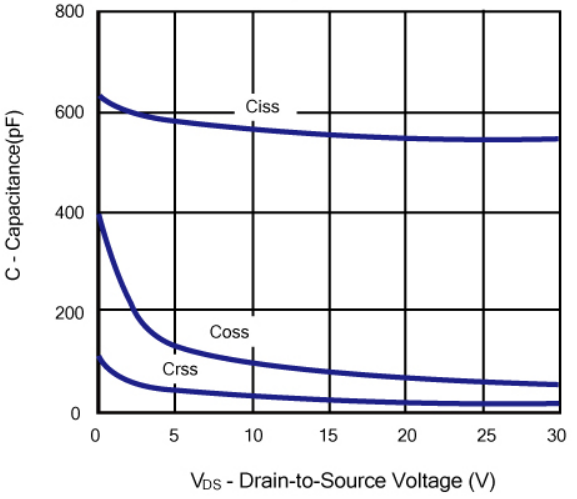
On Resistance vs. Junction Temperature



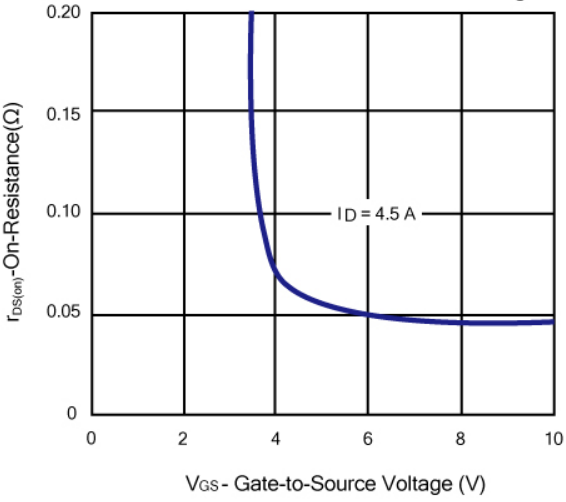
On-Resistance vs. Drain Current



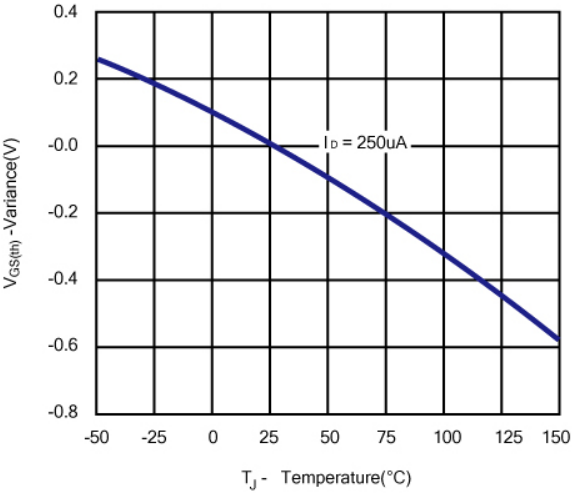
Capacitance



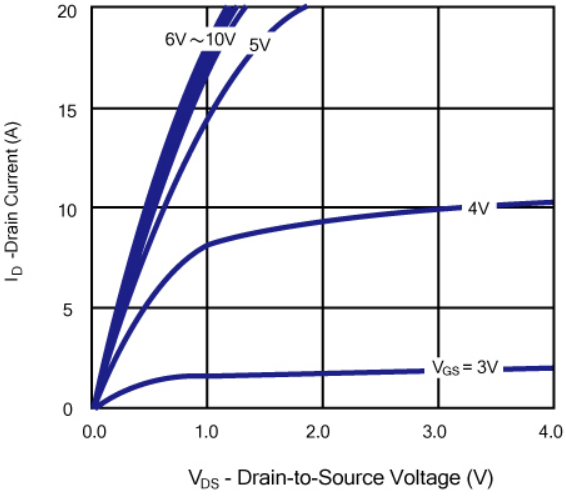
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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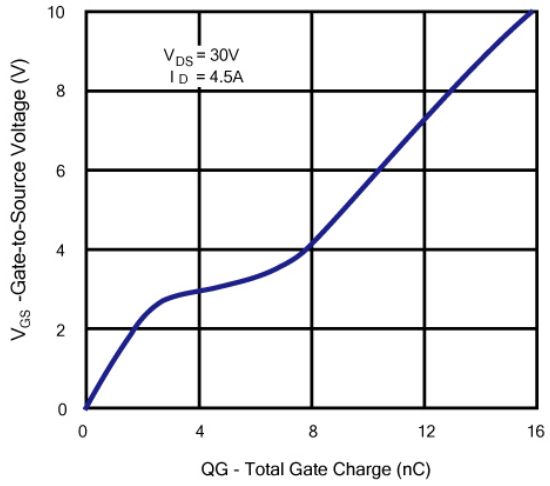
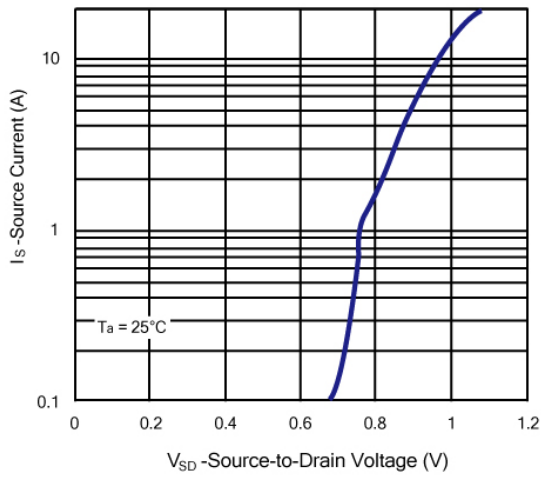
Typical Characteristics (T_J =25℃ Noted)

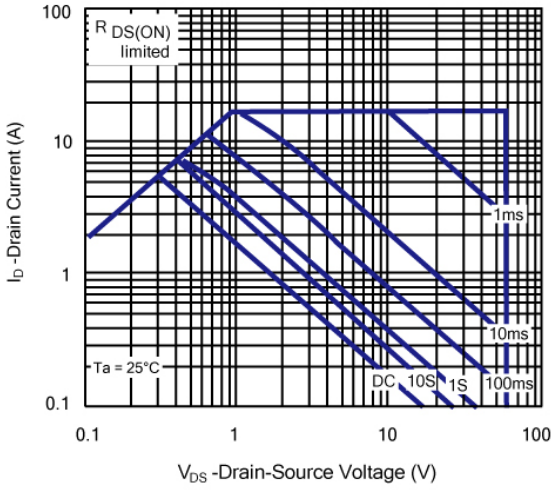
Gate Charge



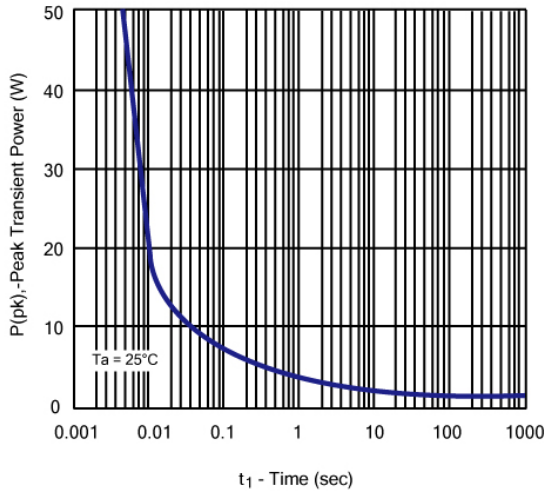
On-Resistance vs. Drain Current



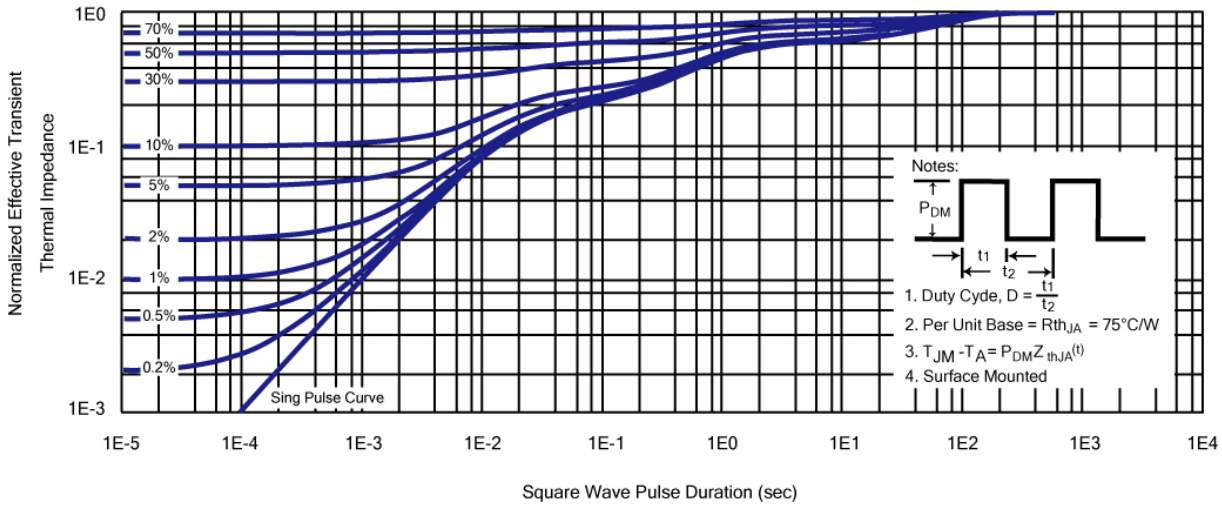
Maximum Forward Biased Safe Operating Area



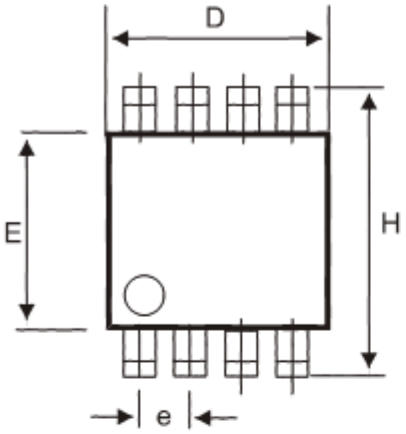
Single Pulse Maximum Power Dissipation

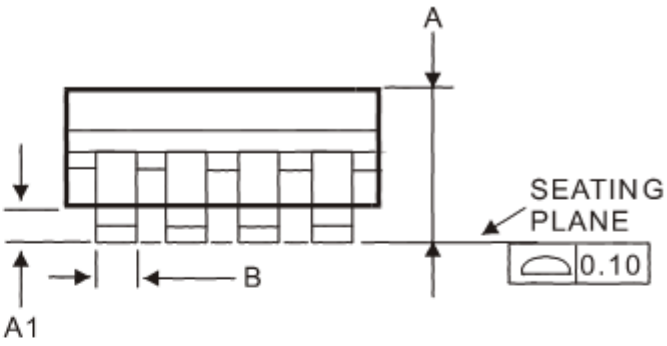


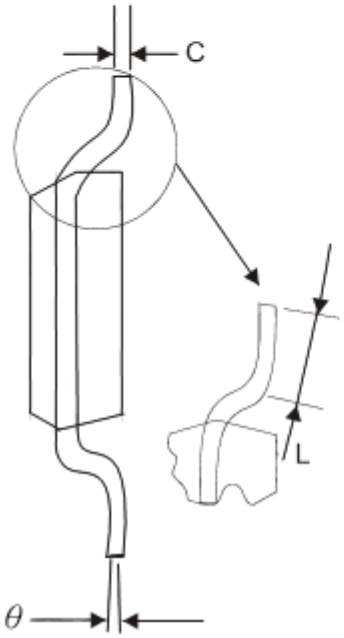
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.