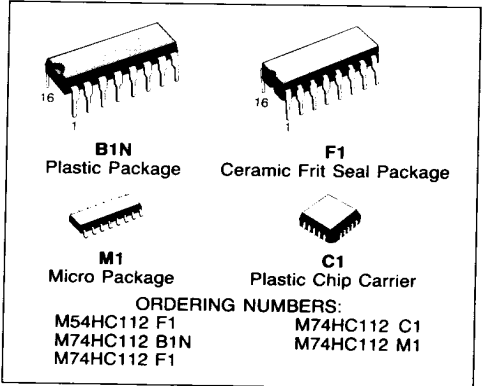


DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
 $f_{MAX} = 59 \text{ MHz (Typ.) at } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 2 \mu\text{A at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = |I_{OL}| = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ to } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS112

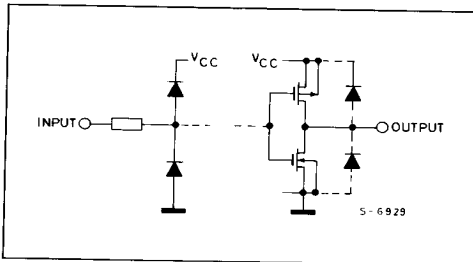


DESCRIPTION

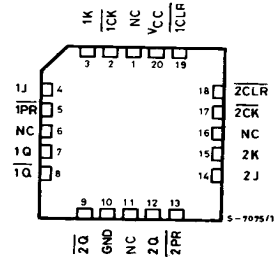
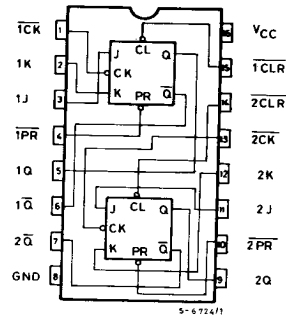
The M54/74HC112 is a high speed CMOS DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR fabricated in silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC112/M74HC112 dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs for each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will function as shown in the truth table. Input data is transferred to the input on the negative going edge of the clock pulse. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



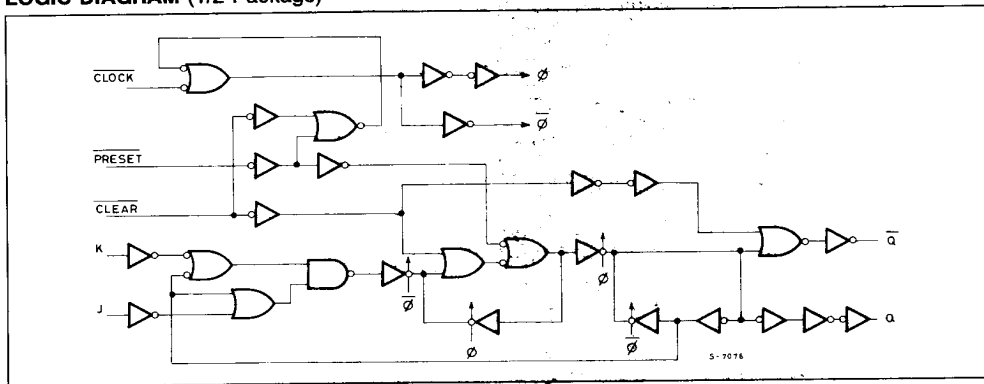
NC =
No Internal
Connection

TRUTH TABLE

INPUTS					OUTPUT		FUNCTION
CLR	PR	J	K	CK	Q	Q̄	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Q _n	Q̄ _n	NO CHANGE
H	H	H	L	↓	L	H	
H	H	L	H	↓	H	L	
H	H	H	H	↓	Q̄ _n	Q _n	TOGGLE
H	H	X	X	↑	Q _n	Q̄ _n	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 7	V
V _I	DC Input Voltage	-0.5 to V _{CC} +0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	-40 to 85 -55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V_{IH}	High Level Input Voltage	2.0		1.5	—	—	1.5	—	1.5	—	V	
		4.5		3.15	—	—	3.15	—	3.15	—		
		6.0		4.2	—	—	4.2	—	4.2	—		
V_{IL}	Low Level Input Voltage	2.0		—	—	0.5	—	0.5	—	0.5	V	
		4.5		—	—	1.35	—	1.35	—	1.35		
		6.0		—	—	1.8	—	1.8	—	1.8		
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			V_{IH} or V_{IL}	-20 μA	4.4	4.5	—	4.4	—	
		6.0	V_{IL}	-4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		4.5		-5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
6.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	—	V	
4.5			—	0.0	0.1	—	0.1	—	0.1	—		
6.0			—	0.0	0.1	—	0.1	—	0.1	—		
4.5			4.0 mA	—	0.17	0.26	—	0.33	—	0.40		—
6.0	5.2 mA	—	0.18	0.26	—	0.33	—	0.40	—			
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND	—	—	± 0.1	—	± 1.0	—	± 1.0	μA	
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND	—	—	2	—	20	—	40	μA	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, $C_L = 15\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, Q)		16	25	ns
t_{PLH}	Propagation Delay Time PR, CLEAR - Q, Q		20	31	ns
f_{MAX}	Maximum Clock Frequency	33	58		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

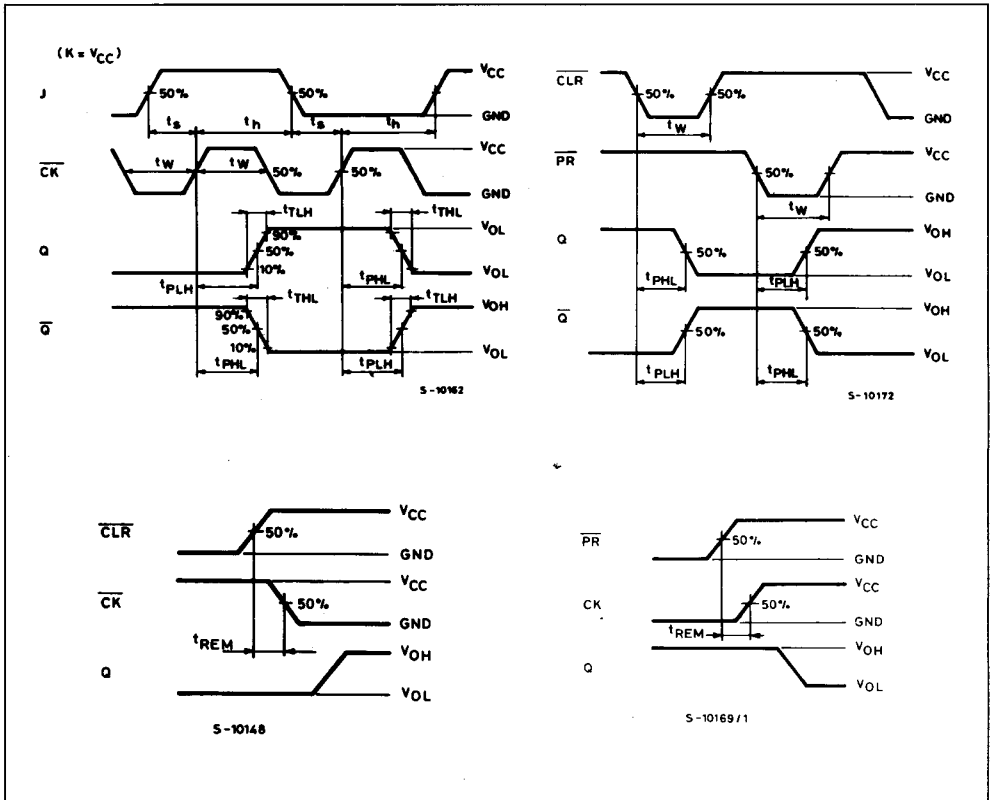
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	22 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, \bar{Q})	2.0 4.5 6.0		— — —	76 19 16	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (\overline{PR} , \overline{CLR} -Q, \bar{Q})	2.0 4.5 6.0		— — —	92 23 20	180 36 31	— — —	225 45 38	— — —	270 54 46	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	13 53 62	— — —	4.8 24 28	— — —	4.0 20 24	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(H)}$	Minimum Pulse Width CLEAR PRESET	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time J, K	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_h	Minimum Hold Time J, K	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time (CLEAR, PRESET)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	54	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained the following equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (for 1 Flip/Flop)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

TEST CIRCUIT I_{CC} (Opr.)