

FEATURES

- Analog/HDMI dual interface**
- Supports high bandwidth digital content protection**
- RGB-to-YCbCr 2-way color conversion**
- Automated clamping level adjustment**
- 1.8 V/3.3 V power supply**
- 100-lead LQFP Pb-free package**
- RGB and YCbCr output formats**
- Analog interface**
 - 8-bit triple ADC
 - 100 MSPS maximum conversion rate
 - Macrovision® detection
 - 2:1 input mux
 - Full sync processing
 - Sync detect for hot plugging
 - Midscale clamping
- Digital video interface**
 - HDMI v 1.1, DVI v 1.0
 - 150 MHz HDMI receiver
 - Supports high bandwidth digital content protection (HDCP 1.1)
- Digital audio interface**
 - HDMI 1.1-compatible audio interface
 - S/PDIF (IEC90658-compatible) digital audio output
 - Multichannel I2S audio output (up to 8 channels)

APPLICATIONS

- Advanced TV
- HDTV
- Projectors
- LCD monitor

GENERAL DESCRIPTION

The AD9880 offers designers the flexibility of an analog interface and high definition multimedia interface (HDMI) receiver integrated on a single chip. Also included is support for high bandwidth digital content protection (HDCP).

Analog Interface

The AD9880 is a complete 8-bit 150 MSPS monolithic analog interface optimized for capturing component video (YPbPr) and RGB graphics signals. Its 150 MSPS encode rate capability and full power analog bandwidth of 330 MHz supports all HDTV formats (up to 1080 p) and FPD resolutions up to SXGA (1280 × 1024 @ 75 Hz).

The analog interface includes a 150 MHz triple ADC with internal 1.25 V reference, a phase-locked loop (PLL), and programmable gain, offset, and clamp control. The user provides only 1.8 V and 3.3 V power supplies, analog input, and Hsync. Three-state

Rev. 0

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FUNCTIONAL BLOCK DIAGRAM

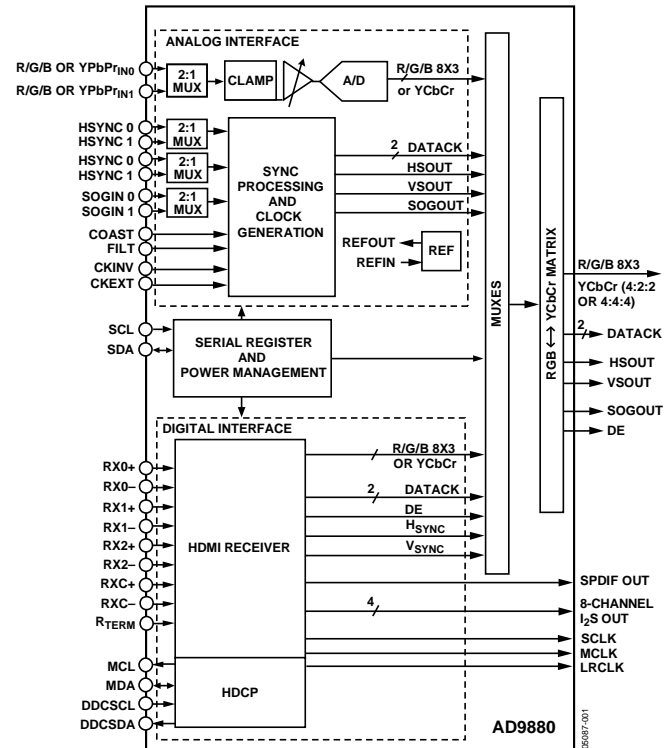


Figure 1.

CMOS outputs can be powered from 1.8 V to 3.3 V. The AD9880's on-chip PLL generates a pixel clock from Hsync. Pixel clock output frequencies range from 12 MHz to 150 MHz. PLL clock jitter is typically less than 700 ps p-p at 150 MHz. The AD9880 also offers full sync processing for composite sync and sync-on-green (SOG) applications.

Digital Interface

The AD9880 contains a HDMI 1.1-compatible receiver and supports all HDTV formats (up to 1080 p and 720 p) and display resolutions up to SXGA (1280 × 1024 @75 Hz). The receiver features an intrapair skew tolerance of up to one full clock cycle. With the inclusion of HDCP, displays can now receive encrypted video content. The AD9880 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of the authentication during transmission, as specified by the HDCP v 1.1 protocol.

Fabricated in an advanced CMOS process, the AD9880 is provided in a space-saving, 100-lead LQFP surface-mount Pb-free plastic package and is specified over the 0°C to 70°C temperature range.

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REVISION HISTORY**8/05—Revision 0: Initial Version**

SPECIFICATIONS

ANALOG INTERFACE ELECTRICAL CHARACTERISTICS

$V_{DD}, V_D = 3.3\text{ V}$, $DV_{DD} = PV_{DD} = 1.8\text{ V}$, ADC clock = maximum.

Table 1.

| Parameter | Temp | Test Level | AD9880KSTZ-100 | | | AD9880KSTZ-150 | | | Unit |
|---|-------|------------|-----------------------|--------|-----------|-----------------------|--------|-----------|--------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | | | 8 | | | 8 | | Bits |
| DC ACCURACY | | | | | | | | | |
| Differential Nonlinearity | 25°C | I | | -0.6 | +1.6/-1.0 | | ±0.7 | +1.8/-1.0 | LSB |
| Integral Nonlinearity | 25°C | I | | ±1.0 | ±2.1 | | ±1.1 | ±2.25 | LSB |
| No Missing Codes | Full | | Guaranteed | | | Guaranteed | | | |
| ANALOG INPUT | | | | | | | | | |
| Input Voltage Range | | | | | | | | | |
| Minimum | Full | VI | | | 0.5 | | | 0.5 | V p-p |
| Maximum | Full | VI | 1.0 | | | 1.0 | | | V p-p |
| Gain Tempco | +25°C | V | | 100 | | | 220 | | ppm/°C |
| Input Bias Current | +25°C | V | | 0.2 | | | 1 | | µA |
| Input Full-Scale Matching | 25°C | VI | | 1.25 | 5 | | 1.25 | 5 | %FS |
| | Full | VI | | 1.50 | 7 | | 1.50 | 7 | %FS |
| Offset Adjustment Range | Full | V | | 50 | | | 50 | | %FS |
| SWITCHING PERFORMANCE ¹ | | | | | | | | | |
| Maximum Conversion Rate | Full | VI | 100 | | | 150 | | | MSPS |
| Minimum Conversion Rate | Full | VI | | | 10 | | | 10 | MSPS |
| Data to Clock Skew | Full | IV | -0.5 | | +2.0 | -0.5 | | +2.0 | ns |
| Serial Port Timing | | | | | | | | | |
| t _{BUFF} | Full | VI | 4.7 | | | 4.7 | | | µs |
| t _{STAH} | Full | VI | 4.0 | | | 4.0 | | | µs |
| t _{DHO} | Full | VI | 0 | | | 0 | | | µs |
| t _{DAL} | Full | VI | 4.7 | | | 4.7 | | | µs |
| t _{DAH} | Full | VI | 4.0 | | | 4.0 | | | µs |
| t _{DSU} | Full | VI | 250 | | | 250 | | | ns |
| t _{STASU} | Full | VI | 4.7 | | | 4.7 | | | µs |
| t _{STOSU} | Full | VI | 4.0 | | | 4.0 | | | µs |
| HSYNC Input Frequency | Full | VI | 15 | | 110 | 15 | | 110 | KHz |
| Maximum PLL Clock Rate | Full | VI | 100 | | | 150 | | | MHz |
| Minimum PLL Clock Rate | Full | IV | | | 12 | | | 12 | MHz |
| PLL Jitter | +25°C | IV | | 700 | | | 700 | | ps p-p |
| Sampling Phase Tempco | Full | IV | | 15 | | | 15 | | ps/°C |
| DIGITAL INPUTS: (5V tolerant) | | | | | | | | | |
| Input Voltage, High (V _{IH}) | Full | VI | 2.6 | | | 2.6 | | | V |
| Input Voltage, Low (V _{IL}) | Full | VI | | | 0.8 | | | 0.8 | V |
| Input Current, High (I _{IH}) | Full | V | | -82 | | | -82 | | µA |
| Input Current, Low (I _{IL}) | Full | V | | 82 | | | 82 | | µA |
| Input Capacitance | 25°C | V | | 3 | | | 3 | | pF |
| DIGITAL OUTPUTS | | | | | | | | | |
| Output Voltage, High (V _{OH}) | Full | VI | V _{DD} - 0.1 | | | V _{DD} - 0.1 | | | V |
| Output Voltage, Low (V _{OL}) | Full | VI | | | 0.4 | | | 0.4 | V |
| Duty Cycle, DATAACK | Full | V | 45 | 50 | 55 | 45 | 50 | 55 | % |
| Output Coding | | | | Binary | | | Binary | | |
| POWER SUPPLY | | | | | | | | | |
| V _D Supply Voltage | Full | IV | 3.15 | 3.3 | 3.47 | 3.15 | 3.3 | 3.47 | V |
| DV _{DD} Supply Voltage | Full | IV | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |

AD9880

| Parameter | Temp | Test Level | AD9880KSTZ-100 | | | AD9880KSTZ-150 | | | Unit |
|--|------|------------|----------------|-----|------------------|----------------|------|------------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{DD} Supply Voltage | Full | IV | 1.7 | 3.3 | 3.47 | 1.7 | 3.3 | 3.47 | V |
| PV _{DD} Supply Voltage | Full | IV | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| I _D Supply Current (V _D) | 25°C | VI | | 260 | 300 | | | 330 | mA |
| I _{DVDD} Supply Current (DV _{DD}) | 25°C | VI | | 45 | 60 | | | 85 | mA |
| I _{DD} Supply Current (V _{DD}) ² | 25°C | VI | | 37 | 100 ³ | | | 130 ³ | mA |
| IP _{VDD} Supply Current (PV _{DD}) | 25°C | VI | | 10 | 15 | | | 20 | mA |
| Total Power | Full | VI | | 1.1 | 1.4 | | 1.15 | 1.4 | W |
| Power-Down Dissipation | Full | VI | | 130 | | | 130 | | mW |
| DYNAMIC PERFORMANCE | | | | | | | | | |
| Analog Bandwidth, Full Power | 25°C | V | | 330 | | | 330 | | MHz |
| Signal-to-Noise Ratio (SNR) | 25°C | I | | 46 | | | 46 | | dB |
| Without Harmonics | Full | V | | 45 | | | 45 | | dB |
| f _{IN} = 40.7 MHz | | | | | | | | | |
| Crosstalk | Full | V | | 60 | | | 60 | | dBc |
| THERMAL CHARACTERISTICS | | | | | | | | | |
| θ _{JA} -Junction-to-Ambient | | V | | 35 | | | 35 | | °C/W |

¹ Drive strength = high.

² DATAACK load = 15 pF, data load = 5 pF.

³ Specified current and power values with a worst case pattern (on/off).

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

V_{DD} = V_D = 3.3 V, DV_{DD} = PV_{DD} = 1.8 V, ADC clock = maximum.

Table 2.

| Parameter | Test Level | Conditions | AD9880KSTZ-100 | | | AD9880KSTZ-150 | | | Unit |
|--|------------|---------------------|-----------------------|-----|-----|----------------|-----|-----|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | | | 8 | | | 8 | | Bit |
| DC DIGITAL I/O Specifications | | | | | | | | | |
| High-Level Input Voltage, (V _{IH}) | VI | | 2.5 | | | 2.5 | | | V |
| Low-Level Input Voltage, (V _{IL}) | VI | | | | 0.8 | | | 0.8 | V |
| High-Level Output Voltage, (V _{OH}) | VI | | V _{DD} - 0.1 | | | | | | V |
| Low-Level Output Voltage, (V _{OL}) | VI | | V _{DD} - 0.1 | | 0.1 | | | 0.1 | V |
| DC SPECIFICATIONS | | | | | | | | | |
| Output High Level | IV | Output drive = high | | 36 | | | 36 | | mA |
| (I _{OHD}) (V _{OUT} = V _{OH}) | IV | Output drive = low | | 24 | | | 24 | | mA |
| Output Low Level | IV | Output drive = high | | 12 | | | 12 | | mA |
| (I _{OLD} , (V _{OUT} = V _{OL})) | IV | Output drive = low | | 8 | | | 8 | | mA |
| DATAACK High Level | IV | Output drive = high | | 40 | | | 40 | | mA |
| (V _{OHC} , (V _{OUT} = V _{OH})) | IV | Output drive = low | | 20 | | | 20 | | mA |
| DATAACK Low Level | IV | Output drive = high | | 30 | | | 30 | | mA |
| (V _{OLC} , (V _{OUT} = V _{OL})) | IV | Output drive = low | | 15 | | | 15 | | mA |
| Differential Input Voltage, Single Ended Amplitude | IV | | 75 | | 700 | 75 | | 700 | mV |

| Parameter | Test Level | Conditions | AD9880KSTZ-100 | | | AD9880KSTZ-150 | | | Unit |
|---|------------|--|----------------|-----|------------------|----------------|-----|------|--------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| POWER SUPPLY | | | | | | | | | |
| V _D Supply Voltage | IV | | 3.15 | 3.3 | 3.47 | 3.15 | 3.3 | 3.47 | V |
| V _{DD} Supply Voltage | IV | | 1.7 | 3.3 | 3.47 | 1.7 | 3.3 | 3.47 | V |
| DV _{DD} Supply Voltage | IV | | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| PV _{DD} Supply Voltage | IV | | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| I _{VD} Supply Current (Typical Pattern) ¹ | V | | | 80 | 100 | | 80 | 110 | mA |
| I _{VDD} Supply Current (Typical Pattern) ² | V | | | 40 | 100 ³ | | 55 | 175* | |
| I _{DVDD} Supply Current (Typical Pattern) ^{1, 4} | V | | | 88 | 110 | | 110 | 145 | mA |
| I _{PVDD} Supply Current (Typical Pattern) ¹ | V | | | 26 | 35 | | 30 | 40 | mA |
| Power-Down Supply Current (I _{PD}) | VI | | | 130 | | | 130 | | mA |
| AC SPECIFICATIONS | | | | | | | | | |
| Intrapair (+ to -) Differential Input Skew (T _{DPS}) | IV | | | | | | | 360 | pS |
| Channel to Channel Differential Input Skew (T _{CCS}) | IV | | | | | | | 6 | Clock Period |
| Low-to-High Transition Time for Data and Controls (D _{LHT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 900 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1300 | ps |
| Low-to-High Transition Time for DATAACK (D _{LHT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 650 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1200 | ps |
| High-to-Low Transition Time for Data and Controls (D _{HLT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 850 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1250 | ps |
| High-to-Low Transition Time for DATAACK (D _{HLT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 800 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1200 | ps |
| Clock to Data Skew ⁵ (T _{SKEW}) | IV | | -0.5 | | 2.0 | -0.5 | | 2.0 | ns |
| Duty Cycle, DATAACK ⁵ | IV | | 45 | 50 | | | | 55 | % |
| DATAACK Frequency (F _{CIP}) | VI | | 20 | | | | | 150 | MHz |

¹ The typical pattern contains a gray scale area, output drive = high. Worst case pattern is alternating black and white pixels.

² The typical pattern contains a gray scale area, output drive = high.

³ Specified current and power values with a worst case pattern (on/off).

⁴ DATAACK load = 10 pF, data load = 5 pF.

⁵ Drive strength = high.

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|------------------------------|-------------------------|
| VD | 3.6 V |
| VDD | 3.6 V |
| DVDD | 1.98 V |
| PVDD | 1.98 V |
| Analog Inputs | V _D to 0.0 V |
| Digital Inputs | 5 V to 0.0 V |
| Digital Output Current | 20 mA |
| Operating Temperature | -25°C to + 85°C |
| Storage Temperature | -65°C to + 150°C |
| Maximum Junction Temperature | 150°C |
| Maximum Case Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

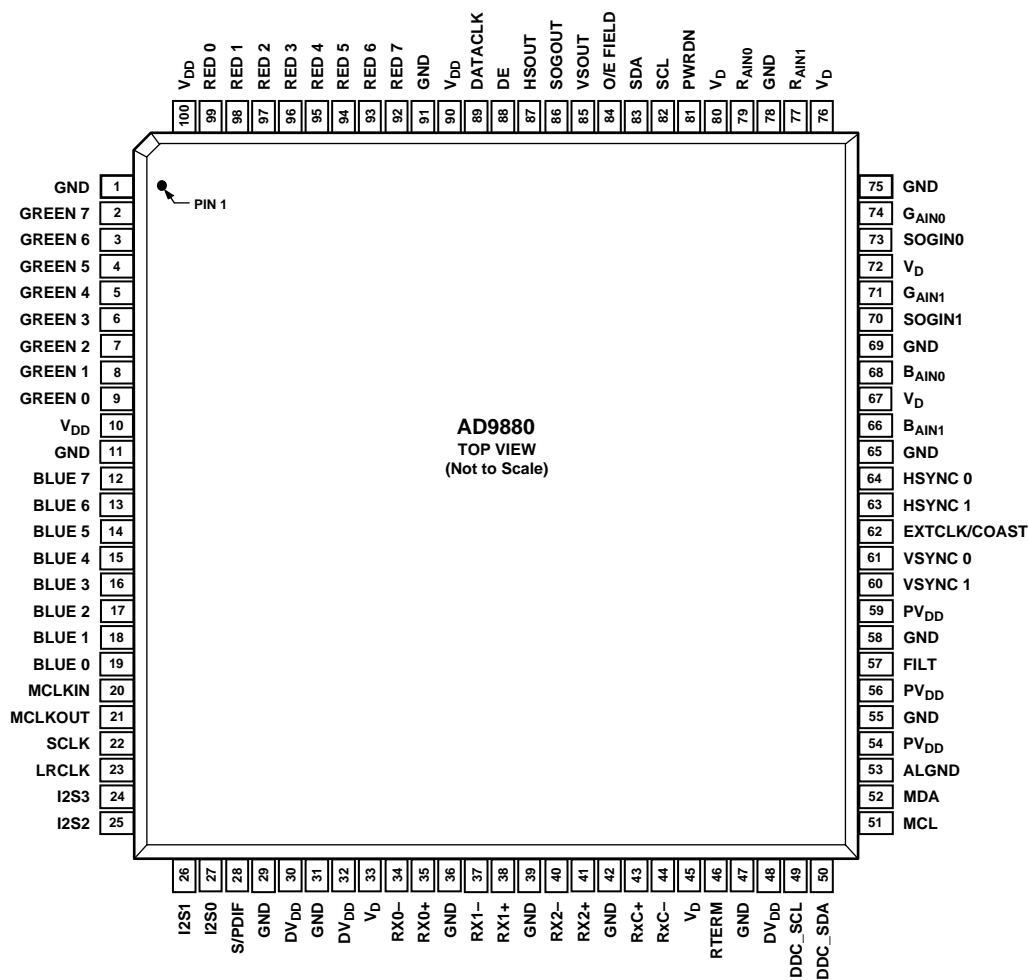


Figure 2. Pin Configuration

05087-002

Table 4. Complete Pinout List

| Pin Type | Pin No. | Mnemonic | Function | Value |
|----------|---------|----------|---|----------------|
| INPUTS | 79 | RAIN0 | Analog Input for Converter R Channel 0 | 0.0 V to 1.0 V |
| | 77 | RAIN1 | Analog Input for Converter R Channel 1 | 0.0 V to 1.0 V |
| | 74 | GAIN0 | Analog Input for Converter G Channel 0 | 0.0 V to 1.0 V |
| | 71 | GAIN1 | Analog Input for Converter G Channel 1 | 0.0 V to 1.0 V |
| | 68 | BAIN0 | Analog Input for Converter B Channel 0 | 0.0 V to 1.0 V |
| | 66 | BAIN1 | Analog Input for Converter B Channel 1 | 0.0 V to 1.0 V |
| | 64 | HSYNC0 | Horizontal SYNC Input for Channel 0 | 3.3 V CMOS |
| | 63 | HSYNC1 | Horizontal SYNC Input for Channel 1 | 3.3 V CMOS |
| | 61 | VSYNC0 | Vertical SYNC Input for Channel 0 | 3.3 V CMOS |
| | 60 | VSYNC1 | Vertical SYNC Input for Channel 1 | 3.3 V CMOS |
| | 73 | SOGIN0 | Input for Sync-on-Green Channel 0 | 0.0 V to 1.0 V |
| | 70 | SOGIN1 | Input for Sync-on-Green Channel 1 | 0.0 V to 1.0 V |
| | 62 | EXTCLK | External Clock Input—Shares Pin with COAST | 3.3 V CMOS |
| | 62 | COAST | PLL COAST Signal Input—Shares Pin with EXTCLK | 3.3 V CMOS |
| | 81 | PWRDN | Power-Down Control | 3.3 V CMOS |

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| Pin Type | Pin No. | Mnemonic | Function | Value |
|----------------------------|------------------------|------------------|---|-----------------|
| OUTPUTS | 92 to 99 | RED [7:0] | Outputs of Red Converter, Bit 7 is MSB | V _{DD} |
| | 2 to 9 | GREEN [7:0] | Outputs of Green Converter, Bit 7 is MSB | V _{DD} |
| | 12 to 19 | BLUE [7:0] | Outputs of Blue Converter, Bit 7 is MSB | V _{DD} |
| | 89 | DATAACK | Data Output Clock | V _{DD} |
| | 87 | HSOUT | HSYNC Output Clock (Phase-Aligned with DATAACK) | V _{DD} |
| | 85 | VSOUT | VSYNC Output Clock (Phase-Aligned with DATAACK) | V _{DD} |
| | 86 | SOGOUT | SOG Slicer Output | V _{DD} |
| | 84 | O/E FIELD | Odd/Even Field Output | V _{DD} |
| REFERENCES | 57 | FILT | Connection For External Filter Components For PLL | |
| POWER SUPPLY | 80, 76, 72, 67, 45, 33 | V _D | Analog Power Supply and DVI Terminators | 3.3 V |
| | 100, 90, 10 | V _{DD} | Output Power Supply | 1.8 V to 3.3 V |
| | 59, 56, 54 | PV _{DD} | PLL Power Supply | 1.8 V |
| | 48, 32, 30 | DV _{DD} | Digital Logic Power Supply | 1.8 V |
| | | GND | Ground | 0 V |
| CONTROL | 83 | SDA | Serial Port Data I/O | 3.3 V CMOS |
| | 82 | SCL | Serial Port Data Clock | 3.3 V CMOS |
| HDCP | 49 | DDC_SCL | HDCP Slave Serial Port Data Clock | 3.3 V CMOS |
| | 50 | DDC_SDA | HDCP Slave Serial Port Data I/O | 3.3 V CMOS |
| | 51 | MCL | HDCP Master Serial Port Data Clock | 3.3 V CMOS |
| | 52 | MDA | HDCP Master Serial Port Data I/O | 3.3 V CMOS |
| AUDIO DATA OUTPUTS | 28 | S/PDIF | S/PDIF Digital Audio Output | V _{DD} |
| | 27 | I2S0 | I ² S Audio (Channels 1, 2) | V _{DD} |
| | 26 | I2S1 | I ² S Audio (Channels 3, 4) | V _{DD} |
| | 25 | I2S2 | I ² S Audio (Channels 5, 6) | V _{DD} |
| | 24 | I2S3 | I ² S Audio (Channels 7, 8) | V _{DD} |
| | 20 | MCLKIN | External Reference Audio Clock In | V _{DD} |
| | 21 | MCLKOUT | Audio Master Clock Output | V _{DD} |
| | 22 | SCLK | Audio Serial Clock Output | V _{DD} |
| | 23 | LRCLK | Data Output Clock For Left And Right Audio Channels | V _{DD} |
| DIGITAL VIDEO DATA | 35 | Rx0+ | Digital Input Channel 0 True | TMDS |
| | 34 | Rx0- | Digital Input Channel 0 Complement | TMDS |
| | 38 | Rx1+ | Digital Input Channel 1 True | TMDS |
| | 37 | Rx1- | Digital Input Channel 1 Complement | TMDS |
| | 41 | Rx2+ | Digital Input Channel 2 True | TMDS |
| | 40 | Rx2- | Digital Input Channel 2 Complement | TMDS |
| DIGITAL VIDEO CLOCK INPUTS | 43 | RxC+ | Digital Data Clock True | TMDS |
| | 44 | RxC- | Digital Data Clock Complement | TMDS |
| DATA ENABLE | 88 | DE | Data Enable | 3.3 V CMOS |
| RTERM | 46 | RTERM | Sets Internal Termination Resistance | 500Ω |

Table 5. Pin Function Descriptions

| Pin | Description |
|-------------------|--|
| INPUTS | |
| R _{AIN0} | Analog Input for the Red Channel 0. |
| G _{AIN0} | Analog Input for the Green Channel 0. |
| B _{AIN0} | Analog Input for the Blue Channel 0. |
| R _{AIN1} | Analog Input for the Red Channel 1. |
| G _{AIN1} | Analog Input for the Green Channel 1. |
| B _{AIN1} | Analog Input for Blue Channel 1. |
| | High impedance inputs that accept the red, green, and blue channel graphics signals, respectively. The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference. They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation. (see Figure 3 for an input reference circuit). |
| Rx0+ | Digital Input Channel 0 True. |
| Rx0- | Digital Input Channel 0 Complement. |
| Rx1+ | Digital Input Channel 1 True. |
| Rx1- | Digital Input Channel 1 Complement. |
| Rx2+ | Digital Input Channel 2 True. |
| Rx2- | Digital input Channel 2 Complement. |
| | These six pins receive three pairs TMD5 (Transition Minimized Differential Signaling) pixel data (at 10X the pixel rate) from a digital graphics transmitter. |
| RxC+ | Digital Data Clock True. |
| RxC- | Digital Data Clock Complement. |
| | This clock pair receives a TMD5 clock at 1× pixel data rate. |
| HSYNC0 | Horizontal Sync Input Channel 0. |
| HSYNC1 | Horizontal Sync Input Channel 1. |
| | These inputs receive a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by serial register 0x12 Bits 5:4 (Hsync polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity. |
| VSYNC0 | Vertical Sync Input Channel 0. |
| VSYNC1 | Vertical Sync Input Channel 1. |
| | These are the inputs for vertical sync. |
| SOGIN0 | Sync-On-Green Input Channel 0. |
| SOGIN1 | Sync-On-Green Input Channel 1. |
| | These inputs are provided to assist with processing signals with embedded sync, typically on the green channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 10 mV steps to any voltage between 10 mV and 330 mV above the negative peak of the input signal. The default voltage threshold is 150 mV. When connected to an ac-coupled graphics signal with embedded sync, it produces a noninverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync (Hsync) information that must be separated before passing the horizontal sync signal to Hsync.) When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Hsync and Vsync Inputs section. |
| EXTCLK/COAST | Coast Input to Clock Generator (Optional). |
| | This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses during the vertical interval. The Coast signal is generally not required for PC-generated signals. The logic sense of this pin is controlled by Coast polarity (Register 0x18, Bits 6:5). When not used, this pin may be grounded and input Coast polarity programmed to 1 (Register 0x18, Pin 5), or tied high (to V _D through a 10 KΩ resistor) and input Coast polarity programmed to 0. Input Coast polarity defaults to 1 at power-up. This pin is shared with the EXTCLK function, which does not affect Coast functionality. For more details on Coast, see the description in the Clock Generation section. |
| EXTCLK/COAST | External Clock. |
| | This allows the insertion of an external clock source rather than the internally generated PLL locked clock. This pin is shared with the Coast function, which will not affect EXTCLK functionality. |

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| Pin | Description |
|-------------------|---|
| PWRDN | Power-Down Control/Three-State Control. The function of this pin is programmable via Register 0x26 [2:1]. |
| FILT | External Filter Connection. For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node. For more information see the section on PCB Layout Recommendations. |
| OUTPUTS | |
| HSOUT | Horizontal Sync Output. A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATAACK and Data, data timing with respect to horizontal sync can always be determined. |
| VSOUT | Vertical Sync Output. The separated Vsync from a composite signal or a direct pass through of the Vsync signal. The polarity of this output can be controlled via serial bus bit (Register 0x24 [6]). |
| SOGOUT | Sync-On-Green Slicer Output. This pin outputs one of four possible signals (controlled by Register 0x1D [1:0]): raw SOG, raw Hsync, regenerated Hsync from the filter, or the filtered Hsync. See the Sync processing block diagram (see Figure 8) to view how this pin is connected. (Note: besides slicing off SOG, the output from this pin is not processed on the AD9880. Vsync separation is performed via the sync separator. |
| O/E FIELD | Odd/Even Field Bit for Interlaced Video. This output will identify whether the current field (in an interlaced signal) is odd or even. The polarity of this signal is programmable via Register 0x24[4]. |
| SERIAL PORT | |
| SDA | Serial Port Data I/O for programming AD9880 registers – I2C address is 0x98. |
| SCL | Serial Port Data Clock for programming AD9880 registers. |
| DDCSDA | Serial Port Data I/O for HDCP communications to transmitter – I2C address is 0x74 or 0x76. |
| DDCSCL | Serial Port Data Clock for HDCP communications to transmitter. |
| MDA | Serial Port Data I/O to EEPROM with HDCP keys – I2C address is 0xA0 |
| MCL | Serial Port Data Clock to EEPROM with HDCP keys. |
| DATA OUTPUTS | |
| Red [7:0] | Data Output, Red Channel. |
| Green [7:0] | Data Output, Green Channel. |
| Blue [7:0] | Data Output, Blue Channel. The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed, but will be different if the color space converter is used. When the sampling time is changed by adjusting the phase register, the output timing is shifted as well. The DATAACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. |
| DATA CLOCK OUTPUT | |
| DATAACK | Data Clock Output. This is the main clock output signal used to strobe the output data and HSOUT into external logic. Four possible output clocks can be selected with Register 0x25 [7:6]. These are related to the pixel clock (1/2× pixel clock, 1× pixel clock, 2× frequency pixel clock and a 90° phase shifted pixel clock) and they are produced either by the internal PLL clock generator or EXTCLK and are synchronous with the pixel sampling clock. The polarity of DATAACK can also be inverted via Register 0x24 [0]. The sampling time of the internal pixel clock can be changed by adjusting the phase register. When this is changed, the pixel-related DATAACK timing is shifted as well. The DATA, DATAACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained. |

| Pin | Description |
|---------------------------------|---|
| POWER SUPPLY ¹ | |
| V _D (3.3 V) | Analog Power Supply. These pins supply power to the ADCs and terminators. They should be as quiet and filtered as possible. |
| V _{DD} (1.8 V – 3.3 V) | Digital Output Power Supply. A large number of output pins (up to 27) switching at high speed (up to 150 MHz) generates many power supply transients (noise). These supply pins are identified separately from the V _D pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9880 is interfacing with lower voltage logic, V _{DD} may be connected to a lower supply voltage (as low as 1.8 V) for compatibility. |
| PV _{DD} (1.8 V) | Clock Generator Power Supply. The most sensitive portion of the AD9880 is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins. |
| DV _{DD} (1.8 V) | Digital Input Power Supply. This supplies power to the digital logic. |
| GND | Ground. The ground return for all circuitry on chip. It is recommended that the AD9880 be assembled on a single solid ground plane, with careful attention to ground current paths. |

¹ The supplies should be sequenced such that V_D and V_{DD} are never less than 300 mV below DV_{DD}. At no time should DV_{DD} be more than 300 mV greater than V_D or V_{DD}.

DESIGN GUIDE

GENERAL DESCRIPTION

The AD9880 is a fully integrated solution for capturing analog RGB or YUV signals and digitizing them for display on flat panel monitors, projectors, or PDPs. In addition, the AD9880 has a digital interface for receiving DVI/HDMI signals and is capable of decoding HDCP encrypted signals through connections to an internal EEPROM. The circuit is ideal for providing an interface for HDTV monitors or as the front end to high performance video scan converters.

Implemented in a high-performance CMOS process, the interface can capture signals with pixel rates of up to 150 MHz.

The AD9880 includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. Included in the output formatting is a color space converter (CSC), which accommodates any input color space and can output any color space. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

DIGITAL INPUTS

All digital control inputs (Hsync, Vsync, I2C) on the AD9880 operate to 3.3 V CMOS levels. In addition, all digital inputs except the TMDS (HDMI/DVI) inputs are 5 V tolerant. (Applying 5 V to them does not cause any damage.) TMDS inputs (RX0+/-, RX1+/-, RX2+/-, and RXC+/-) must maintain a 100 Ω differential impedance (through proper PCB layout) from the connector to the input where they are internally terminated (50 Ω to 3.3 V). If additional ESD protection is desired, use of a California Micro Devices (CMD) CM1213 (among others) series low capacitance ESD protection offers 8 kV of protection to the HDMI TMDS lines.

ANALOG INPUT SIGNAL HANDLING

The AD9880 has six high-impedance analog input pins for the red, green, and blue channels. They accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or RCA-type connectors. The AD9880 should be located as close as practical to the input connector. Signals should be routed via 75 Ω matched impedance traces to the IC input pins.

At that point the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9880 inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The ultrawide bandwidth inputs of the AD9880 (330 MHz) can track the input signal continuously as it moves from one pixel level to the next, and digitizes the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly, and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 High Speed Signal Chip Bead inductor in the circuit shown in Figure 3 gives good results in most applications.

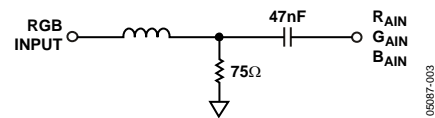


Figure 3. Analog Input Interface Circuit

HSYNC AND VSYNC INPUTS

The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic. However, it is tolerant of 5 V logic signals.

OUTPUT SIGNAL HANDLING

The digital outputs are designed to operate from 1.8 V to 3.3 V (V_{DD}).

CLAMPING

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board ADC.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at 300 mV. Then white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability.

This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9880.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the ADCs producing a black output (Code 0x00) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most pc graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync called the back porch where a good black reference is provided. This is the time when clamping should be done.

Clamp timing employs the AD9880 internal clamp timing generator. The clamp placement register is programmed with the number of pixel periods that should pass after the trailing edge of Hsync before clamping starts. A second register (clamp duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 0x08 (providing 8 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 0x14 (giving the clamp 20 pixel periods to reestablish the black reference). For three-level syncs embedded on the green channel, it is necessary to increase the clamp placement to beyond the positive portion of the sync. For example, a good clamp placement (Register 0x19) for a 720p input is 0x26. This delays the start of clamp by 38 pixel clock cycles after the rising edge of the three-level sync, allowing plenty of time for the signal to return to a black reference.

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there is a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it takes excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to

within ½ LSB in 10 lines with a clamp duration of 20 pixel periods on a 75 Hz SXGA signal.

YUV Clamping

YUV graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the graphics signal rather than the bottom. For these signals it can be necessary to clamp to the midscale range of the ADC range (128) rather than bottom of the ADC range (0).

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either midscale or ground independently. These bits are located in Register 0x1B [7:5]. The midscale reference voltage is internally generated for each converter.

Auto Offset

The auto-offset circuit works by calculating the required offset setting to yield a given output code during clamp. When this block is enabled, the offset setting in the I²C is seen as a desired clamp code rather than an actual offset. The circuit compares the output code during clamp to the desired code and adjusts the offset up or down to compensate.

The offset on the AD9880 can be adjusted automatically to a specified target code. Using this option allows the user to set the offset to any value and be assured that all channels with the same value programmed into the target code will match. This eliminates any need to adjust the offset at the factory. This function is capable of running continuously anytime the clamp is asserted.

There is an offset adjust register for each channel, namely the offset registers at Addresses 0x08, 0x0A, and 0x0C. The offset adjustment is a signed (twos complement) number with ±64 LSB range. The offset adjustment is added to whatever offset the auto-offset comes up with. For example: using ground clamp, the target code is set to 4. To get this code, the auto-offset generates an offset of 68. If the offset adjustment is set to 10, the offset sent to the converter is 78. Likewise, if the offset adjust is set to -10, the offset sent to the converter is 58. Refer to application note AN-775, Implementing the Auto-Offset Function of the AD9880, for a detailed description of how to use this function.

Sync-on-Green (SOG)

The SOG input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level to a programmable level (typically 150 mV) above the negative peak. The SOG input must be ac-coupled to the green analog input through its own capacitor. The value of the capacitor must be 1 nF ± 20%. If SOG is not used, this connection is not

required. Note that the SOG signal is always negative polarity. For additional detail on setting the SOG threshold and other SOG-related functions, see the Sync Processing section.

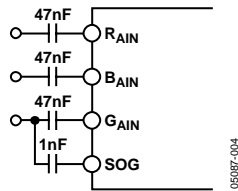


Figure 4. Typical Clamp Configuration for RGB/YUV Applications

Clock Generation

A PLL is employed to generate the pixel clock. In this PLL, the Hsync input provides a reference frequency. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (Registers 0x01 and 0x02) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal slews from the old pixel amplitude and settles at its new value. This is followed by a time when the input voltage is stable before the signal must slew to a new value. The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter and the stable pixel time also becomes shorter.

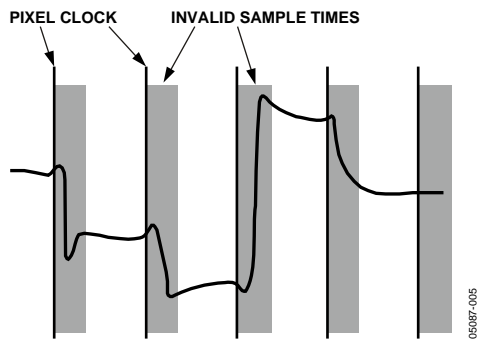


Figure 5. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined and must also be subtracted from the stable pixel time. Considerable care has been taken in the design of the AD9880's clock generation circuit to minimize jitter. The clock jitter of the AD9880 is less than 13% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of the VCO range and charge pump current for VESA standard display modes are listed in Table 8.

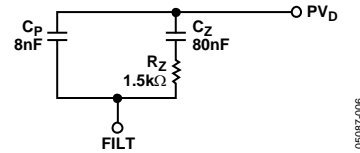


Figure 6. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are

- The 12-Bit Divisor Register. The input Hsync frequency range can be any frequency which, combined with the PLL_Div, does not exceed the VCO range. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 10 MHz to 100 MHz. The divisor register controls the exact multiplication factor.
- The 2-Bit VCO Range Register. To improve the noise performance of the AD9880, the VCO operating frequency range is divided into four overlapping regions. The VCO range register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table 6.

Table 6.

| VCORNGE | Pixel Rate Range |
|---------|------------------|
| 00 | 12-30 |
| 01 | 30-60 |
| 10 | 60-120 |
| 11 | 120-150 |

- The 5-Bit Phase Adjust Register. The phase of the generated sampling clock can be shifted to locate an optimum sampling point within a clock cycle. The phase adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

The COAST pin or the internal Coast is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal or during disturbances in Hsync (such as equalization pulses). This can be used during the vertical sync period or any other time that the Hsync signal is unavailable. The polarity of the Coast signal can be set through the Coast polarity register. Also, the polarity of the Hsync signal can be set through the Hsync polarity register. For both Hsync and Coast, a value of 1 is active high. The internal Coast function is driven off the Vsync signal, which is typically a time when Hsync signals can be disrupted with extra equalization pulses.

Power Management

The AD9880 uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, the power-down bit, and the power-down pin to determine the correct power state. There are four power states: full-power, seek mode, auto power-down and power-down.

Table 7 summarizes how the AD9880 determines which power mode to be in and which circuitry is powered on/off in each of these modes. The power-down command has priority and then

the automatic circuitry. The power-down pin (Pin 81—polarity set by Register 0x26[3]) can drive the chip into four power-down options. Bits 2 and 1 of Register 0x26 control these four options. Bit 0 controls whether the chip is powered down or the outputs are placed in high impedance mode (with the exception of SOG). Bits 7 to 4 of Register 0x26 control whether the outputs, SOG, Sony Philips digital interface (SPDIF) or I2S (IIS or Inter IC sound bus) outputs are in high impedance mode or not. See the 2-Wire Serial Control Register Detail section for the details.

Table 7. Power-Down Mode Descriptions

| Mode | Inputs | | | Power-On or Comments |
|------------|-------------------------|--------------------------|-----------------------------|---|
| | Power-Down ¹ | Sync Detect ² | Auto PD Enable ³ | |
| Full Power | 1 | 1 | X | Everything |
| Seek Mode | 1 | 0 | 0 | Everything |
| Seek Mode | 1 | 0 | 1 | Serial bus, sync activity detect, SOG, band gap reference |
| Power-Down | 0 | X | | Serial bus, sync activity detect, SOG, band gap reference |

¹ Power-down is controlled via Bit 0 in Serial Bus Register 0x26.

² Sync detect is determined by OR'ing Bits 7 to 2 in Serial Bus Register 0x15.

³ Auto power-down is controlled via Bit 7 in Serial Bus Register 0x27

Table 8. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

| Standard | Resolution | Refresh Rate | Horizontal Frequency | Pixel Rate | VCO Range ¹ | Current |
|----------|-------------|--------------|----------------------|-------------|------------------------|---------|
| VGA | 640 × 480 | 60 Hz | 31.5 kHz | 25.175 MHz | 00 | 101 |
| | | 72 Hz | 37.7 kHz | 31.500 MHz | 01 | 011 |
| | | 75 Hz | 37.5 kHz | 31.500 MHz | 01 | 100 |
| | | 85 Hz | 43.3 kHz | 36.000 MHz | 01 | 100 |
| SVGA | 800 × 600 | 56 Hz | 35.1 kHz | 36.000 MHz | 01 | 100 |
| | | 60 Hz | 37.9 kHz | 40.000 MHz | 01 | 101 |
| | | 72 Hz | 48.1 kHz | 50.000 MHz | 01 | 110 |
| | | 75 Hz | 46.9 kHz | 49.500 MHz | 01 | 110 |
| | | 85 Hz | 53.7 kHz | 56.250 MHz | 01 | 110 |
| XGA | 1024 × 768 | 60 Hz | 48.4 kHz | 65.000 MHz | 10 | 011 |
| | | 70 Hz | 56.5 kHz | 75.000 MHz | 10 | 100 |
| | | 75 Hz | 60.0 kHz | 78.750 MHz | 10 | 100 |
| | | 80 Hz | 64.0 kHz | 85.500 MHz | 10 | 101 |
| | | 85 Hz | 68.3 kHz | 94.500 MHz | 10 | 110 |
| SXGA | 1280 × 1024 | 60 Hz | 64.0 kHz | 108.000 MHz | 10 | 110 |
| | 1280 × 1024 | 75 Hz | 80.0 kHz | 135.000 MHz | 11 | 110 |
| TV | 480i | 60 Hz | 15.75 kHz | 13.51 MHz | 00 | 010 |
| | 480p | 60 Hz | 31.47 kHz | 27 MHz | 00 | 101 |
| | 720p | 60 Hz | 45 kHz | 74.25 MHz | 10 | 100 |
| | 1035i | 60 Hz | 33.75 kHz | 74.25 MHz | 10 | 100 |
| | 1080i | 60 Hz | 33.75 kHz | 74.25 MHz | 10 | 100 |
| | 1080p | 60 Hz | 67.5 kHz | 148.5 MHz | 11 | 110 |

¹ These are preliminary recommendations for the analog PLL and are subject to change without notice.

TIMING

The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally.

There is a pipeline in the AD9880, which must be flushed before valid data becomes available. This means 23 data sets are presented before valid data is available.

The timing diagram in Figure 7 shows the operation of the AD9880.

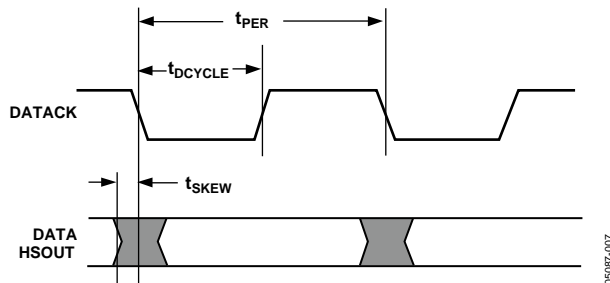


Figure 7. Output Timing

Hsync Timing

Horizontal Sync (Hsync) is processed in the AD9880 to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the phase adjust register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between the Hsync output (HSOUT) and data clock (DATAACK).

Three things happen to Hsync in the AD9880. First, the polarity of Hsync input is determined and thus has a known output polarity. The known output polarity can be programmed either active high or active low (Register 0x24, Bit 7). Second, HSOUT is aligned with DATAACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 0x23. HSOUT is the sync signal that should be used to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the Coast input and function are unnecessary, and should not be used and the pin should be permanently connected to the inactive state.

In some systems, however, Hsync is disturbed during the vertical sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ composite sync (Csync) signals or embedded SOG, Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the

clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock to this new frequency, and changes frequency by the end of the Vsync period. It then takes a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a tearing of the image at the top of the display.

The Coast input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free run at its then-current frequency. The PLL can free run for several lines without significant frequency drift.

Coast can be generated internally by the AD9880 (see Register 0x12 [1]), can be driven directly from a Vsync input, or can be provided externally by the graphics controller.

Sync Processing

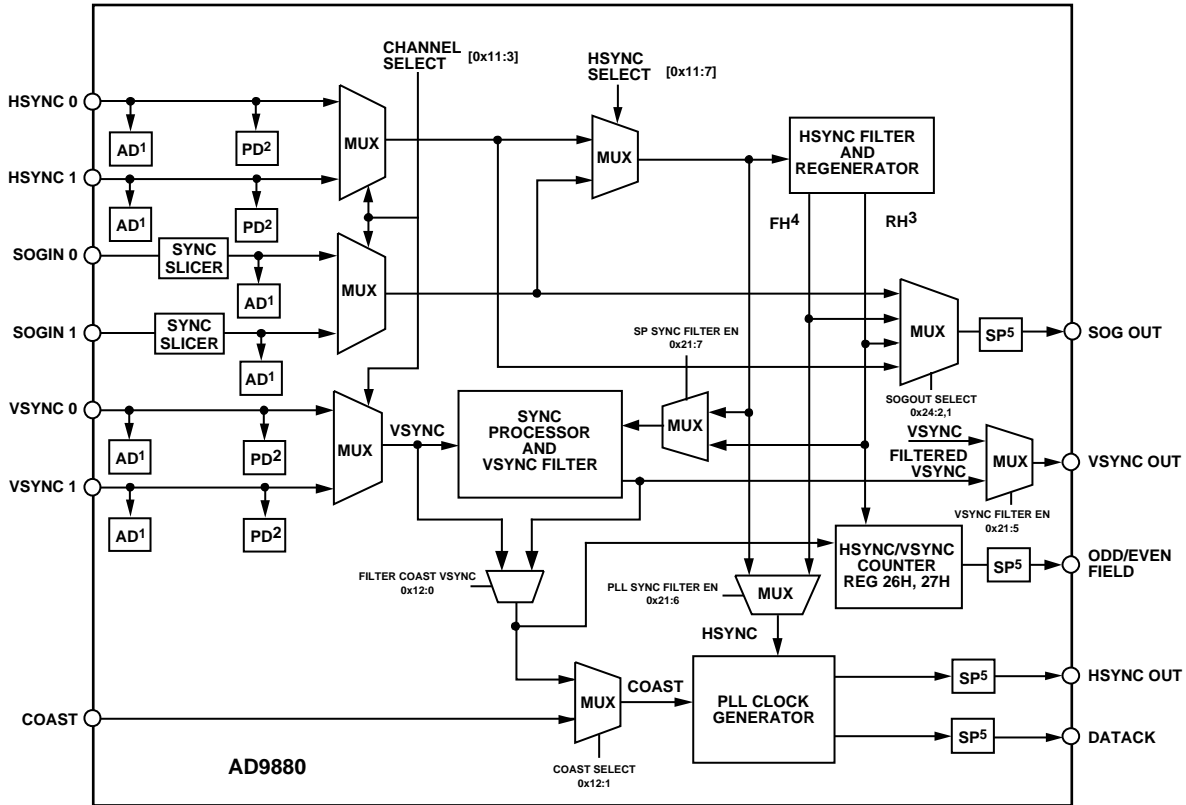
The inputs of the sync processing section of the AD9880 are combinations of digital Hsyncs and Vsyncs, analog sync-on-green, or sync-on-Y signals, and an optional external Coast signal. From these signals it generates a precise, jitter-free (9% or less at 95 MHz) clock from its PLL; an odd-/even-field signal; Hsync and Vsync out signals; a count of Hsyncs per Vsync; and a programmable SOG output. The main sync processing blocks are the sync slicer, sync separator, Hsync filter, Hsync regenerator, Vsync filter, and Coast generator.

The sync slicer extracts the sync signal from the green graphics or luminance video signal that is connected to the SOGIN input and outputs a digital composite sync. The sync separator's task is to extract Vsync from the composite sync signal, which can come from either the sync slicer or the Hsync input. The Hsync filter is used to eliminate any extraneous pulses from the Hsync or SOGIN inputs, outputting a clean, low-jitter signal that is appropriate for mode detection and clock generation. The Hsync regenerator is used to recreate a clean, although not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync. The Vsync filter is used to eliminate spurious Vsyncs, maintain a stable timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output. The Coast generator creates a robust Coast signal that allows the PLL to maintain its frequency in the absence of Hsync pulses.

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the green graphics or luminance video signal that is connected to the SOGIN input. The sync signal is extracted in a two step process. First, the SOG input (typically 0.3 V below the black level) is detected and clamped to a known dc voltage. Next, the

signal is routed to a comparator with a variable trigger level (set by Register 0x1D, Bits [7:3]), but nominally 0.128 V above the clamped voltage. The sync slicer output is a digital composite sync signal containing both Hsync and Vsync information (see Figure 9).



- ¹ACTIVITY DETECT
- ²POLARITY DETECT
- ³REGENERATED HSYNC
- ⁴FILTERED HSYNC
- ⁵SET POLARITY

Figure 8. Sync Processing Block Diagram

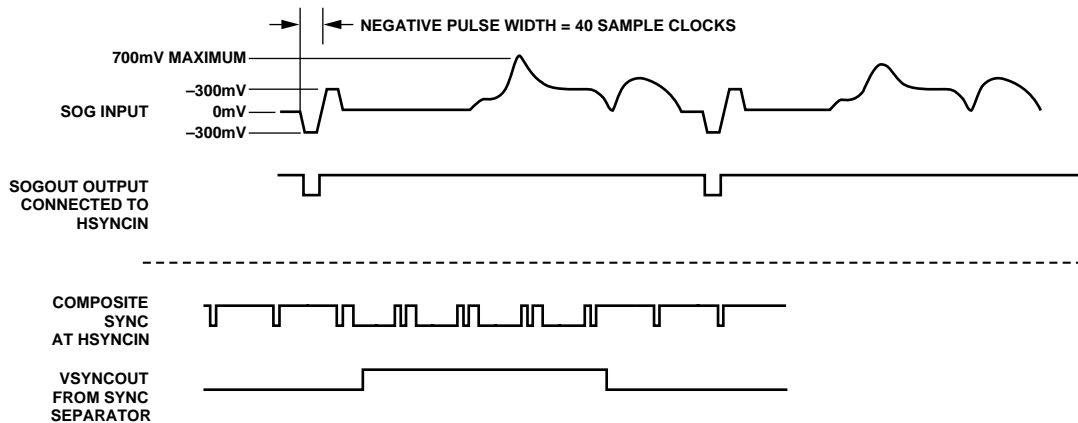


Figure 9. Sync Slicer and Sync Separator Output

Sync Separator

As part of sync processing, the sync separator's task is to extract Vsync from the composite sync signal. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. By using a digital low-pass filter and a digital comparator, it rejects pulses with small durations (such as Hsyncs and equalization pulses) and only passes pulses with large durations, such as Vsync (see Figure 9).

The threshold of the digital comparator is programmable for maximum flexibility. To program the threshold duration, write a value (N) to Register 0x11. The resulting pulse width is $N \times 200$ ns. So, if $N = 5$ the digital comparator threshold is 1 μ s. Any pulses less than 1 μ s is rejected, while any pulse greater than 1 μ s passes through.

The sync separator on the AD9880 is simply an 8-bit digital counter with a 6 MHz clock. It works independently of the polarity of the composite sync signal. Polarities are determined elsewhere on the chip. The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down until eventually reaching 0 before the next Hsync pulse arrives. The specific value of N varies for different video modes, but is always less than 255. For example with a 1 μ s width Hsync, the counter only reaches 5 (1 μ s/200 ns = 5). Now, when Vsync is present on the composite sync the counter also counts up. However, since the Vsync signal is much longer, it counts to a higher number, M. For most video modes, M is at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection, T, can be programmed through the Serial Register 0x11.

Once Vsync has been detected, there is a similar process to detect when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync finishes. Similarly to the previous case, it detects the absence of Vsync when the counter reaches the threshold count, T. In this way, it rejects noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

There are two things to keep in mind when using the sync separator. First, the resulting clean Vsync output is delayed

from the original Vsync by a duration equal to the digital comparator threshold ($N \times 200$ ns). Second, there is some variability to the 200 ns multiplier value. The maximum variability over all operating conditions is $\pm 20\%$ (160 ns to 240 ns). Since normal Vsync and Hsync pulse widths differ by a factor of about 500 or more, 20% variability is not an issue.

Hsync Filter and Regenerator

The Hsync filter is used to eliminate any extraneous pulses from the Hsync or SOGIN inputs, outputting a clean, low-jitter signal that is appropriate for mode detection and clock generation.

The Hsync regenerator is used to recreate a clean, although not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync. The Hsync regenerator has a high degree of tolerance to extraneous and missing pulses on the Hsync input, but is not appropriate for use by the PLL in creating the pixel clock because of jitter.

The Hsync regenerator runs automatically and requires no setup to operate. The Hsync filter requires the setting up of a filter window. The filter window sets a periodic window of time around the regenerated Hsync leading edge where valid Hsyncs are allowed to occur. The general idea is that extraneous pulses on the sync input occur outside of this filter window and thus are filtered out. To set the filter window timing, program a value (x) into Register 0x20. The resulting filter window time is $\pm x$ times 25 ns around the regenerated Hsync leading edge. Just as for the sync separator threshold multiplier, allow a $\pm 20\%$ variance in the 25 ns multiplier to account for all operating conditions (20 ns to 30 ns range).

A second output from the Hsync filter is a status bit (Register 0x16[0]) that tells whether extraneous pulses are present on the incoming sync signal or not. Extraneous pulses are often included for copy protection purposes; this status bit can be used to detect that.

The filtered Hsync (rather than the raw Hsync/SOGIN signal) for pixel clock generation by the PLL is controlled by Register 0x21[6]. The regenerated Hsync (rather than the raw Hsync/SOGIN signal) for sync processing is controlled by Register 0x21[7]. Use of the filtered Hsync and regenerated Hsync is recommended. See Figure 10 for an illustration of a filtered Hsync.

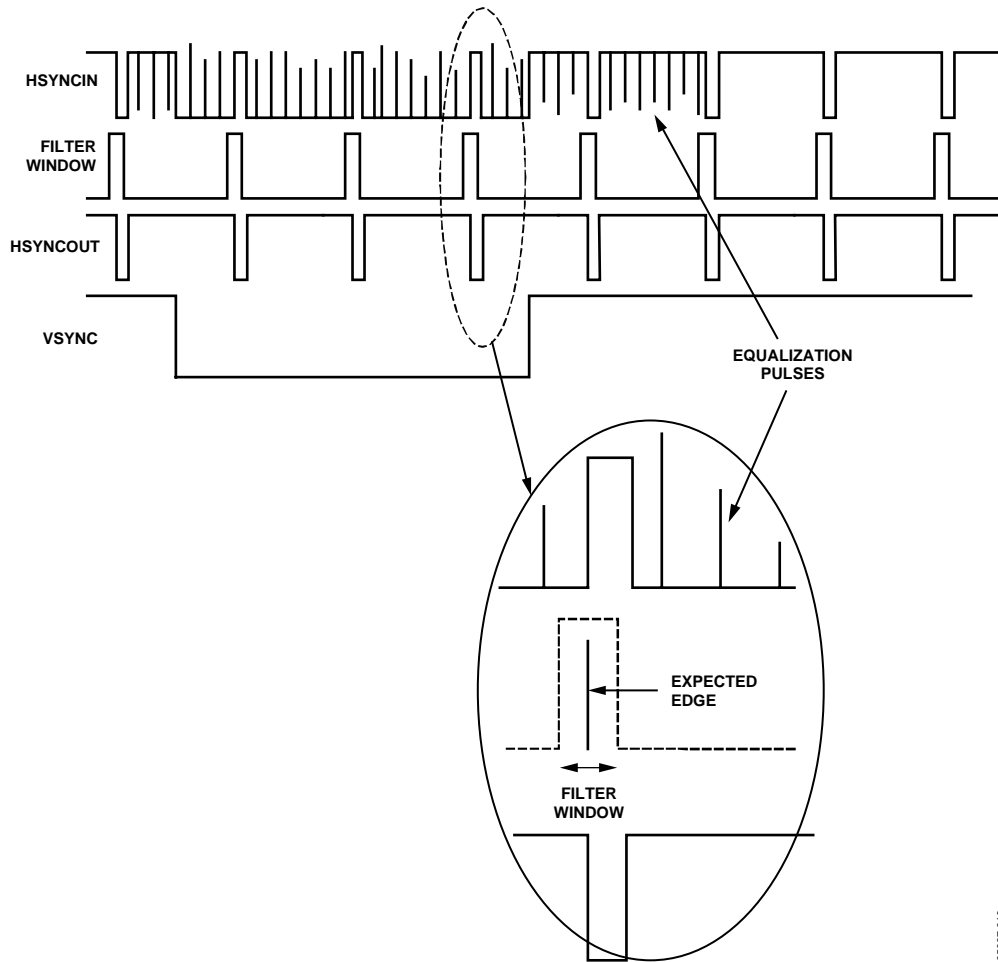


Figure 10. Sync Processing Filter

05087-010

Vsync Filter and Odd/Even Fields

The Vsync filter is used to eliminate spurious Vsyncs, maintain a consistent timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output.

The filter works by examining the placement of Vsync with respect to Hsync and, if necessary, slightly shifting it in time at the VSOUT output. The goal is to keep the Vsync and Hsync leading edges from switching at the same time, eliminating confusion as to when the first line of a frame occurs. Enabling the Vsync filter is done with Register 0x21[5]. Use of the Vsync filter is recommended for all cases, including interlaced video, and is required when using the Hsync per Vsync counter. Figure 12 illustrates even/odd field determination in two situations.

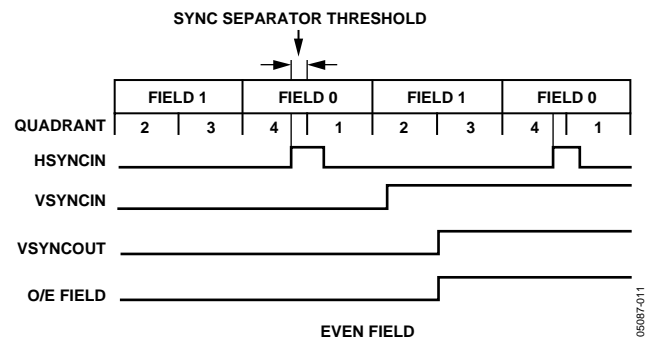


Figure 11. SYNC SEPARATOR THRESHOLD

05087-011

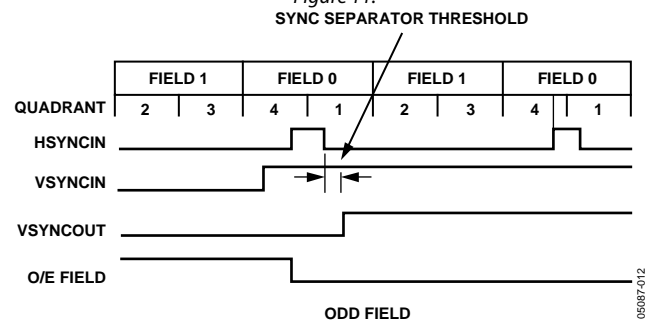


Figure 12. Vsync Filter—Odd/Even

05087-012

HDMI RECEIVER

The HDMI receiver section of the AD9880 allows the reception of a digital video stream, which is backward-compatible with DVI and able to accommodate not only video of various formats (RGB, YCrCb 4:4:4, 4:2:2), but also up to eight channels of audio. Infoframes are transmitted carrying information about the video format, audio clocks, and many other items necessary for a monitor to utilize fully the information stream available.

The earlier digital visual interface (DVI) format was restricted to an RGB 24 bit color space only. Embedded in this data stream were Hsyncs, Vsyncs and display enable (DE) signals, but no audio information. The HDMI specification allows transmission of all the DVI capabilities, but adds several YCrCb formats that make the inclusion of a programmable color space converter (CSC) a very desirable feature. With this, the scaler following the AD9880 can specify that it always wishes to receive a particular format, for instance, 4:2:2 YCrCb regardless of the transmitted mode. If RGB is sent, the CSC can easily convert that to 4:2:2 YCrCb while relieving the scaler of this task.

In addition, the HDMI specification supports the transmission of up to eight channels of S/PDIF or I2S audio. The audio information is packetized and transmitted during the video blanking periods along with specific information about the clock frequency. Part of this audio information (Audio Infoframe) tells the user how many channels of audio, where they should be placed, information regarding the source (make, model), and other data.

DE GENERATOR

The AD9880 has an onboard generator for DE, for start of active video (SAV), and for end of active video (EAV), all of which are necessary for describing the complete data stream for a BT656 compatible output. In addition to this particular output, it is possible to generate the DE for cases in which a scaler is not planned to be used. This signal alerts the following circuitry as to which are displayable video pixels.

4:4:4 TO 4:2:2 FILTER

The AD9880 contains a filter which allows it to convert a signal from YCrCb 4:4:4 to YCrCb 4:2:2 while maintaining the maximum accuracy and fidelity of the original signal.

Input Color space to Output Color space

The AD9880 can accept a wide variety of input formats and either retain that format or convert to another. Input formats supported are

- 4:4:4 YCrCb 8 bit
- 4:2:2 YCrCb 8, 10, and 12 bit
- RGB 8-bit

Output modes supported are

- 4:4:4 YCrCb 8 bits
- 4:2:2 YCrCb 8, 10, and 12 bits
- Dual 4:2:2 YCrCb 8 bits.

Color space Conversion (CSC) Matrix

The color space conversion (CSC) matrix in the AD9880 consists of three identical processing channels. In each channel, three input values are multiplied by three separate coefficients. Also included are an offset value for each row of the matrix and a scaling multiple for all values. Each value has a 13 bit two's complement resolution to ensure the signal integrity is maintained. The CSC is designed to run at speeds up to 150 MHz supporting resolutions up to 1080 p at 60 Hz. With any-to-any color space support, formats such as RGB, YUV, YCbCr, and others are supported by the CSC.

The main inputs, R_{in} , G_{in} , and B_{in} come from the 8- to 12-bit inputs from each channel. These inputs are based on the input format detailed in Table 7 to Table 15. The mapping of these inputs to the CSC inputs is shown in Table 9.

Table 9. CSC Port Mapping

| Input Channel | CSC Input Channel |
|---------------|-------------------|
| R/CR | R_{IN} |
| Gr/Y | G_{IN} |
| B/CB | B_{IN} |

One of the three channels is represented in Figure 13. In each processing channel the three inputs are multiplied by three separate coefficients marked a_1 , a_2 , and a_3 . These coefficients are divided by 4096 to obtain nominal values ranging from -0.9998 to $+0.9998$. The variable labeled a_4 is used as an offset control. The CSC_mode setting is the same for all three processing channels. This multiplies all coefficients and offsets by a factor of 2^{CSC_mode} .

The functional diagram for a single channel of the CSC as shown in Figure 13 is repeated for the remaining G and B channels. The coefficients for these channels are b_1 , b_2 , b_3 , b_4 , c_1 , c_2 , c_3 , and c_4 .

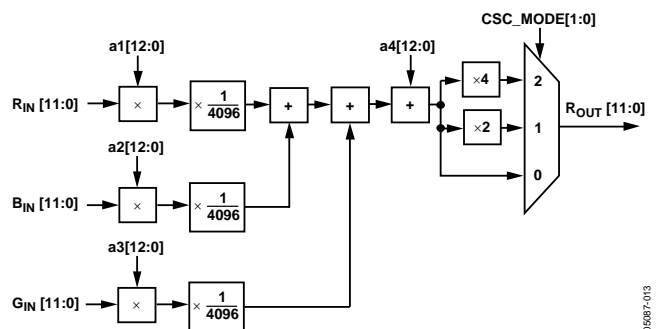


Figure 13. Single CSC Channel

A programming example and register settings for several common conversions are listed in the Color Space Converter (CSC) Common Settings.

For a detailed functional description and more programming examples, please refer to the application note AN-795, AD9880 Color space Converter User's Guide.

AUDIO PLL SETUP

Data contained in the Audio Inframes among other registers define for the AD9880 HDMI receiver not only the type of audio, but the sample frequency. It also contains information about the N and CTS values used to recreate the clock. With this information it is possible to regenerate the audio sampling frequency. The audio clock is regenerated by dividing the 20-bit CTS value into the TMDS clock, then multiplying by the 20-bit N value. This yields a multiple of the f_s (sampling frequency) of either $128 \times f_s$ or $256 \times f_s$. It is possible for this to be specified up to $1024 \times f_s$.

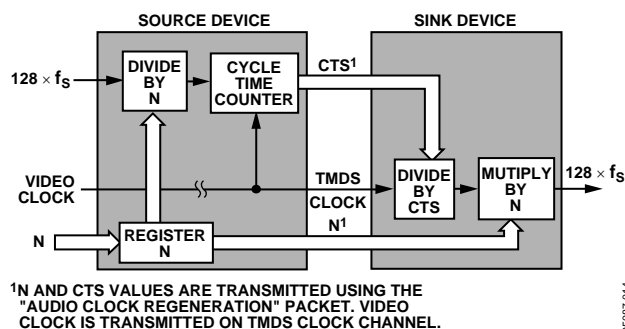


Figure 14. N and CTS for Audio Clock

AUDIO BOARD LEVEL MUTING

The audio can be muted through the Inframes or locally via the serial bus registers. This can be controlled with Register R0x57, Bits [7:4].

AVI Inframes

Contained within the HDMI TMDS transmission are Inframes containing specific information for the monitor such as

- Audio information
 - 2 to 8 channels of audio identified
 - Audio coding
 - Audio sampling frequency

- Speaker placement
- N and CTS values (for reconstruction of the audio)
- Muting
- Source information
 - CD
 - SACD
 - DVD
- Video information
 - Video ID Code (per CEA861B)
 - Color space
 - Aspect ratio
 - Horizontal and vertical bar information
 - MPEG frame information (I, B, or P frame)
- Vendor (transmitter source) information
 - Vendor name and product model

This information is the fundamental difference between DVI and HDMI transmissions and is located in read-only registers R0x5A to R0xEE. In addition to this information, registers are provided that indicate that new information has been received. Registers with addresses ending in 0xX7 or 0xXF beginning at R0x87 contain the new data flags (NDF) information. All of these registers contain the same information and all are reset once any of them are read. Although there is no external interrupt signal, it is very straightforward for the user to read any of these registers and see if there is new information to be processed.

TIMING DIAGRAMS

The following timing diagrams show the operation of the AD9880. The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally. There is a pipeline in the AD9880, which must be flushed before valid data becomes available. This means six data sets are presented before valid data is available.

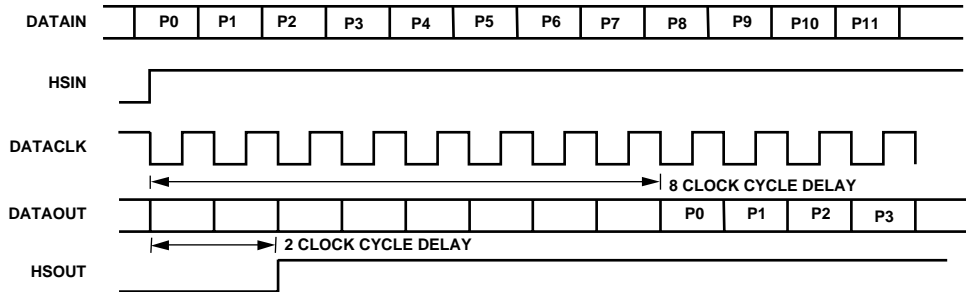
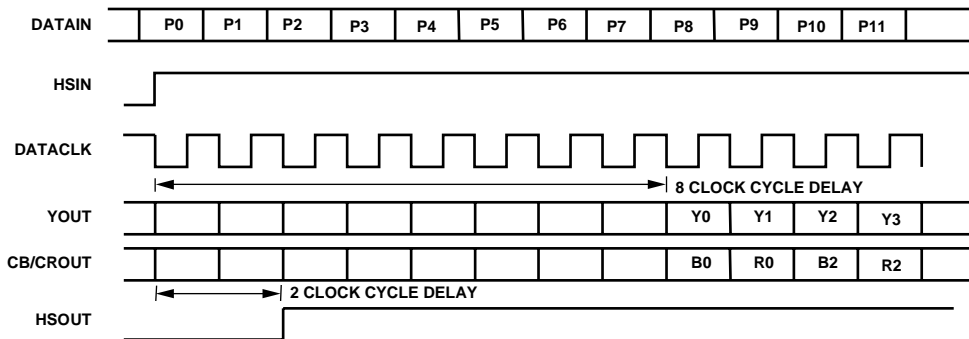


Figure 15. RGB ADC Timing

06087-015



1. PIXEL AFTER HSOUT CORRESPONDS TO BLUE INPUT.
2. EVEN NUMBER OF PIXEL DELAY BETWEEN HSOUT AND DATAOUT.

Figure 16. YCrCb ADC Timing

06087-016

Table 10.

| Port | Red | | | | | | | | Green | | | | | | | | Blue | | | | | | | |
|-----------|----------------------------|---|---|---|---------------|---|---|---|---------------|---|---|---|-------------------------|---|---|---|------------------------|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 4:4:4 | Red/Cr [7:0] | | | | | | | | Green/Y [7:0] | | | | | | | | Blue/Cb [7:0] | | | | | | | |
| 4:2:2 | CbCr [7:0] | | | | | | | | Y [7:0] | | | | | | | | DDR 4:2:2 ↑ CbCr ↓ Y,Y | | | | | | | |
| 4:4:4 DDR | DDR ↑ ¹ G [3:0] | | | | DDR ↑ B [7:4] | | | | DDR ↑ B [3:0] | | | | DDR 4:2:2 ↑ CbCr [11:0] | | | | | | | | | | | |
| | DDR ↓ R [7:0] | | | | | | | | DDR ↓ G [7:4] | | | | DDR 4:2:2 ↓ Y,Y [11:0] | | | | | | | | | | | |
| 4:2:2-12 | CbCr [11:0] | | | | | | | | Y [11:0] | | | | | | | | | | | | | | | |

¹ Arrows in the table indicate clock edge. Rising edge of clock = ↑, falling edge = ↓.

2-WIRE SERIAL REGISTER MAP

The AD9880 is initialized and controlled by a set of registers that determines the operating modes. An external controller is employed to write and read the control registers through the 2-wire serial interface port.

Table 11. Control Register Map

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|--|---|---|---|
| 0x00 | Read | [7:0] | 00000000 | Chip Revision | Chip revision ID. Revision is read [7:4], [3:0]. |
| 0x01 | Read/Write | [7:0] | 01101001 | PLL Divider MSB | PLL feedback divider value MSB. |
| 0x02 | Read/Write | [7:4] | 1101**** | PLL Divider | PLL feedback divider value. |
| 0x03 | Read/Write | [7:6] [5:3] [2] | 01***** **001*** *****0** | VCO Range Charge Pump External Clock Enable | VCO range. Charge pump current control for PLL. Selects the external clock input rather than the internal PLL clock. |
| 0x04 | Read/Write | [7:3] | 10000*** | Phase Adjust | Selects the clock phase to use for the ADC clock. |
| 0x05 | Read/Write | [7:0] | 10000000 | Red Gain | Controls the gain of the red channel PGA. 0 = low gain, 255 = high gain. |
| 0x06 | Read/Write | [7:0] | 10000000 | Green Gain | Controls the gain of the green channel PGA. 0 = low gain, 255 = high gain. |
| 0x07 | Read/Write | [7:0] | 10000000 | Blue Gain | Controls the gain of the blue channel PGA. 0 = low gain, 255 = high gain. |
| 0x08 | Read/Write | [7:0] | 00000000 | Red Offset Adjust | User adjustment of auto offset. Allows user control of brightness. |
| 0x09 | Read/Write | [7:0] | 10000000 | Red Offset | Red offset/target code. 0 = small offset, 255 = large offset. |
| 0x0A | Read/Write | [7:0] | 00000000 | Green Offset Adjust | User adjustment of auto offset. Allows user control of brightness. |
| 0x0B | Read/Write | [7:0] | 10000000 | Green Offset | Green offset/target code. 0 = small offset, 255 = large offset. |
| 0x0C | Read/Write | [7:0] | 00000000 | Blue Offset Adjust | User adjustment of auto offset. Allows user control of brightness. |
| 0x0D | Read/Write | [7:0] | 10000000 | Blue Offset | Blue offset/target code. 0 = small offset, 255 = large offset. |
| 0x0E | Read/Write | [7:0] | 00100000 | Sync Separator Threshold | Selects the maximum Hsync pulse width for composite sync separation. |
| 0x0F | Read/Write | [7:2] | 010000** | SOG Comparator Threshold Enter | The enter level for the SOG slicer. Must be less than or equal to the exit level. |
| 0x10 | Read/Write | [7:2] | 010000** | SOG Comparator Threshold Exit | The exit level for the SOG slicer. Must be greater than or equal to the enter level. |
| 0x11 | Read/Write | [7] [6] [5] [4] [3] [2] [1] [0] | 0***** *0***** **0***** ***0***** ****0*** *****0** *****0* *****0 | Hsync Source Hsync Source Override Vsync Source Vsync Source Override Channel Select Channel Select Override Interface Select Interface Override | 0 = Hsync. 1 = SOG. 0 = auto Hsync source. 1 = manual Hsync source. 0 = Vsync. 1 = Vsync from SOG. 0 = auto Hsync source. 1 = manual Hsync source. 0 = Channel 0. 1 = Channel 1. 0 = autochannel select. 1 = manual channel select. 0 = analog interface. 1 = digital interface. 0 = auto-interface select. 1 = manual interface select. |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|-------------------------|---|
| 0x12 | Read/Write | [7] | 1***** | Input Hsync Polarity | 0 = active low. 1 = active high. |
| | | [6] | *0***** | Hsync Polarity Override | 0 = auto Hsync polarity. 1 = manual Hsync polarity. |
| | | [5] | **1***** | Input Vsync Polarity | 0 = active low. 1 = active high. |
| | | [4] | ***0**** | Vsync Polarity Override | 0 = auto Vsync polarity. 1 = manual Vsync polarity. |
| | | [3] | ****1*** | Input Coast Polarity | 0 = active low. 1 = active high. |
| | | [2] | *****0** | Coast Polarity Override | 0 = auto Coast polarity. 1 = manual Coast polarity. |
| | | [1] | *****0* | Coast Source | 0 = internal Coast. 1 = external Coast. |
| | | [0] | *****1 | Filter Coast Vsync | 0 = Use raw Vsync for Coast generation. 1 = Use filtered Vsync for Coast generation. |
| 0x13 | Read/Write | [7:0] | 00000000 | Precoast | Number of Hsync periods before Vsync to Coast. |
| 0x14 | Read/Write | [7:0] | 00000000 | Postcoast | Number of Hsync periods after Vsync to Coast. |
| 0x15 | Read | [7] | 0***** | Hsync 0 Detected | 0 = not detected. 1 = detected. |
| | | [6] | *0***** | Hsync 1 Detected | 0 = not detected. 1 = detected. |
| | | [5] | **0***** | Vsync 0 Detected | 0 = not detected. 1 = detected. |
| | | [4] | ***0**** | Vsync 1 Detected | 0 = not detected. 1 = detected. |
| | | [3] | ****0*** | SOG 0 Detected | 0 = not detected. 1 = detected. |
| | | [2] | *****0** | SOG1 Detected | 0 = not detected. 1 = detected. |
| | | [1] | *****0* | Coast Detected | 0 = not detected. 1 = detected. |
| 0x16 | Read | [7] | 0***** | Hsync 0 Polarity | 0 = active low. 1 = active high. |
| | | [6] | *0***** | Hsync 1 Polarity | 0 = active low. 1 = active high. |
| | | [5] | **0***** | Vsync 0 Polarity | 0 = active low. 1 = active high. |
| | | [4] | ***0**** | Vsync 1 Polarity | 0 = active low. 1 = active high. |
| | | [3] | ****0*** | Coast Polarity | 0 = active low. 1 = active high. |
| | | [2] | *****0** | Pseudo Sync Detected | 0 = not detected. 1 = detected. |
| | | [1] | *****0* | Sync Filter Locked | 0 = not locked. 1 = locked. |
| | | [0] | *****0 | Bad Sync Detect | 0 = not detected. 1 = detected. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|------------------------------|---|
| 0x17 | Read | [3:0] | ****0000 | Hsyncs Per Vsync MSB | MSB of Hsyncs per Vsync. |
| 0x18 | Read | [7:0] | 00000000 | Hsyncs Per Vsync | Hsyncs per Vsync count. |
| 0x19 | Read/Write | [7:0] | 00001000 | Clamp Placement | Number of pixel clocks after trailing edge of Hsync to begin clamp. |
| 0x1A | Read/Write | [7:0] | 00010100 | Clamp Duration | Number of pixel clocks to clamp. |
| 0x1B | Read/Write | [7] | 0***** | Red Clamp Select | 0 = clamp to ground. 1 = clamp to midscale. |
| | | [6] | *0***** | Green Clamp Select | 0 = clamp to ground. 1 = clamp to midscale. |
| | | [5] | **0***** | Blue Clamp Select | 0 = clamp to ground. 1 = clamp to midscale. |
| | | [4] | ***0**** | Clamp During Coast Enable | 0 = don't clamp during Coast. 1 = clamp during Coast. |
| | | [3] | ****0*** | Clamp Disable | 0 = internal clamp enabled. 1 = internal clamp disabled. |
| | | [1] | *****1* | Programmable Bandwidth | 0 = low bandwidth. 1 = full bandwidth. |
| | | [0] | *****0 | Hold Auto Offset | 0 = normal auto offset operation. 1 = hold current offset value. |
| 0x1C | Read/Write | [7] | 0***** | Auto Offset Enable | 0 = manual offset. 1 = auto offset using offset as target code. |
| | | [6:5] | *10***** | Auto Offset Update Mode | 00 = every clamp. 01 = every 16 clamps. 10 = every 64 clamps. 11 = Every Vsync. |
| | | [4:3] | ***01*** | Difference Shift Amount | 00 = 100% of difference used to calculate new offset. 01 = 50%. 10 = 25%. 11 = 12.5%. |
| | | [2] | *****1** | Auto Jump Enable | 0 = normal operation. 1 = if code > 15 codes off then offset is jumped to the predicted offset necessary to fix the > 15 code mismatch. |
| | | [1] | *****1* | Post Filter Enable | 0 = disable post filter. 1 = enable post filter. Post filter reduces update rate by 1/6 and requires that all six updates recommend a change before changing the offset. This prevents unwanted offset changes. |
| | | [0] | *****0 | Toggle Filter Enable | The toggle filter looks for the offset to toggle back and forth and holds it if triggered. This is to prevent toggling in case of missing codes in the PGA. |
| 0x1D | Read/Write | [7:0] | 00001000 | Slew Limit | Limits the amount the offset can change by in a single update. |
| 0x1E | Read/Write | [7:0] | 32 | Sync Filter Lock Threshold | Number of clean Hsyncs required for sync filter to lock. |
| 0x1F | Read/Write | [7:0] | 50 | Sync Filter Unlock Threshold | Number of missing Hsyncs required to unlock the sync filter. Counter counts up if Hsync pulse is missing and down for a good Hsync. |
| 0x20 | Read/Write | [7:0] | 50 | Sync Filter Window Width | Width of the window in which Hsync pulses are allowed. |
| 0x21 | Read/Write | [7] | 1***** | SP Sync Filter Enable | Enables Coast, Vsync duration, and Vsync filter to use the regenerated Hsync rather than the raw Hsync. |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|--------------------------|--|
| | | [6] | *1***** | PLL Sync Filter Enable | Enables the PLL to use the filtered Hsync rather than the raw Hsync. This clips any bad Hsyncs, but does not regenerate missing pulses. |
| | | [5] | **0***** | Vsync Filter Enable | Enables the Vsync filter. The Vsync filter gives a predictable Hsync/Vsync timing relationship but clips one Hsync period off the leading edge of Vsync. |
| | | [4] | ***0**** | Vsync Duration Enable | Enables the Vsync duration block. This block can be used if necessary to restore the duration of a filtered Vsync. |
| | | [3] | **** 1*** | Auto Offset Clamp Mode | 0 = auto offset measures code during clamp. 1 = auto offset measures code (10 or 16) clock cycles after end of clamp for 6 clock cycles. |
| | | [2] | **** *1** | Auto Offset Clamp Length | Sets delay after end of clamp for auto offset clamp mode = 1. 0 = Delay is 10 clock cycles. 1 = Delay is 16 clock cycles. |
| 0x22 | Read/Write | [7:0] | 4 | Vsync Duration | Vsync Duration. |
| 0x23 | Read/Write | [7:0] | 32 | Hsync Duration | Hsync Duration. Sets the duration of the output Hsync in pixel clocks. |
| 0x24 | Read/Write | [7] | 1***** | Hsync Output Polarity | Output Hsync Polarity (both DVI and Analog). 0 = active low out. 1 = active high out. |
| | | [6] | *1***** | Vsync Output Polarity | Output Vsync polarity (both DVI and analog). 0 = active low out. 1 = active high out. |
| | | [5] | **1***** | DE Output Polarity | Output DE polarity (both DVI and analog) . 0 = active low out. 1 = active high out. |
| | | [4] | ***1**** | Field Output Polarity | Output field polarity (both DVI and analog). 0 = active low out. 1 = active high out. |
| | | [3] | ****1*** | SOG Output Polarity | Output SOG polarity (analog only). 0 = active low out. 1 = active high out. |
| | | [2:1] | *****11* | SOG Output Select | Selects signal present on SOG output. 00 = SOG (SOG0 or SOG1). 01 = Raw Hsync (HSYNC0 or HSYNC1). 10 = Regenerated sync. 11 = Hsync to PLL. |
| | | [0] | *****0 | Output CLK Invert | 0 = Don't invert clock out. 1 = Invert clock out. |
| 0x25 | Read/Write | [7:6] | 01***** | Output CLK Select | Select which clock to use on output pin. 1× CLK is divided down from TMDS clock input when pixel repetition is in use. 00 = ½× CLK. 01 = 1× CLK. 10 = 2× CLK. 11 = 90° phase 1X CLK. |
| | | [5:4] | **11**** | Output Drive Strength | Set the drive strength of the outputs. 00 = lowest, 11 = highest. |
| | | [3:2] | ****00** | Output Mode | Selects which pins the data comes out on. 00 = 4:4:4 mode (normal). 01 = 4:2:2 + DDR 4:2:2 on blue. 10 = DDR 4:4:4 + DDR 4:2:2 on blue. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|-------------------------|---|
| | | [1] | *****1* | Primary Output Enable | 11 = 12-bit 4:2:2 (HDMI can have 12-bit 4:2:2 data). Enables primary output. |
| | | [0] | *****0 | Secondary Output Enable | Enables secondary output (DDR 4:2:2 in Output Modes 1 and 2). |
| 0x26 | Read/Write | [7] | 0***** | Output Three-State | Three-state the outputs. |
| | | [6] | *0***** | SOG Three-State | Three-state the SOG output. |
| | | [5] | **0***** | SPDIF Three-State | Three-state the SPDIF output. |
| | | [4] | ***0**** | I2S Three-State | Three-state the I2S output and the MCLK out. |
| | | [3] | ****1*** | Power-Down Pin Polarity | Sets polarity of power-down pin. 0 = active low. 1 = active high. |
| | | [2:1] | *****00* | Power-Down Pin Function | Selects the function of the power-down pin. 00 = power-down. 01 = power-down and three-state SOG. 10 = three-state outputs only. 11 = three-state outputs and SOG. |
| | | [0] | *****0 | Power-Down | 0 = normal. 1 = power-down. |
| 0x27 | Read/Write | [7] | 1***** | Auto Power-Down Enable | 0 = disable auto low power state. 1 = enable auto low power state. |
| | | [6] | *0***** | HDCP A0 | Sets the LSB of the address of the HDCP I ² C. Set to 1 only for a second receiver in a dual-link configuration. 0 = Use internally generated MCLK. 1 = Use external MCLK input. |
| | | [5] | **0***** | MCLK External Enable | If an external MCLK is used then it must be locked to the video clock according to the CTS and N available in the I ² C. Any mismatch between the internal MCLK and the input MCLK results in dropped or repeated audio samples. |
| | | [4] | ***0**** | BT656 EN | Enables EAV/SAV codes to be inserted into the video output data. |
| | | [3] | ****0*** | Force DE Generation | Allows use of the internal DE generator in DVI mode. |
| | | [2:0] | *****000 | Interlace Offset | Sets the difference (in Hsyncs) in field length between Field 0 and Field 1. |
| 0x28 | Read/Write | [7:2] | 011000** | VS Delay | Sets the delay (in lines) from Vsync leading edge to the start of active video. |
| | | [1:0] | *****01 | HS Delay MSB | MSB, Register 0x29. |
| 0x29 | Read/Write | [7:0] | 00000100 | HS Delay | Sets the delay (in pixels) from Hsync leading edge to the start of active video. |
| 0x2A | Read/Write | [3:0] | ****0101 | Line Width MSB | MSB, Register 0x2B. |
| 0x2B | Read/Write | [7:0] | 00000000 | Line Width | Sets the width of the active video line (in pixels). |
| 0x2C | Read/Write | [3:0] | ****0010 | Screen Height MSB | MSB, Register 0x2D. |
| 0x2D | Read/Write | [7:0] | 11010000 | Screen Height | Sets the height of the active screen (in lines). |
| 0x2E | Read/Write | [7] | 0***** | Ctrl EN | Allows Ctrl [3:0] to be output on the I2s data pins. 00 = I2S mode. |
| | | [6:5] | *00***** | I2S Out Mode | 01 = right-justified. 10 = left-justified. 11 = raw IEC60958 mode. |
| | | [4:0] | ***11000 | I2S Bit Width | Sets the desired bit width for right-justified mode. |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|------------------------|--|
| 0x2F | Read | [6] | *0***** | TMD5 Sync Detect | Detects a TMD5 DE. |
| | | [5] | **0***** | TMD5 Active | Detects a TMD5 clock. |
| | | [4] | ***0**** | AV Mute | Gives the status of AV mute based on general control packets. |
| | | [3] | ****0*** | HDCP Keys Read | Returns 1 when read of EEPROM keys is successful. |
| | | [2:0] | *****000 | HDMI Quality | Returns quality number based on DE edges. |
| 0x30 | Read | [6] | *0***** | HDMI Content Encrypted | This bit is high when HDCP decryption is in use (content is protected). The signal goes low when HDCP is not being used. Customers can use this bit to determine whether or not to allow copying of the content. The bit should be sampled at regular intervals since it can change on a frame by frame basis. |
| | | [5] | **0***** | DVI Hsync Polarity | Returns DVI Hsync polarity. |
| | | [4] | ***0**** | DVI Vsync Polarity | Returns DVI Vsync polarity. |
| | | [3:0] | ****0000 | HDMI Pixel Repetition | Returns current HDMI pixel repetition amount. 0 = 1x, 1 = 2x, ... The clock and data outputs automatically de-repeat by this value. |
| 0x31 | Read/Write | [7:4] | 1001**** | MV Pulse Max | Sets the max pseudo sync pulse width for Macrovision detection. |
| | | [3:0] | ****0110 | MV Pulse Min | Sets the min pseudo sync pulse width for Macrovision detection. |
| 0x32 | Read/Write | [7] | 0***** | MV Oversample En | Tells the Macrovision detection engine whether we are oversampling or not. |
| | | [6] | *0***** | MV Pal En | Tells the Macrovision detection engine to enter PAL mode. |
| | | [5:0] | **001101 | MV Line Count Start | Sets the start line for Macrovision detection. |
| 0x33 | Read/Write | [7] | 1***** | MV Detect Mode | 0 = standard definition. 1 = progressive scan mode. |
| | | [6] | *0***** | MV Settings Override | 0 = use hard coded settings for line counts and pulse widths. 1 = use I ² C values for these settings. |
| | | [5:0] | **010101 | MV Line Count End | Sets the end line for Macrovision detection. |
| 0x34 | Read/Write | [7:6] | 10***** | MV Pulse Limit Set | Sets the number of pulses required in the last 3 lines (SD mode only). |
| | | [5] | **0***** | Low Freq Mode | Sets whether the Audio PLL is in low freq. mode or not. Low frequency mode should only be set for pixel clocks <80 MHz. |
| | | [4] | ***0**** | Low Freq Override | Allows the previous bit to be used to set low frequency mode rather than the internal auto-detect. |
| | | [3] | ****0*** | Up Conversion Mode | 0 = Repeat Cr and Cb values. 1 = Interpolate Cr and Cb values. |
| | | [2] | *****0** | CrCb Filter Enable | Enables the FIR filter for 4:2:2 CrCb output. |
| | | [1] | *****0* | CSC_Enable | Enables the color space converter (CSC). The default settings for the CSC provide HDTV to RGB conversion. Sets the fixed point position of the CSC coefficients. Including the A4, B4, C4, offsets. |
| 0x35 | Read/Write | [6:5] | *01* **** | CSC_Mode | 00 = ±1.0, -4096 to 4095 01 = ±2.0, -8192 to 8190 1x = ±4.0, -16384 to 16380 |
| | | [4:0] | ***01100 | CSC_Coeff_A1 MSB | MSB, Register 0x36. |
| 0x36 | Read/Write | [7:0] | 01010010 | CSC_Coeff_A1 | Color space converter (CSC) coefficient for equation: R _{OUT} = (A1 × R _{IN}) + (A2 × G _{IN}) + (A3 × B _{IN}) + A4 G _{OUT} = (B1 × R _{IN}) + (B2 × G _{IN}) + (B3 × B _{IN}) + B4 B _{OUT} = (C1 × R _{IN}) + (C2 × G _{IN}) + (C3 × B _{IN}) + C4 |
| 0x37 | Read/Write | [4:0] | ***01000 | CSC_Coeff_A2 MSB | MSB, Register 0x38. |
| 0x38 | Read/Write | [7:0] | 00000000 | CSC_Coeff_A2 | Color space converter (CSC) coefficient for equation: R _{OUT} = (A1 × R _{IN} + (A2 × G _{IN}) + (A3 × B _{IN}) + A4 G _{OUT} = (B1 × R _{IN}) + (B2 × G _{IN}) + (B3 × B _{IN}) + B4 B _{OUT} = (C1 × R _{IN}) + (C2 × G _{IN}) + (C3 × B _{IN}) + C4 |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|------------------|--|
| 0x39 | Read/Write | [4:0] | ***00000 | CSC_Coeff_A3 MSB | MSB, Register 0x3A. |
| 0x3A | Read/Write | [7:0] | 00000000 | CSC_Coeff_A3 | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x3B | Read/Write | [4:0] | ***11001 | CSC_Coeff_A4 MSB | MSB, Register 0x3C. |
| 0x3C | Read/Write | [7:0] | 11010111 | CSC_Coeff_A4 | Color space Converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x3D | Read/Write | [4:0] | ***11100 | CSC_Coeff_B1 MSB | MSB, Register 0x3E. |
| 0x3E | Read/Write | [7:0] | 01010100 | CSC_Coeff_B1 | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x3F | Read/Write | [4:0] | ***01000 | CSC_Coeff_B2 MSB | MSB, Register 0x40. |
| 0x40 | Read/Write | [7:0] | 00000000 | CSC_Coeff_B2 | Color space Converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x41 | Read/Write | [4:0] | ***11110 | CSC_Coeff_B3 MSB | MSB, Register 0x42. |
| 0x42 | Read/Write | [7:0] | 10001001 | CSC_Coeff_B3 | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x43 | Read/Write | [4:0] | ***00010 | CSC_Coeff_B4 MSB | MSB, Register 0x44. |
| 0x44 | Read/Write | [7:0] | 10010010 | CSC_Coeff_B4 | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x45 | Read/Write | [4:0] | ***00000 | CSC_Coeff_C1 MSB | MSB, Register 0x46. |
| 0x46 | Read/Write | [7:0] | 00000000 | CSC_Coeff_C1 | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x47 | Read/Write | [4:0] | ***01000 | CSC_Coeff_C2 MSB | MSB, Register 0x48. |
| 0x48 | Read/Write | [7:0] | 00000000 | CSC_Coeff_C2 | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x49 | Read/Write | [4:0] | ***01110 | CSC_Coeff_C3 MSB | MSB, Register 0x4A. |
| 0x4A | Read/Write | [7:0] | 10000111 | CSC_Coeff_C3 | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x4B | Read/Write | [4:0] | ***11000 | CSC_Coeff_C4 MSB | MSB, Register 0x4C. |
| 0x4C | Read/Write | [7:0] | 10111101 | CSC_Coeff_C4 | Color space Converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|----------------------|-------------------------|--|---|--|--|
| 0x50 | Read/Write | [7:0] | 00100000 | Test | Must be written to 0x20 for proper operation. |
| 0x56 | Read/Write | [7:0] | 00001111 | Test | Must be written to default 0x0F for proper operation. |
| 0x57 | Read/Write | [7] [6] [3] [2] | 0***** *0***** ****0*** *****0** | A/V Mute Override AV Mute Value Disable Video Mute Disable Audio Mute | A1 overrides the AV mute value with Bit 6. Sets AV mute value if override is enabled. Disables mute of video during AV mute. Disables mute of audio during AV mute. |
| 0x58 | Read/Write | [7] [6:4] [3] [2:0] | | MCLK PLL Enable MCLK PLL_N N_CTS_Disable MCLK FS_N | MCLK PLL enable—uses analog PLL. MCLK PLL N [2:0]—this controls the division of the MCLK out of the PLL: 0 = /1, 1 = /2, 2 = /3, 3 = /4, etc. Prevents the N/CTS packet on the link from writing to the N and CTS registers. Controls the multiple of 128 fs used for MCLK out. 0 = 128 fs, 1 = 256 fs, 2 = 384, 7 = 1024 fs. |
| 0x59 | Read/Write | [6] [5] [4] [2] [1] [0] | | MDA/MCL PU CLK Term O/R Manual CLK Term FIFO Reset UF FIFO Reset OF MDA/MCL Three-State | This disables the MDA/MCL pull-ups. Clock termination power-down override 0 = auto, 1 = manual. Clock termination: 0 = normal, 1 = disconnected. This bit resets the audio FIFO if underflow is detected. This bit resets the audio FIFO if overflow is detected. This bit three-states the MDA/MCL lines. |
| 0x5A | Read | [6:0] | | Packet Detected | These 7 bits are updated if any specific packet has been received since last reset or loss of clock detect. Normal is 0x00. Bit Data Packet Detected 0 AVI infoframe. 1 Audio infoframe. 2 SPD infoframe. 3 MPEG source infoframe. 4 ACP packets. 5 ISRC1 packets. 6 ISRC2 packets. |
| 0x5B | Read | [3] | | HDMI Mode | 0 = DVI, 1 = HDMI. |
| 0x5E | Read | [7:6] [5:3] 2 1 0 | | Channel Status | Mode = 00. All others are reserved. When Bit 1 = 0 (Linear PCM). 000 = 2 audio channels without pre-emphasis. 001 = 2 audio channels with 50/15 μ s pre-emphasis. 010 = reserved. 011 = reserved. 0 = Software for which copyright is asserted. 1 = Software for which no copyright is asserted. 0 = audio sample word represents linear PCM samples. 1 = audio sample word used for other purposes. 0 = consumer use of channel status block. |
| Audio Channel Status | | | | | |
| 0x5F | Read | [7:0] | | Channel Status Category Code | |
| 0x60 | Read | [7:4] [3:0] | | Channel Number Source Number | |
| 0x61 | Read | [5:4] [3:0] | | Clock Accuracy Sampling | Clock accuracy. 00 = Level II. 01 = Level III. 10 = Level I. 11 = reserved. 0011 = 32 kHz. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|---------------|-------------------------|--|---------------|---|---|
| | | | | Frequency | 0000 = 44.1 kHz. 1000 = 88.2 kHz. 1100 = 176.4 kHz. 0010 = 48k Hz. 1010 = 96 kHz. 1110 = 192 kHz. |
| 0x62 | Read | [3:0] | | Word Length | Word length. 0000 not specified. 0100 16 bits. 0011 17 bits. 0010 18 bits. 0001 19 bits. 0101 20 bits. 1000 not specified. 1100 20 bits. 1011 21 bits. 1010 22 bits. 1001 23 bits. 1101 24 bits. |
| 0x7B | Read | [7:0] | | CTS [19:12] | Cycle time stamp—this 20-bit value is used with the N value to regenerate an audio clock. For remaining bits see Register 0x7C and Register 0x7D. |
| 0x7C | Read | [7:0] | | CTS [11:4] | |
| 0x7D | Read Read | [7:4] [3:0] | | CTS [3:0] N [19:16] | 20-bit N used with CTS to regenerate the audio clock. For remaining bits, see Register 0x7E and Register 0x7F. |
| 0x7E | Read | [7:0] | | N [15:8] | |
| 0x7F | Read | [7:0] | | N [7:0] | |
| AVI Infoframe | | | | | |
| 0x80 | Read | [7:0] | | AVI Infoframe Version | |
| 0x81 | Read | [6:5] 4 [3:2] [1:0] | | Active Format Information Status Bar Information Scan Information | Y [1:0] Indicates RGB, 4:2:2 or 4:4:4. 00 = RGB. 01 = YCbCr 4:2:2. 10 = YCbCr 4:4:4. Active format information present. 0 = no data. 1 = active format information valid. B [1:0]. 00 = no bar information. 01 = horizontal bar information valid. 10 = vertical bar information valid. 11 = horizontal and vertical bar information valid. S [1:0]. 00 = no information. 01 = overscanned (television). 10 = underscanned (computer). |
| 0x82 | Read | [7:6] [5:4] | | Colorimetry Picture Aspect Ratio | C [1:0]. 00 = no data. 01 = SMPTE 170M, ITU601. 10 = ITU709. M [1:0]. 00 = no data. |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|----------------------------|--|
| | | [3:0] | | Active Format Aspect Ratio | 01 = 4:3. 10 = 16:9. R [3:0]. 1000 = same as picture aspect ratio. 1001 = 4:3 (center). 1010 = 16:9 (center). 1011 = 14:9 (center). |
| 0x83 | Read | [1:0] | | Nonuniform Picture Scaling | SC[1:0]. 00 = no known non-uniform scaling. 01 = picture has been scaled horizontally. 10 = picture has been scaled vertically. 11 = picture has been scaled horizontally and vertically. |
| 0x84 | Read | [6:0] | | Video Identification Code | VIC [6:0] video identification code—refer to CEA EDID short video descriptors. |
| 0x85 | Read | [3:0] | | Pixel Repeat | PR [3:0]—This specifies how many times a pixel has been repeated. 0000 = no repetition—pixel sent once. 0001 = pixel sent twice (repeated once). 0010 = pixel sent 3 times. 1001 = pixel sent 10 times. 0xA—0xF reserved. |
| 0x86 | Read | [7:0] | | Active Line Start LSB | This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar. Combines with Register 0x88 for a 16 bit value. |
| 0x87 | Read | [6:0] | | New Data Flags | New data flags. These 8 bits are updated if any specific data changes. Normal (no NDFs) is 0x00. When any NDF register is read, all bits reset to 0x00. All NDF registers contain the same data. Bit Data Packet Changed 0 AVI Infoframe. 1 audio Infoframe. 2 SPD Infoframe. 3 MPEG source Infoframe. 4 ACP packets. 5 ISRC1 packets. 6 ISRC2 packets. |
| 0x88 | Read | [7:0] | | Active Line Start MSB | Active line start MSB (see Register 0x86). |
| 0x89 | Read | [7:0] | | Active Line End LSB | This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar. Combines with Register 0x8A for a 16-bit value. |
| 0x8A | Read | [7:0] | | Active Line End MSB | Active line end MSB. See Register 0x89. |
| 0x8B | Read | [7:0] | | Active Pixel Start LSB | This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar. Combines with Register 0x8C for a 16-bit value. |
| 0x8C | Read | [7:0] | | Active Pixel Start MSB | Active pixel start MSB. See Register 0x8B. |
| 0x8D | Read | [7:0] | | Active Pixel End LSB | This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar. Combines with Register 0x8E for a 16-bit value. |
| 0x8E | Read | [7:0] | | Active Pixel End MSB | Active pixel end MSB. See Register 0x8D. |
| 0x8F | Read | [6:0] | | New Data Flags | New Data Flags (see 0x87). |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-----------------------|-------------------------|-------|---------------|---------------------------------|--|
| 0x9A | Read | [7:0] | | VN2 | VN2. |
| 0x9B | Read | [7:0] | | VN3 | VN3. |
| 0x9C | Read | [7:0] | | VN4 | VN4. |
| 0x9D | Read | [7:0] | | VN5 | VN5. |
| 0x9E | Read | [7:0] | | VN6 | VN6. |
| 0x9F | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xA0 | Read | [7:0] | | VN7 | VN7. |
| 0xA1 | Read | [7:0] | | VN8 | VN8. |
| 0xA2 | Read | [7:0] | | Product Description Character 1 | Product Description Character 1 (PD1) (7-bit ASCII code)—This is the first character of 16 that contains the model number and a short description. |
| 0xA3 | Read | [7:0] | | PD2 | PD2. |
| 0xA4 | Read | [7:0] | | PD3 | PD3. |
| 0xA5 | Read | [7:0] | | PD4 | PD4. |
| 0xA6 | Read | [7:0] | | PD5 | PD5. |
| 0xA7 | Read | [7:0] | | New Data Flags | New data flags (see 0x87). |
| 0xA8 | Read | [6:0] | | PD6 | PD6. |
| 0xA9 | Read | [7:0] | | PD7 | PD7. |
| 0xAA | Read | [7:0] | | PD8 | PD8. |
| 0xAB | Read | [7:0] | | PD9 | PD9. |
| 0xAC | Read | [7:0] | | PD10 | PD10. |
| 0xAD | Read | [7:0] | | PD11 | PD11. |
| 0xAE | Read | [7:0] | | PD12 | PD12. |
| 0xAF | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xB0 | Read | [7:0] | | PD13 | PD13. |
| 0xB1 | Read | [7:0] | | PD14 | PD14. |
| 0xB2 | Read | [7:0] | | PD15 | PD15. |
| 0xB3 | Read | [7:0] | | PD16 | PD16. |
| 0xB4 | Read | [7:0] | | Source Device Information Code | This is a code that classifies the source device. 0x00 = unknown. 0x01 = Digital STB. 0x02 = DVD. 0x03 = D-VHS. 0x04 = HDD video. 0x05 = DVC. 0x06 = DSC. 0x07 = Video CD. 0x08 = Game. 0x09 = PC general. |
| 0xB7 | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| MPEG Source Infoframe | | | | | |
| 0xB8 | Read | [7:0] | | MPEG Source Infoframe Version | |
| 0xB9 | Read | [7:0] | | MB[0] | MB [0] (Lower byte of MPEG bit rate: Hz) This is the lower 8 bits of 32 bits (4 bytes) that specify the MPEG bit rate in Hz. |
| 0xBA | Read | [7:0] | | MB[1] | MB [1]. |
| 0xBB | Read | [7:0] | | MB[2] | MB [2]. |
| 0xBC | Read | [7:0] | | | MB [3] (upper byte). |
| | | 4 | | Field Repeat | FR—New field or repeated field. 0 = New field or picture. 1 = Repeated field. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-----------------|---------------|--|---|
| 0xBD | Read | [1:0] | | MPEG Frame | MF [1:0] This identifies whether frame is an I, B, or P picture. 00 = unknown. 01 = I picture. 10 = B picture. 11 = P picture. |
| 0xBE | Read | [7:0] | | | Reserved. |
| 0xBF | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xC0 | Read | [7:0] | | Audio Content Protection Packet (ACP) Type | Audio content protection packet (ACP) type. 0x00 = Generic audio. 0x01 = IEC 60958-identified audio. 0x02 = DVD-audio. 0x03 = Reserved for super audio CD (SACD). 0x04 - 0xFF reserved. |
| 0xC1 | Read | [7:0] | | ACP Packet Byte 0 | ACP Packet Byte 0 (ACP_PB0). |
| 0xC2 | Read | [7:0] | | ACP_PB1 | ACP_PB1. |
| 0xC3 | Read | [7:0] | | ACP_PB2 | ACP_PB2. |
| 0xC4 | Read | [7:0] | | ACP_PB3 | ACP_PB3. |
| 0xC5 | Read | [7:0] | | ACP_PB4 | ACP_PB4. |
| 0xC6 | Read | [7:0] | | ACP_PB5 | ACP_PB5. |
| 0xC7 | Read | [6:0] | | NDF | New data flags (see 0x87). |
| 0xC8 | Read | 7 6 [2:0] | | ISRC1 Continued ISRC1 Valid ISRC1 Status | International standard recording code (ISRC1) continued—This indicates an ISRC2 packet is being transmitted. 0 = ISRC1 status BITS and PBs not valid. 1 = ISRC1 status BITS and PBs valid. 001 = starting position. 010 = intermediate position. 100 = final position. |
| 0xC9 | Read | [7:0] | | ISRC1 Packet Byte 0 | ISRC1 Packet Byte 0 (ISRC1_PB0). |
| 0xCA | Read | [7:0] | | ISRC1_PB1 | ISRC1_PB1. |
| 0xCB | Read | [7:0] | | ISRC1_PB2 | ISRC1_PB2. |
| 0xCC | Read | [7:0] | | ISRC1_PB3 | ISRC1_PB3. |
| 0xCD | Read | [7:0] | | ISRC1_PB4 | ISRC1_PB4. |
| 0xCE | Read | [7:0] | | ISRC1_PB5 | ISRC1_PB5. |
| 0xCF | Read | [6:0] | | NDF | New data flags (see 0x87). |
| 0xD0 | Read | [7:0] | | ISRC1_PB6 | ISRC1_PB6. |
| 0xD1 | Read | [7:0] | | ISRC1_PB7 | ISRC1_PB7. |
| 0xD2 | Read | [7:0] | | ISRC1_PB8 | ISRC1_PB8. |
| 0xD3 | Read | [7:0] | | ISRC1_PB9 | ISRC1_PB9. |
| 0xD4 | Read | [7:0] | | ISRC1_PB10 | ISRC1_PB10. |
| 0xD5 | Read | [7:0] | | ISRC1_PB11 | ISRC1_PB11. |
| 0xD6 | Read | [7:0] | | ISRC1_PB12 | ISRC1_PB12. |
| 0xD7 | Read | [6:0] | | NDF | New data flags (see 0x87). |
| 0xD8 | Read | [7:0] | | ISRC1_PB13 | ISRC1_PB13. |
| 0xD9 | Read | [7:0] | | ISRC1_PB14 | ISRC1_PB14. |
| 0xDA | Read | [7:0] | | ISRC1_PB15 | ISRC1_PB15. |
| 0xDB | Read | [7:0] | | ISRC1_PB16 | ISRC1_PB16. |
| 0xDC | Read | [7:0] | | ISRC2 Packet Byte 0 | ISRC2 Packet Byte 0 (ISRC2_PB0)—This is transmitted only when the ISRC_ continue bit (Register 0xC8, Bit 7) is set to 1. |
| 0xDD | Read | [7:0] | | ISRC2_PB1 | ISRC2_PB1. |
| 0xDE | Read | [7:0] | | ISRC2_PB2 | ISRC2_PB2. |
| 0xDF | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |

AD9880

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|----------------|----------------------------|
| 0xE0 | Read | [7:0] | | ISRC2_PB3 | ISRC2_PB3. |
| 0xE1 | Read | [7:0] | | ISRC2_PB4 | ISRC2_PB4. |
| 0xE2 | Read | [7:0] | | ISRC2_PB5 | ISRC2_PB5. |
| 0xE3 | Read | [7:0] | | ISRC2_PB6 | ISRC2_PB6. |
| 0xE4 | Read | [7:0] | | ISRC2_PB7 | ISRC2_PB7. |
| 0xE5 | Read | [7:0] | | ISRC2_PB8 | ISRC2_PB8. |
| 0xE6 | Read | [7:0] | | ISRC2_PB9 | ISRC2_PB9. |
| 0xE7 | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xE8 | Read | [7:0] | | ISRC2_PB10 | ISRC2_PB10. |
| 0xE9 | Read | [7:0] | | ISRC2_PB11 | ISRC2_PB11. |
| 0xEA | Read | [7:0] | | ISRC2_PB12 | ISRC2_PB12. |
| 0xEB | Read | [7:0] | | ISRC2_PB13 | ISRC2_PB13. |
| 0xEC | Read | [7:0] | | ISRC2_PB14 | ISRC2_PB14. |
| 0xED | Read | [7:0] | | ISRC2_PB15 | ISRC2_PB15. |
| 0xEE | Read | [7:0] | | ISRC2_PB16 | ISRC2_PB16. |

2-WIRE SERIAL CONTROL REGISTER DETAIL

CHIP IDENTIFICATION

0x00 7-0 *Chip Revision*

An 8-bit value that reflects the current chip revision.

PLL DIVIDER CONTROL

0x01 7-0 *PLL Divide Ratio MSBs*

The eight most significant bits of the 12-bit PLL divide ratio PLLDIV.

The PLL derives a pixel clock from the incoming Hsync signal. The pixel clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 221 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications, which assists in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (see Table 8).

However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV usually produces one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx)

The AD9880 updates the full divide ratio only when the LSBs are changed. Writing to this register by itself does not trigger an update.

0x02 7-4 *PLL Divide Ratio LSBs*

The four least significant bits of the 12-bit PLL divide ratio PLLDIV.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx).

CLOCK GENERATOR CONTROL

0x03 7-6 *VCO Range Select*

Two bits that establish the operating range of the clock generator. VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate). The PLL gives the best jitter performance at high frequencies. For this reason, to output low pixel rates and still get good jitter performance, the PLL actually operates at a higher frequency but then divides down the clock rate. Table 12 shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table 12. VCO Ranges

| VCO Range | Pixel Rate Range |
|-----------|------------------|
| 00 | 12 to 30 |
| 01 | 30 to 60 |
| 10 | 60 to 120 |
| 11 | 120 to 150 |

The power-up default value is 01.

5-3 *Charge Pump Current*

Three bits that establish the current driving the loop filter in the clock generator.

Table 13. Charge Pump Currents

| Ip2 | Ip1 | Ip0 | Current (µA) |
|-----|-----|-----|--------------|
| 0 | 0 | 0 | 50 |
| 0 | 0 | 1 | 100 |
| 0 | 1 | 0 | 150 |
| 0 | 1 | 1 | 250 |
| 1 | 0 | 0 | 350 |
| 1 | 0 | 1 | 500 |
| 1 | 1 | 0 | 750 |
| 1 | 1 | 1 | 1500 |

The power-up default value is current = 001.

2 *External Clock Enable*

This bit determines the source of the pixel clock.

Table 14. External Clock Select Settings

| EXTCLK | Function |
|--------|----------------------------------|
| 0 | Internally generated clock. |
| 1 | Externally provided clock signal |

A Logic 0 enables the internal PLL that generates the pixel clock from an externally provided Hsync.

A Logic 1 enables the external CKEXT input pin. In this mode, the PLL divide ratio (PLLDIV) is ignored. The clock phase adjusts (phase is still functional). The power-up default value is EXTCLK = 0.

0x04 7-3 Phase Adjust

These bits provide a phase adjustment for the DLL to generate the ADC clock. A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase. The power up default is 16.

INPUT GAIN**0x05 7-0 Red Channel Gain**

These bits control the programmable gain amplifier (PGA) of the red channel. The AD9880 can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting the red gain to 255 corresponds to an input range of 1.0 V. A red gain of 0 establishes an input range of 0.5 V. Note that increasing red gain results in the picture having less contrast (the input signal uses fewer of the available converter codes). The power-up default is 0x80.

0x06 7-0 Green Channel Gain

These bits control the PGA of the green channel. The AD9880 can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting the green gain to 255 corresponds to an input range of 1.0 V. A green gain of 0 establishes an input range of 0.5 V. Note that increasing green gain results in the picture having less contrast (the input signal uses fewer of the available converter codes). The power-up default is 0x80.

0x07 7-0 Blue Channel Gain

These bits control the PGA of the blue channel. The AD9880 can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting the blue gain to 255 corresponds to an input range of 1.0 V. A blue gain of 0 establishes an input range of 0.5 V. Note that increasing blue gain results in the picture having less contrast (the input signal uses fewer of the available converter codes). The power-up default is 0x80.

INPUT OFFSET**0x08 7-0 Red Channel Offset Adjust**

If clamp feedback is enabled, the 8-bit offset adjust determines the clamp code. The 8-bit offset adjust is a twos complement number consisting of 1 sign bit plus 7 bits (0x7F = +127, 0x00 = 0, 0xFF = -1, and 0x80 = -128). For example, if the register is programmed to 130d, then the output code is equal to 130d at the end of the clamp period. Note that incrementing the offset register setting by 1 LSB adds 1 LSB of offset, regardless of the clamp feedback setting.

The power-up default is 0.

0x09 7-0 Red Channel Offset

These eight bits are the red channel offset control. The offset control shifts the analog input, resulting in a change in brightness. Note that the function of the offset register depends on whether clamp feedback is enabled (Register 0x1C, Bit 7 = 1).

If clamp feedback is disabled, the offset register bits control the absolute offset added to the channel. The offset control provides a +127/-128 LSBs of adjustment range, with one LSB of offset corresponding to 1 LSB of output code. If clamp feedback is enabled these bits provide the relative offset (brightness) from the offset adjust in the previous register. The power-up default is 0x80.

0x0A 7-0 Green Channel Offset Adjust

If clamp feedback is enabled, the 8-bit offset adjust determines the clamp code. The 8-bit offset adjust is a twos complement number consisting of 1 sign bit plus 7 bits (0x7F = +127, 0x00 = 0, 0xFF = -1, and 0x80 = -128). For example, if the register is programmed to 130d, then the output code is equal to 130d at the end of the clamp period. Note that incrementing the offset register setting by 1 LSB adds 1 LSB of offset, regardless of the clamp feedback setting. The power-up default is 0.

0x0B 7-0 Green Channel Offset

These eight bits are the green channel offset control. The offset control shifts the analog input, resulting in a change in brightness. Note that the function of the offset register depends on whether clamp feedback is enabled (Register 0x1C, Bit 7 = 1).

If clamp feedback is disabled, the offset register bits control the absolute offset added to the channel. The offset control provides a +127/-128 LSBs of adjustment range, with one LSB of offset corresponding to 1 LSB of output code. If clamp feedback is enabled these bits provide the relative offset (brightness) from the offset adjust in the previous register. The power-up default is 0x80.

0x0C 7-0 Blue Channel Offset Adjust

If clamp feedback is enabled, the 8-bit offset adjust determines the clamp code. The 8-bit offset adjust is a twos complement number consisting of 1 sign bit plus 7 bits (0x7F = +127, 0x00 = 0, 0xFF = -1, and 0x80 = -128). For example, if the register is programmed to 130d, then the output code is equal to 130d at the end of the clamp period. Note that incrementing the offset register setting by 1 LSB adds 1 LSB of offset, regardless of the clamp feedback setting. The power-up default is 0.

0x0D 7-0 Blue Channel Offset
 These eight bits are the blue channel offset control. The offset control shifts the analog input, resulting in a change in brightness. Note that the function of the offset register depends on whether clamp feedback is enabled (Register 0x1C, Bit 7 = 1).

If clamp feedback is disabled, the offset register bits control the absolute offset added to the channel. The offset control provides a +127/–128 LSBs of adjustment range, with 1 LSB of offset corresponding to 1 LSB of output code. If clamp feedback is enabled these bits provide the relative offset (brightness) from the offset adjust in the previous register. The power-up default is 0x80.

SYNC

0x0E 7-0 Sync Separator
 Selects the max Hsync pulse width for composite sync separation. Power-down default is 0x20.

0x0F 7-2 SOG Comparator Threshold Enter
 The enter level for the SOG slicer. Must be < than exit level (Register 0x10). The power-up default is 0x10.

0x10 7-2 SOG Comparator Threshold Exit
 The exit level for the SOG slicer. Must be > enter level (Register 0x0F). The power-up default is 0x10.

0x11 7 Hsync Source
 0 = Hsync, 1 = SOG. The power-up default is 0. These selections are ignored if Register 0x11, Bit 6 = 0.

0x11 6 Hsync Source Override
 0 = auto Hsync source, 1 = manual Hsync source. Manual Hsync source is defined in Register 0x11, Bit 7. The power-up default is 0.

0x11 5 Vsync Source
 0 = Vsync, 1 = Vsync from SOG. The power-up default is 0. These selections are ignored if Register 0x11, Bit 4 = 0.

0x11 4 Vsync Source Override
 0 = auto Vsync source, 1 = MANUAL Vsync source. Manual Vsync source is defined in Register 0x11, Bit 5. The power-up default is 0.

0x11 3 Channel Select
 0 = Channel 0, 1 = Channel 1. The power-up default is 0. These selections are ignored if Register 0x11, Bit 2 = 0.

0x11 2 Channel Select Override
 0 = auto channel select, 1 = manual channel select. Manual channel select is defined in Register 0x11, Bit 3. The power-up default is 0.

0x11 1 Interface Select
 0 = analog interface, 1 = digital interface. The power-up default is 0. These selections are ignored if Register 0x11, Bit 0 = 0.

0x11 0 Interface Select Override
 0 = auto interface select, 1 = manual interface select. Manual interface select is defined in Register 0x11, Bit 1. The power-up default is 0.

0x12 7 Input Hsync Polarity
 0 = active low, 1 = active high. The power-up default is 1. These selections are ignored if Register 10x2, Bit 6 = 0.

0x12 6 Hsync Polarity Override
 0 = auto Hsync polarity, 1 = manual Hsync polarity. Manual Hsync polarity is defined in Register 0x11, Bit 7. The power-up default is 0.

0x12 5 Input Vsync Polarity
 0 = active low, 1 = active high. The power-up default is 1. These selections are ignored if Register 0x11, Bit 4 = 0.

0x12 4 Vsync Polarity Override
 0 = auto Vsync polarity, 1 = manual Vsync polarity. Manual Vsync polarity is defined in Register 0x11, Bit 5. The power-up default is 0.

COAST AND CLAMP CONTROLS

0x12 3 Input Coast Polarity
 0 = active low, 1 = active high. The power-up default is 1.

0x12 2 Coast Polarity Override
 0 = auto Coast polarity, 1 = manual Coast polarity. The power-up default is 0.

0x12 1 Coast Source
 0 = internal Coast, 1 = external Coast. The power-up default is 0.

0x12 0 Filter Coast Vsync
 0 = use raw Vsync for Coast generation, 1 = use filtered Vsync for Coast generation. The power-up default is 1.

0x13 7-0 Precoast

This register allows the internally generated Coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period. For Precoast to work correctly, it is necessary for the Vsync filter (0x21, Bit 5) and sync processing filter (0x21 Bit 7) both to be either enabled or disabled. The power-up default is 0.

0x14 7-0 Postcoast

This register allows the internally generated Coast signal to be applied following the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period. For Postcoast to work correctly, it is necessary for the Vsync filter (0x21, Bit 5) and sync processing filter (0x21, Bit 7) both to be either enabled or disabled. The power-up default is 0.

STATUS OF DETECTED SIGNALS

0x15 7 Hsync0 Detection Bit

Indicates if Hsync0 is active. This bit is used to indicate when activity is detected on the Hsync0 input pin. If Hsync is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = Hsync0 not active. 1 = Hsync0 is active.

Table 15. Hsync0 Detection Results

| Detect | Result |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

0x15 6 Hsync1 Detection Bit

Indicates if Hsync1 is active. This bit is used to indicate when activity is detected on the Hsync1 input pin. If Hsync is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = Hsync1 not active. 1 = Hsync1 is active.

Table 16. Hsync1 Detection Result

| Detect | Result |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

0x15 5 Vsync0 Detection Bit

Indicates if Vsync0 is active. This bit is used to indicate when activity is detected on the Vsync0 input pin. If Vsync is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = Vsync0 not active. 1 = Vsync0 is active.

Table 17. Vsync0 Detection Results

| Detect | Result |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

0x15 4 Vsync1 Detection Bit

Indicates if Vsync1 is active. This bit is used to indicate when activity is detected on the Vsync1 input pin. If Vsync is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = Vsync1 not active. 1 = Vsync1 is active.

Table 18. Vsync1 Detection Results

| Detect | Result |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

0x15 3 SOG0 Detection Bit

Indicates if SOG0 is active. This bit is used to indicate when activity is detected on the SOG0 input pin. If SOG is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = SOG0 not active. 1 = SOG0 is active.

Table 19. SOG0 Detection Result

| Detect | Result |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

0x15 2 SOG1 Detection Bit

Indicates if SOG1 is active. This bit is used to indicate when activity is detected on the SOG1 input pin. If SOG is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = SOG1 not active. 1 = SOG1 is active.

Table 20. SOG1 Detection Results

| Detect | Result |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

0x15 1 Coast Detection Bit

This bit detects activity on the EXTCLK/EXTCOAST pin. It indicates that one of the two signals is active, but it doesn't indicate if it is EXTCLK or EXTCOAST. A dc signal is not detected.

Table 21. Coast Detection Results

| Detect | Result |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

POLARITY STATUS**0x16 7 Hsync0 Polarity**

Indicates the polarity of the Hsync0 input.

Table 22. Detected Hsync0 Polarity Results

| Detect | Result |
|--------|-------------------------|
| 0 | Hsync polarity negative |
| 1 | Hsync polarity positive |

0x16 6 Hsync 1 Polarity

Indicates the polarity of the Hsync1 input.

Table 23. Detected Hsync1 Polarity Result

| Detect | Result |
|--------|-------------------------|
| 0 | Hsync polarity negative |
| 1 | Hsync polarity positive |

0x16 5 Vsync0 Polarity

Indicates the polarity of the Vsync0 input.

Table 24. Detected Vsync0 Polarity Results

| Detect | Result |
|--------|-------------------------|
| 0 | Vsync polarity negative |
| 1 | Vsync polarity Positive |

0x16 4 Vsync1 Polarity

Indicates the polarity of the Vsync1 input.

Table 25. Detected Vsync 1 Polarity Results

| Detect | Result |
|--------|-------------------------|
| 0 | Vsync polarity negative |
| 1 | Vsync polarity positive |

0x16 3 Coast Polarity

Indicates the polarity of the external Coast signal.

Table 26. Detected Coast Polarity Results

| Detect | Result |
|--------|-------------------------|
| 0 | Coast polarity negative |
| 1 | Coast polarity positive |

0x16 2 Pseudo Sync Detected**0x16 1 Sync Filter Locked**

Indicates whether sync filter is locked to periodic sync signals. 0 = sync filter locked to periodic sync signal. 1 = sync filter not locked.

Table 27. Sync Filter Lock Detect

| Detect | Result |
|--------|--|
| 0 | Sync filter locked to periodic sync signal |
| 1 | Sync filter not locked to periodic sync signal |

0x16 0 Bad Sync Detect**0x17 3-0 Hsyncs per Vsync MSBs**

The 4 MSBs of the 12-bit counter that reports the number of Hsyncs/Vsync on the active input. This is useful in determining the mode and an aid in setting the PLL divide ratio.

0x18 7-0 Hsyncs per Vsync LSBs

The 8 LSBs of the 12-bit counter that reports the number of Hsyncs/Vsync on the active input.

0x19 7-0 Clamp Placement

Number of pixel clocks after trailing edge of Hsync to begin clamp. The power-up default is 8.

0x1A 7-0 Clamp Duration

Number of pixel clocks to clamp. The power-up default is 0x14.

0x1B 7 Red Clamp Select

This bit selects whether the red channel is clamped to ground or midscale. Ground clamping is used for red in RGB applications and midscale clamping is used in YPrPb (YUV) applications.

Table 28. Red Clamp

| Select | Result |
|--------|--|
| 0 | Channel clamped to ground during clamping period |
| 1 | Channel clamped to midscale during clamping period |

The power-up default is 0.

0x1B 6 Green Clamp Select

This bit selects whether the green channel is clamped to ground or midscale. Ground clamping is normally used for green in RGB applications and YPrPb (YUV) applications.

Table 29. Green Clamp

| Select | Result |
|--------|--|
| 0 | Channel clamped to ground during clamping period |
| 1 | Channel clamped to midscale during clamping period |

The power-up default is 0.

0x1B 5 Blue Clamp Select

This bit selects whether the blue channel is clamped to ground or midscale. Ground clamping is used for blue in RGB applications and midscale clamping is used in YPrPb (YUV) applications.

Table 30. Blue Clamp

| Select | Result |
|--------|--|
| 0 | Channel clamped to ground during clamping period |
| 1 | Channel clamped to midscale during clamping period |

The power-up default is 0.

0x1B 4 Clamp During Coast

This bit permits clamping to be disabled during Coast. The reason for this is video signals are generally not at a known backporch or midscale position during Coast.

Table 31. Clamp During Coast

| Select | Result |
|--------|-----------------------------------|
| 0 | Clamping during Coast is disabled |
| 1 | Clamping during Coast is enabled |

The power-up default is 0.

0x1B 3 Clamp Disable

Table 32. Clamp Disable

| Select | Result |
|--------|-------------------------|
| 0 | Internal clamp enabled |
| 1 | Internal clamp disabled |

The power-up default is 0.

0x1B 2-1 Programmable Bandwidth

Table 33. Bandwidth

| Select | Result |
|--------|----------------|
| x0 | Low bandwidth |
| x1 | High bandwidth |

The power-up default is 1.

0x1B 0 Hold Auto Offset

Table 34. Auto Offset Hold

| Select | Result |
|--------|------------------------------|
| 0 | Normal auto offset operation |
| 1 | Hold current offset value |

The power-up default is 0.

0x1C 7 Auto Offset Enable

0 = manual offset
1 = auto offset using offset as target code. The power-up default is 0.

0x1C 6-5 Auto Offset Update Mode

00 = every clamp
01 = every 16 clamps
10 = every 64 clamps
11 = every Vsync
The power-up default setting is 10.

0x1C 4-3 Difference Shift Amount

00 = 100% of difference used to calculate new offset
01 = 50%
10 = 25%
11 = 12.5%
The power-up default is 01.

0x1C 2 Auto Jump Enable

0 = normal operation
1 = if the code >15 codes off, the offset is jumped to the predicted offset necessary to fix the >15 code mismatch. The power-up default is 1.

0x1C 1 Post Filter Enable

The post filter reduces the update rate by 1/6 and requires that all six updates recommend a change before changing the offset. This prevents unwanted offset changes.

0 = disable post filter
1 = enable post filter
The power-up default is 1.

0x1C 0 Toggle Filter Enable

The toggle filter looks for the offset to toggle back and forth and holds it if triggered. This is to prevent toggling in case of missing codes in the PGA.
1 = toggle filter on, 0 = toggle filter off.

The power-up default is 0.

0x1D 7-0 Slew Limit

Limits the amount the offset can change by in a single update. The power-up default is 0x08.

0x1E 7-0 Sync Filter Lock Threshold

This 8-bit register is programmed to set the number of valid Hsyncs needed to lock the sync filter. This ensures that a consistent, stable Hsync is present before attempting to filter. The power-up default setting is 32d.

0x1F 7-0 Sync Filter Unlock Threshold

This 8-bit register is programmed to set the number of missing or invalid Hsyncs needed to unlock the sync filter. This disables the filter operation when there is no longer a stable Hsync signal. The power-up default setting is 50d.

0x20 7-0 Sync Filter Window Width

This 8-bit register sets the distance in 40 MHz clock periods (25 ns), which is the allowed distance for Hsync pulses before and after the expected Hsync edge. This is the heart of the filter in that it only looks for Hsync pulses at a given time (plus or minus this window) and then ignores extraneous equalization pulses that disrupt accurate PLL operation. The power-up default setting is 10d, or 200 ns on either side of the expected Hsync.

0x21 7 Sync Processing Filter Enable

This bit selects which Hsync is used for the sync processing functions of internal Coast, H/V count, field detection, and Vsync duration counts. A clean Hsync is fundamental to accurate processing of the sync. The power-up default setting is 1.

Table 35. Sync Processing Filter Enable

| Select | Result |
|--------|---|
| 0 | Sync processing uses raw Hsync or SOG |
| 1 | Sync processing uses regenerated Hsync from sync filter |

0x21 6 PLL Sync Filter Enable

This bit selects which signal the PLL uses. It can select between raw Hsync or SOG, or filtered versions. The filtering of the Hsync and SOG can eliminate nearly all extraneous transitions which have traditionally caused PLL disruption. The power-up default setting is 0.

Table 36. PLL Sync Filter Enable

| Select | Result |
|--------|---------------------------------------|
| 0 | PLL uses raw Hsync or SOG inputs |
| 1 | PLL uses filtered Hsync or SOG inputs |

0x21 5 Vsync Filter Enable

The purpose of the Vsync filter is to guarantee the position of the Vsync edge with respect to the Hsync edge and to generate a field signal. The filter works by examining the placement of Vsync and regenerating a correctly placed Vsync one line later. The Vsync is first checked to see whether it occurs in the Field 0 position or the Field 1 position. This is done by checking the leading edge position against the sync separator threshold and the Hsync position. The Hsync width is divided into four quadrants with Quadrant 1 starting at the Hsync leading edge plus a sync separator threshold. If the Vsync leading edge occurs in Quadrant 1 or 4 then the field is set to 0 and the output Vsync is placed coincident with the Hsync leading edge. If the Vsync leading edge occurs in Quadrant 2 or 3 then the field is set to 1 and the output Vsync leading edge is placed in the center of the line. In this way, the Vsync filter creates a

predictable relative position between Hsync and Vsync edges at the output.

If the Vsync occurs near the Hsync edge, this guarantees that the Vsync edge follows the Hsync edge. This performs filtering also in that it requires a minimum of 64 lines between Vsyncs. The Vsync filter cleans up extraneous pulses that might occur on the Vsync. This should be enabled whenever the Hsync/Vsync count is used. Setting this bit to 0 disables the Vsync filter. Setting this bit to 1 enables the Vsync filter. Power-up default is 0.

Table 37. Vsync Filter Enable

| Vsync Filter Bit | Result |
|------------------|-----------------------|
| 0 | Vsync filter disabled |
| 1 | Vsync filter enabled |

0x21 4 Vsync Duration Enable

This enables the Vsync duration block which is designed to be used with the Vsync filter. Setting the bit to 0 leaves the Vsync output duration unchanged; setting the bit to 1 sets the Vsync output duration based on Register 0x22. The power-up default is 0.

Table 38. Vsync Duration Enable

| Vsync Duration Bit | Result |
|--------------------|-----------------------------------|
| 0 | Vsync output duration unchanged |
| 1 | Vsync output duration set by 0x22 |

0x21 3 Auto Offset Clamp Mode

This bit specifies if the auto offset measurement takes place during clamp or either 10 or 16 clocks afterward. The measurement takes 6 clock cycles.

Table 39. AO Clamp Mode

| AO Offset Mode | Result |
|----------------|---|
| 0 | Auto offset measurement takes place during clamp period |
| 1 | Auto offset measurement is set by 0x21, Bit 2 |

0x21 2 Auto Offset Clamp Length

This bit sets the delay following the end of the clamp period for AO measurement. This bit is valid only if Register 0x21, Bit 3 = 1.

Table 40. AO Clamp Length

| AO Offset Clamp Bit | Result |
|---------------------|--------------------------|
| 0 | Delay is 10 clock cycles |
| 1 | Delay is 16 clock cycles |

0x22 7-0 Vsync Duration

This is used to set the output duration of the Vsync, and is designed to be used with the Vsync filter. This is valid only if Register 0x21, Bit 4 is set to 1. Power-up default is 4.

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0x23 7-0 Hsync Duration

An 8 bit register that sets the duration of the Hsync output pulse. The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9880 then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the Hsync output, which is also phase-adjusted. The power-up default is 32.

0x24 7 Hsync Output Polarity

This bit sets the polarity of the Hsync output. Setting this bit to 0 sets the Hsync output to active low. Setting this bit to 1 sets the Hsync output to active high. Power-up default setting is 1.

Table 41. Hsync Output Polarity Settings

| Hsync Output Polarity Bit | Result |
|---------------------------|--------------------------------|
| 0 | Hsync output polarity negative |
| 1 | Hsync output polarity positive |

0x24 6 Vsync Output Polarity

This bit sets the polarity of the Vsync output (both DVI and analog). Setting this bit to 0 sets the Vsync output to active low. Setting this bit to 1 sets the Vsync output to active high. Power-up default is 1.

Table 42. Vsync Output Polarity Settings

| Vsync Output Polarity Bit | Result |
|---------------------------|-----------------------------------|
| 0 | Vsync output polarity is negative |
| 1 | Vsync output polarity is positive |

0x24 5 Display Enable Output Polarity

This bit sets the polarity of the display enable (DE) for both DVI and analog.

Table 43. DE Output Polarity Settings

| DE Output Polarity Bit | Result |
|------------------------|--------------------------------|
| 0 | DE output polarity is negative |
| 1 | DE output polarity is positive |

The power-up default is 1.

0x24 4 Field Output Polarity

This bit sets the polarity of the field output signal on Pin 21. The power-up default setting is 1.

Table 44. Field Output Polarity

| Select | Result |
|--------|--|
| 0 | Active low = even field; active high = odd field |
| 1 | Active low = odd field; active high = even field |

Output field polarity (both DVI and analog)

0 = active low out

1 = active high out

The power-up default is 1.

0x24 3 SOG Output Polarity

This bit sets the polarity of the SOGOUT signal (analog only).

Table 45. SOGOUT Polarity Settings

| SOGOUT | Result |
|--------|-------------|
| 0 | Active low |
| 1 | Active high |

The power-up default setting is 1.

0x24 2-1 SOG Output Select

These register bits control the output on the SOGOUT pin. Options are the raw SOG from the slicer (this is the unprocessed SOG signal produced from the sync slicer), the raw Hsync, the regenerated sync from the sync filter, which can generate missing syncs because of coasting or drop-out, or the filtered sync that excludes extraneous syncs not occurring within the sync filter window.

Table 46. SOGOUT Polarity Settings

| SOGOUT Select | Function |
|---------------|---|
| 00 | Raw SOG from sync slicer (SOG0 or SOG1) |
| 01 | Raw Hsync (Hsync0 or Hsync1) |
| 10 | Regenerated sync from sync filter |
| 11 | Hsync to PLL |

The power-up default setting is 11.

0x24 0 Output Clock Invert

This bit allows inversion of the output clock as specified by Register 0x25, Bits 7 to 6. The power-up default setting is 0.

Table 47. Output Clock Invert

| Select | Result |
|--------|-------------------|
| 0 | Noninverted clock |
| 1 | Inverted clock |

0x25 7-6 Output Clock Select

These bits select the clock output on the DATACLK pin. They include 1/2× clock, a 2× clock, a 90° phase shifted clock or the normal pixel clock. The power-up default setting is 01.

Table 48. Output Clock Select

| Select | Result |
|--------|--------------------------|
| 00 | ½× pixel clock |
| 01 | 1× pixel clock |
| 10 | 2× pixel clock |
| 11 | 90° phase 1× pixel clock |

0x25 5-4 Output Drive Strength

These two bits select the drive strength for all the high-speed digital outputs (except VSOUT, A0 and O/E field). Higher drive strength results in faster rise/fall times and in general makes it easier to capture data. Lower drive strength results in slower rise/fall times and helps to reduce EMI and digitally generated power supply noise. The power-up default setting is 11.

Table 49. Output Drive Strength

| Output Drive | Result |
|--------------|-----------------------------------|
| 00 | Low output drive strength |
| 01 | Medium low output drive strength |
| 10 | Medium high output drive strength |
| 11 | High output drive strength |

0x25 3-2 Output Mode

These bits choose between four options for the output mode, one of which is exclusive to an HDMI input. 4:4:4 mode is standard RGB; 4:2:2 mode is YCrCb, which reduces the number of active output pins from 24 to 16; 4:4:4 double data rate (DDR) output mode; and the data is RGB mode, but changes on every clock edge. The power-up default setting is 00.

Table 50. Output Mode

| Output Mode | Result |
|-------------|---|
| 00 | 4:4:4 RGB mode |
| 01 | 4:2:2 YCrCb mode + DDR 4:2:2 on blue (secondary) |
| 10 | DDR 4:4:4: DDR mode + DDR 4:2:2 on blue (secondary) |
| 11 | 12-bit 4:2:2 (HDMI option only) |

The power-up default is 00.

0x25 1 Primary Output Enable

This bit places the primary output in active or high impedance mode.

The primary output is designated when using either 4:2:2 or DDR 4:4:4. In these modes, the data on the red and green output channels is the primary output, while the output data on the blue channel (DDR YCrCb) is the secondary output. The power-up default setting is 1.

Table 51. Primary Output Enable

| Select | Result |
|--------|--|
| 0 | Primary output is in high impedance mode |
| 1 | Primary output is enabled |

0x25 0 Secondary Output Enable

This bit places the secondary output in active or high impedance mode.

The secondary output is designated when using either 4:2:2 or DDR 4:4:4. In these modes the data on the blue output channel is the secondary output while the output data on the red and green channels is the primary output. Secondary output is always a DDR YCrCb data mode. The power-up default setting is 0.

Table 52. Secondary Output Enable

| Select | Result |
|--------|--|
| 0 | Secondary output is in high impedance mode |
| 1 | Secondary output is enabled |

0x26 7 Output Three-State

When enabled, this bit puts all outputs (except SOGOUT) in a high impedance state. The power-up default setting is 0.

Table 53. Output Three-State

| Select | Result |
|--------|--|
| 0 | Normal outputs |
| 1 | All outputs (except SOGOUT) in high impedance mode |

0x26 6 SOG Three-State

When enabled, this bit allows the SOGOUT pin to be placed in a high impedance state. The power-up default setting is 0.

Table 54. SOGout Three-State

| Select | Result |
|--------|--------------------------------------|
| 0 | Normal SOG output |
| 1 | SOGOUT pin is in high impedance mode |

0x26 5 SPDIF Three-State

When enabled, this bit places the SPDIF audio output pins in a high impedance state. The power-up default setting is 0.

Table 55. SOGOUT Three-State

| Select | Result |
|--------|-----------------------------------|
| 0 | Normal SPDIF output |
| 1 | SPDIF pins in high impedance mode |

0x26 4 I2S Three-State

When enabled, this bit places the I2S output pins in a high impedance state. The power-up default setting is 0.

Table 56. SOGOUT Three-State

| Select | Result |
|--------|----------------------------------|
| 0 | Normal I2S output |
| 1 | I2S pins in high impedance mode. |

0x26 3 Power-Down Polarity

This bit defines the polarity of the input power-down pin. The power-up default setting is 1.

Table 57. Power-Down Input Polarity

| Select | Result |
|--------|-------------------------------|
| 0 | Power-down pin is active low |
| 1 | Power-down pin is active high |

0x26 2-1 Power-Down Pin Function

These bits define the different operational modes of the power-down pin. These bits are functional only when the power-down pin is active; when it is not active, the part is powered up and functioning. The power-up default setting is 00.

Table 58. Power Down Pin Function

| PWRDN Pin Function | Result |
|--------------------|--|
| 00 | The chip is powered down and all outputs except SOGOUT are in high impedance mode. |
| 01 | The chip is powered down and all outputs are in high impedance mode. |
| 10 | The chip remains powered up, but all outputs except SOGOUT are in high impedance mode. |
| 11 | The chip remains powered up, but all outputs are in high impedance mode. |

0x26 0 Power-Down

This bit is used to put the chip in power-down mode. In this mode the chips power dissipation is reduced to a fraction of the typical power (see Table 1 for exact power dissipation). When in power-down, the HSOUT, VSOUT, DATAACK, and all 30 of the data outputs are put into a high impedance state. Note that the SOGOUT output is not put into high impedance. Circuit blocks that continue to be active during power-down include the voltage references, sync processing, sync detection, and the serial register. These blocks facilitate a fast start-up from power-down. The power-up default setting is 0.

Table 59. Power-Down Settings

| Select | Result |
|--------|------------------|
| 0 | Normal operation |
| 1 | Power-Down |

0x27 7 Auto Power-Down Enable

This bit enables the chip to go into low power mode, or seek mode if no sync inputs are detected. The power-up default setting is 1.

Table 60. Auto Power-Down Select

| Auto Power Down | Result |
|-----------------|--|
| 0 | Auto power down disabled |
| 1 | Chip powers down if no sync inputs present |

0x27 6 HDCP A0 Address

This bit sets the LSB of the address of the HDCP I²C. This should be set to 1 only for a second receiver in a dual-link configuration. The power-up default is 0.

0x27 5 MCLK External Enable

This bit enables the MCLK to be supplied externally. If an external MCLK is used, then it must be locked to the video clock according to the CTS and N available in the I²C. Any mismatch between the internal MCLK and the input MCLK results in dropped or repeated audio samples. The power-up default setting is 0.

Table 61. MCLK External Select

| Select | Result |
|--------|-------------------------------|
| 0 | Use internally generated MCLK |
| 1 | Use external MCLK input |

BT656 GENERATION

0x27 4 BT656 Enable

This bit enables the output to be BT656-compatible with defined start of active video (SAV) and end of active video (EAV) controls to be inserted. These require specification of the number of active lines, active pixels per line, and delays to place these markers. The power-up default setting is 0.

Table 62. BT656 Mode

| Select | Result |
|--------|--------------------------|
| 0 | Disable BT656 video mode |
| 1 | Enable BT656 video mode |

0x27 3 Force DE Generation

This bit allows the use of the internal DE generator in DVI mode. The power-up default setting is 0.

Table 63. DE Generation

| Select | Result |
|--------|--|
| 0 | Internal DE generation disabled |
| 1 | Force DE generation via programmed registers |

0x27 2-0 Interlace Offset

These bits define the offset in Hsyncs from Field 0 to Field 1. The power-up default setting is 000.

0x28 7-2 Vsync Delay

These bits set the delay (in lines) from the leading edge of Vsync to active video. The power-up default setting is 24.

0x28 1-0 Hsync Delay MSBs

Along with the eight bits following these ten bits set the delay (in pixels) from the Hsync leading edge to the start of active video. The power-up default setting is 0x104.

0x29 7-0 Hsync Delay LSBs

See the Hsync Delay MSBs section.

0x2A 3-0 Line Width MSBs

Along with the 8 bits following these 12 bits, set the width of the active video line (in pixels). The power-up default setting is 0x500.

0x2B 7-0 Line Width LSBs

See the line width MSBs section.

0x2C 3-0 Screen Height MSBs

Along with the 8 bits following these 12 bits, set the height of the active screen (in lines). The power-up default setting is 0x2D0.

0x2D 7-0 Screen Height LSBs

See the Screen Height MSBs section.

0x2E 7 Ctrl Enable

When set, this bit allows Ctrl [3:0] signals decoded from the DVI to be output on the I2S data pins. The power-up default setting is 0.

Table 64. CTRL Enable.

| Select | Result |
|--------|--------------------------------|
| 0 | I2S signals on I2S lines |
| 1 | Ctrl [3:0] output on I2S lines |

0x2E 6-5 I2S Output Mode

These bits select between four options for the I2S output: I2S, right-justified, left-justified, or raw IEC60958 mode. The power-up default setting is 00.

Table 65. I2S Output Select

| I2S Output Mode | Result |
|-----------------|-------------------|
| 00 | I2S mode |
| 01 | Right-Justified |
| 10 | Left-Justified |
| 11 | Raw IEC60958 mode |

0x2E 4-0 I2S Bit Width

These bits set the I2S bit width for right-justified mode. The power-up default setting is 24 bits.

0x2F 6 TMDS Sync Detect

This read-only bit indicates the presence of a TMDS DE.

Table 66. Detected TMDS Sync Results

| Detect | Result |
|--------|--------------------|
| 0 | No TMDS DE present |
| 1 | TMDS DE detected |

0x2F 5 TMDS Active

This read only bit indicates the presence of a TMDS clock.

Table 67. Detected TMDS Clock Results

| Detect | Result |
|--------|-----------------------|
| 0 | No TMDS clock present |
| 1 | TMDS clock detected |

0x2F 4 AV Mute

This read-only bit indicates the presence of AV (audio video) mute based on general control packets.

Table 68. Detected AV Mute Status

| Detect | Result |
|--------|--------------|
| 0 | AV not muted |
| 1 | AV muted |

0x2F 3 HDCP Keys Read

This read-only bit reports if the HDCP keys were read successfully.

Table 69. HDCP Keys

| Detect | Result |
|--------|---------------------------|
| 0 | Failure to read HDCP keys |
| 1 | HDCP keys read |

0x2F 2-0 HDMI Quality

These read-only bits indicate a level of HDMI quality based on the DE (display enable) edges. A larger number indicates a higher quality.

0x30 6 HDMI Content Encrypted

This read-only bit is high when HDCP decryption is in use (content is protected). The signal goes low when HDCP is not being used. Customers can use this bit to determine whether or not to allow copying of the content. The bit should be sampled at regular intervals since it can change on a frame by frame basis.

Table 70. HDCP Activity

| Detect | Result |
|--------|------------------------|
| 0 | HDCP not in use |
| 1 | HDCP decryption in use |

0x30 5 DVI Hsync Polarity

This read-only bit indicates the polarity of the DVI Hsync.

Table 71. DVI Hsync Polarity Detect

| Detect | Result |
|--------|-----------------------------------|
| 0 | DVI Hsync polarity is low active |
| 1 | DVI Hsync polarity is high active |

0x30 4 DVI Vsync Polarity

This read-only bit indicates the polarity of the DVI Vsync.

Table 72. DVI Vsync Polarity Detect

| Detect | Result |
|--------|-----------------------------------|
| 0 | DVI Vsync polarity is low active |
| 1 | DVI Vsync polarity is high active |

0x30 3-0 HDMI Pixel Repetition

These read-only bits indicate the pixel repetition on DVI. 0 = 1x, 1 = 2x, 2 = 3x, up to a maximum repetition of 10x (0x9).

Table 73.

| Select | Repetition Multiplier |
|--------|-----------------------|
| 0000 | 1x |
| 0001 | 2x |
| 0010 | 3x |
| 0011 | 4x |
| 0100 | 5x |
| 0101 | 6x |
| 0110 | 7x |
| 0111 | 8x |
| 1000 | 9x |
| 1001 | 10x |

MACROVISION

0x31 7-4 Macrovision Pulse Max

These bits set the pseudo sync pulse width maximum for Macrovision detection in pixel clocks. This is functional for 13.5 MHz SDTV or 27 MHz progressive scan. Power up default is 9.

0x31 3-0 Macrovision Pulse Min

These bits set the pseudo sync pulse width minimum for Macrovision detection in pixel clocks. This is functional for 13.5 MHz SDTV or 27 MHz progressive scan. Power up default is 6.

0x32 7 Macrovision Oversample Enable

Tells the Macrovision detection engine whether we are oversampling or not. This accommodates 27 MHz sampling for SDTV and 54 MHz sampling for progressive scan and is used as a correction factor for clock counts. Power up default is 0.

0x32 6 Macrovision PAL Enable

Tells the Macrovision detection engine to enter PAL mode when set to 1. Default is 0 for NTSC mode.

0x32 5-0 Macrovision Line Count Start

Sets the start line for Macrovision detection. Along with Register 0x33, Bits [5:0] they define the region where MV pulses are expected to occur. The power-up default is Line 13.

0x33 7 Macrovision Detect Mode

0 = standard definition
1 = progressive scan mode

0x33 6 Macrovision Settings Override

This defines whether preset values are used for the MV line counts and pulse widths or the values stored in I²C registers.

0 = use hard coded settings for line counts and pulse widths
1 = use I²C values for these settings

0x33 5-0 Macrovision Line Count End

Sets the end line for Macrovision detection. Along with Register 0x32, Bits [5:0] they define the region where MV pulses are expected to occur. The power up default is Line 21.

0x34 7-6 Macrovision Pulse Limit Select

Sets the number of pulses required in the last three lines (SD mode only). If there is not at least this number of MV pulses, the engine stops. These two bits define the following pulse counts:

00 = 6
01 = 4
10 = 5 (default)
11 = 7

0x34 5 Low Frequency Mode

Sets whether the audio PLL is in low frequency mode or not. Low frequency mode should only be set for pixel clocks < 80 MHz.

0x34 4 Low Frequency Override

Allows the previous bit to be used to set low frequency mode rather than the internal autodetect.

0x34 3 Up Conversion Mode

0 = repeat Cb/Cr values
1 = interpolate Cb/Cr values

0x34 2 CbCr Filter Enable

Enables the FIR filter for 4:2:2 CbCr output.

COLOR SPACE CONVERSION

The default power up values for the color space converter coefficients (R0x35 through R0x4C) are set for ATSC RGB to YCbCr conversion. They are completely programmable for other conversions.

0x34 1 Color space Converter Enable

This bit enables the color space converter. The power-up default setting is 0.

Table 74. Color space Converter

| Select | Result |
|--------|-------------------------------|
| 0 | Disable color space converter |
| 1 | Enable color space converter |

0x35 6-5 Color space Converter Mode

These two bits set the fixed point position of the CSC coefficients, including the A4, B4, and C4 offsets.

Table 75. CSC Fixed Point Converter Mode

| Select | Result |
|--------|------------------------------|
| 00 | $\pm 1.0, -4096$ to 4095 |
| 01 | $\pm 2.0, -8192$ to 8190 |
| 1x | $\pm 4.0, -16384$ to 16380 |

0x35 4-0 Color space Conversion Coefficient A1 MSBs

These 5 bits form the 5 MSBs of the Color space Conversion Coefficient A1. This combined with the 8 LSBs of the following register form a 13-bit twos complement coefficient which is user programmable. The equation takes the form of:

$$R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$$

$$G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$$

$$B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$$

The default value for the 13 bit A1 coefficient is 0x0C52.

0x36 7-0 Color space Conversion Coefficient A1 LSBs

See the Register 0x35 section.

0x37 4-0 CSC A2 MSBs

These five bits form the 5 MSBs of the Color space Conversion Coefficient A2. Combined with the 8 LSBs of the following register they form a 13 bit twos complement coefficient that is user programmable. The equation takes the form of:

$$R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$$

$$G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$$

$$B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$$

The default value for the 13-bit A2 coefficient is 0x0800.

0x38 7-0 CSC A2 LSBs

See the Register 0x37 section.

0x39 4-0 CSC A3 MSBs

The default value for the 13-bit A3 is 0x0000.

0x3A 7-0 CSC A3 LSBs

0x3B 4-0 CSC A4 MSBs

The default value for the 13-bit A4 is 0x19D7.

0x3C 7-0 CSC A4 LSBs

0x3D 4-0 CSC B1 MSBs

The default value for the 13-bit B1 is 0x1C54.

0x3E 7-0 CSC B1 LSBs

0x3F 4-0 CSC B2 MSB

The default value for the 13-bit B2 is 0x0800.

0x40 7-0 CSC B2 LSBs

0x41 4-0 CSC B3 MSBs

The default value for the 13-bit B3 is 0x1E89.

0x42 7-0 CSC B3 LSBs

0x43 4-0 CSC B4 MSBs

The default value for the 13-bit B4 is 0x0291.

0x44 7-0 CSC B4 LSBs

0x45 4-0 CSC C1 MSBs

The default value for the 13-bit C1 is 0x0000.

0x46 7-0 CSC C1 LSBs

0x47 4-0 CSC C2 MSBs

The default value for the 13 bit C2 is 0x0800.

0x48 7-0 CSC C2 LSBs

0x49 4-0 CSC C3 MSBs

The default value for the 13-bit C3 is 0x0E87.

0x4A 7-0 CSC C3 LSBs

0x4B 4-0 CSC C4 MSBs

The default value for the 13-bit C4 is 0x18BD.

0x4C 7-0 CSC C4 LSBs

0x57 7 A/V Mute Override

0x57 6 A/V Mute Value

0x57 3 Disable AV Mute

0x57 2 Disable Audio Mute

0x58 7 MCLK PLL Enable

This bit enables the use of the analog PLL.

0x58 6-4 MCLK PLL_N

These bits control the division of the MCLK out of the PLL.

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Table 76.

| PLL_N [2:0] | MCLK Divide Value |
|-------------|-------------------|
| 0 | /1 |
| 1 | /2 |
| 2 | /3 |
| 3 | /4 |
| 4 | /5 |
| 5 | /6 |
| 6 | /7 |
| 7 | /8 |

0x58 3 N_CTS_Disable

This bit makes it possible to prevent the N/CTS packet on the link from writing to the N and CTS registers.

0x58 2-0 MCLK fs_N

These bits control the multiple of 128 fs used for MCLK out.

Table 77.

| MCLK fs_N [2:0] | fs Multiple |
|-----------------|-------------|
| 0 | 128 |
| 1 | 256 |
| 2 | 384 |
| 3 | 512 |
| 4 | 640 |
| 5 | 768 |
| 6 | 896 |
| 7 | 1024 |

0x59 6 MDA/MCL PU Disable

This bit disables the inter MDA/MCL pull-ups.

0x59 5 CLK Term O/R

This bit allows for overriding during power down. 0 = auto, 1 = manual.

0x59 4 Manual CLK Term

This bit allows normal clock termination or disconnects this. 0 = normal, 1 = disconnected.

0x59 2 FIFO Reset UF

This bit resets the audio FIFO if underflow is detected.

0x59 1 FIFO Reset OF

This bit resets the audio FIFO if overflow is detected.

0x59 0 MDA/MCL Three-State

This bit three-states the MDA/MCL lines to allow in-circuit programming of the EEPROM.

0x5A 6-0 Packet Detect

This register indicates if a data packet in specific sections has been detected. These seven bits are updated if any specific packet has been received since last reset or loss of clock detect. Normal is 0x00.

Table 78.

| Packet Detect Bit | Packet Detected |
|-------------------|-----------------------|
| 0 | AVI infoframe |
| 1 | Audio infoframe |
| 2 | SPD infoframe |
| 3 | MPEG Source infoframe |
| 4 | ACP packets |
| 5 | ISRC1 packets |
| 6 | ISRC2 packets |

0x5B 3 HDMI Mode

0 = DVI, 1 = HDMI.

0x5E 7-6 Channel Status Mode

0x5E 5-3 PCM Audio Data

0x5E 2 Copyright Information

0x5E 1 Linear PCM Identification

0x5E 0 Use of Channel Status Block

0x5F 7-0 Channel Status Category Code

0x60 7-4 Channel Number

0x60 3-0 Source Number

0x61 5-4 Clock Accuracy

0x61 3-0 Sampling Frequency

Table 79.

| Code | Frequency (kHz) |
|------|-----------------|
| 0x0 | 44.1 |
| 0x2 | 48 |
| 0x3 | 32 |
| 0x8 | 88.2 |
| 0xA | 96 |
| 0xC | 176.4 |
| 0xE | 192 |

0x62 3-0 Word Length

0x7B 7-0 CTS (Cycle Time Stamp) (19-12)

These are the most significant 8 bits of a 20-bit word used in the 20-bit N term in the regeneration of the audio clock.

0x7C 7-0 CTS (11-4)

0x7D 7-4 CTS (3-0)

0x7D 3-0 N (19-16)

These are the most significant 4 bits of a 20-bit word used along with the 20-bit CTS term to regenerate the audio clock.

0x80 AVI Infoframe Version

0x81 6-5 Y[1:0]

This register indicates whether data is RGB, 4:4:4 or 4:2:2.

Table 80.

| Y | Video Data |
|----|-------------|
| 00 | RGB |
| 01 | YCbCr 4:2:2 |
| 10 | YCbCr 4:4:4 |

0x81 4 Active Format Information Present

0 = no data
1 = active format information valid

0x81 3-2 Bar Information

Table 81.

| B | Bar Type |
|----|---|
| 00 | No bar information |
| 01 | Horizontal bar information valid |
| 10 | Vertical bar information valid |
| 11 | Horizontal and vertical bar information valid |

0x81 1-0 Scan Information

Table 82.

| S [1:0] | Scan Type |
|---------|--------------------------|
| 00 | No information |
| 01 | Overscanned (television) |
| 10 | Underscanned (computer) |

0x82 7-6 Colorimetry

Table 83.

| C [1:0] | Colorimetry |
|---------|--------------------|
| 00 | No data |
| 01 | SMPTE 170M, ITU601 |
| 10 | ITU 709 |

0x82 5-4 Picture Aspect Ratio

Table 84.

| M [1:0] | Aspect Ratio |
|---------|--------------|
| 00 | No data |
| 01 | 4:3 |
| 10 | 16:9 |

0x82 3-0 Active Format Aspect Ratio

Table 85.

| R [3:0] | Active Format A/R |
|---------|--|
| 0x8 | Same as picture aspect ratio (M [1:0]) |
| 0x9 | 4:3 (center) |
| 0xA | 16:9 (center) |
| 0xB | 14:9 (center) |

0x83 1-0 Nonuniform Picture Scaling

Table 86.

| SC [1:0] | Picture Scaling |
|----------|--|
| 00 | No known nonuniform scaling |
| 01 | Has been scaled horizontally |
| 10 | Has been scaled vertically |
| 11 | Has been scaled both horizontally and vertically |

0x84 6-0 Video ID Code

See CEA EDID short video descriptors.

0x85 3-0 Pixel Repeat

This value indicates how many times the pixel was repeated. 0x0 = no repeats, sent once, 0x8 = 8 repeats, sent 9 times, and so on.

0x86 7-0 Active Line Start LSB

Combined with the MSB in Register 0x88, these bits indicate the beginning line of active video. All lines before this comprise a top horizontal bar. This is used in letter box modes. If the 2-byte value is 0x00, there is no horizontal bar.

0x87 6-0 New Data Flags (NDF)

This register indicates whether data in specific sections has changed. In the address space from 0x80 to 0xFF, each register address ending in 0b111 (for example, 0x87, 0x8F, 0x97, 0xAF) is an NDF register. They all have the same data and all are reset upon reading any one of them.

Table 87.

| NDF Bit number | Changes Occurred |
|----------------|-----------------------|
| 0 | AVI infoframe |
| 1 | Audio infoframe |
| 2 | SPD infoframe |
| 3 | MPEG Source infoframe |
| 4 | ACP packets |
| 5 | ISRC1 packets |
| 6 | ISRC2 packets |

0x88 7-0 Active Line Start MSB

See Register 0x86.

0x89 7-0 Active Line End LSB

Combined with the MSB in Register 0x8A these bits indicate the last line of active video. All lines past this comprise a lower horizontal bar. This is used in letter-box modes. If the 2-byte value is greater than the number of lines in the display, there is no lower horizontal bar.

0x8A 7-0 Active Line End MSB

See Register 0x89.

0x8B 7-0 Active Pixel Start LSB

Combined with the MSB in Register 0x8C, these bits indicate the first pixel in the display which is active video. All pixels before this comprise a left vertical bar. If the 2-byte value is 0x00, there is no left bar.

0x8C 7-0 Active Pixel Start MSB

See Register 0x8B.

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0x8D 7-0 Active Pixel End LSB

Combined with the MSB in Register 0x8E these bits indicate the last active video pixel in the display. All pixels past this comprise a right vertical bar. If the 2-byte value is greater than the number of pixels in the display, there is no vertical bar.

0x8E 7-0 Active Pixel End MSB

See Register 0x8D.

0x8F 6-0 NDF

See Register 0x87.

0x90 7-0 Audio Infoframe Version

0x91 7-4 Audio Coding Type

These bits identify the audio coding so that the receiver may process audio properly.

Table 88.

| CT [3:0] | Audio Coding |
|-----------------|------------------------|
| 0x0 | Refer to stream header |
| 0x1 | IEC60958 PCM |
| 0x2 | AC-3 |
| 0x3 | MPEG1 (Layers 1 and 2) |
| 0x4 | MP3 (MPEG1 Layer 3) |
| 0x5 | MPEG2 (multichannel) |
| 0x6 | AAC |
| 0x7 | DTS |
| 0x8 | ATRAC |

0x91 2-0 Audio Channel Count

These bits specify how many audio channels are being sent—2 channels to 8 channels.

Table 89.

| CC [2:0] | Channel Count |
|-----------------|------------------------|
| 000 | Refer to stream header |
| 001 | 2 |
| 010 | 3 |
| 011 | 4 |
| 100 | 5 |
| 101 | 6 |
| 110 | 7 |
| 111 | 8 |

0x92 4-2 Sampling Frequency

0x92 1-0 Ample Size

0x93 7-0 Max Bit Rate

For compressed audio only when this value is multiplied by 8 kHz represents the maximum bit rate. A value of 0x08 in this field would yield a maximum bit rate of (8 kHz × 8 kHz = 64 kHz).

0x94 7-0 Speaker Mapping

These bits define the mapping (suggested placement) of speakers.

Table 90.

| Abbreviation | Speaker Placement |
|---------------------|--------------------------|
| FL | Front left |
| FC | Front center |
| FR | Front right |
| FCL | Front center left |
| FCR | Front center right |
| RL | Rear left |
| RC | Rear center |
| RR | Rear right |
| RCL | Rear center left |
| RCR | Rear center right |
| LFE | Low frequency effect |

Table 91.

| CA | | | | | Channel Number | | | | | | | | |
|-------|-------|-------|-------|-------|----------------|-------|-------|-------|-------|-------|-------|-------|----|
| Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | |
| 0 | 0 | 0 | 0 | 0 | | | | | | - | - | FR | FL |
| 0 | 0 | 0 | 0 | 1 | | | | | | - | LFE | FR | FL |
| 0 | 0 | 0 | 1 | 0 | | | | | | FC | - | FR | FL |
| 0 | 0 | 0 | 1 | 1 | | | | | | FC | LFE | FR | FL |
| 0 | 0 | 1 | 0 | 0 | | | | RC | | - | - | FR | FL |
| 0 | 0 | 1 | 0 | 1 | | | | RC | | - | LFE | FR | FL |
| 0 | 0 | 1 | 1 | 0 | | | | RC | FC | | - | FR | FL |
| 0 | 0 | 1 | 1 | 1 | | | | RC | FC | LFE | | FR | FL |
| 0 | 1 | 0 | 0 | 0 | | | RR | RL | | - | - | FR | FL |
| 0 | 1 | 0 | 0 | 1 | | | | RR | RL | | LFE | FR | FL |
| 0 | 1 | 0 | 1 | 0 | | | | RR | RL | FC | | FR | FL |
| 0 | 1 | 0 | 1 | 1 | - | - | | RR | RL | FC | LFE | FR | FL |
| 0 | 1 | 1 | 0 | 0 | - | RC | | RR | RL | | - | FR | FL |
| 0 | 1 | 1 | 0 | 1 | - | RC | | RR | RL | | LFE | FR | FL |
| 0 | 1 | 1 | 1 | 0 | - | RC | | RR | RL | FC | | FR | FL |
| 0 | 1 | 1 | 1 | 1 | - | RC | | RR | RL | FC | LFE | FR | FL |
| 1 | 0 | 0 | 0 | 0 | RRC | RLC | | RR | RL | | - | FR | FL |
| 1 | 0 | 0 | 0 | 1 | RRC | RLC | | RR | RL | | LFE | FR | FL |
| 1 | 0 | 0 | 1 | 0 | RRC | RLC | | RR | RL | FC | | FR | FL |
| 1 | 0 | 0 | 1 | 1 | RRC | RLC | | RR | RL | FC | LFE | FR | FL |
| 1 | 0 | 1 | 0 | 0 | FRC | FLC | | - | - | | v | FR | FL |
| 1 | 0 | 1 | 0 | 1 | FRC | FLC | | - | - | v | LFE | FR | FL |
| 1 | 0 | 1 | 1 | 0 | FRC | FLC | | - | FC | | - | FR | FL |
| 1 | 0 | 1 | 1 | 1 | FRC | FLC | | - | FC | LFE | | FR | FL |
| 1 | 1 | 0 | 0 | 0 | FRC | FLC | | RC | | - | - | FR | FL |
| 1 | 1 | 0 | 0 | 1 | FRC | FLC | | RC | | - | LFE | FR | FL |
| 1 | 1 | 0 | 1 | 0 | FRC | FLC | | RC | FC | | - | FR | FL |
| 1 | 1 | 0 | 1 | 1 | FRC | FLC | | RC | FC | LFE | | FR | FL |
| 1 | 1 | 1 | 0 | 0 | FRC | FLC | | RR | RL | | v | FR | FL |
| 1 | 1 | 1 | 0 | 1 | FRC | FLC | | RR | RL | | LFE | FR | FL |
| 1 | 1 | 1 | 1 | 0 | FRC | FLC | | RR | RL | FC | | FR | FL |
| 1 | 1 | 1 | 1 | 1 | FRC | FLC | | RR | RL | FC | LFE | FR | FL |

0x95 7 Down-Mix Inhibit

0x95 6-3 Level Shift Values

These bits define the amount of attenuation. The value directly corresponds to the amount of attenuation: for example, 0000 = 0 dB, 0001 = 1 dB to 1111 = 15 dB attenuation.

0x96 7-0 Reserved

0x97 6-0 New Data Flags

See Register 0x87 for a description.

0x98 7-0 Source Product Description (SPD) Infoframe Version

0x99 7-0 Vendor Name Character 1 (VN1)

This is the first character in eight that is the name of the company that appears on the product. The data characters are 7-bit ASCII code.

0x9A 7-0 VN2

0x9B 7-0 VN3

0x9C 7-0 VN4

0x9D 7-0 VN5

0x9E 7-0 VN6

0x9F 6-0 New Data Flags

See Register 0x87 for a description.

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0xA0 7-0 VN7

0xA1 7-0 VN8

0xA2 7-0 Product Description Character 1 (PD1)

This is the first character of 16 which contains the model number and a short description of the product. The data characters are 7-bit ASCII code.

0xA3 7-0 PD2

0xA4 7-0 PD3

0xA5 7-0 PD4

0xA6 7-0 PD5

0xA7 6-0 New Data Flags

See Register 0x87 for a description.

0xA8 7-0 PD6

0xA9 7-0 PD7

0xAA 7-0 PD8

0xAB 7-0 PD9

0xAC 7-0 PD10

0xAD 7-0 PD11

0xAE 7-0 PD12

0xAF 6-0 New Data Flags

See Register 0x87 for a description.

0xB0 7-0 PD13

0xB1 7-0 PD14

0xB2 7-0 PD15

0xB3 7-0 PD16

0xB4 7-0 Source Device Information Code

These bytes classify the source device.

Table 92.

| SDI Code | Source |
|----------|-------------|
| 0x00 | Unknown |
| 0x01 | Digital STB |
| 0x02 | DVD |
| 0x03 | D-VHS |
| 0x04 | HDD video |
| 0x05 | DVC |
| 0x06 | DSC |
| 0x07 | Video CD |
| 0x08 | Game |
| 0x09 | PC general |

0xB7 6-0 New Data Flags

See Register 0x87 for a description.

0xB8 7-0 MPEG Source Infoframe Version

0xB9 7-0 MPEG Bit Rate Byte 0 (MB0)

This is the lower 8 bits of 32 bits that specify the MPEG bit rate in Hz.

0xBA 7-0 MB1

0xBB 7-0 MB2

0xBC 7-0 MB3—Upper Byte

0xBD 4 Field Repeat

This defines whether the field is new or repeated.

Table 93.

| FR | Field Type |
|----|----------------------|
| 0 | New field or picture |
| 1 | Repeated field |

0xBD 1-0 MPEG Frame

This identifies the frame as I, B, or P.

Table 94.

| MF [1-0] | Frame Type |
|----------|------------|
| 00 | Unknown |
| 01 | I—picture |
| 10 | B—picture |
| 11 | P—picture |

0xBE 7-0 Reserved

0xBF 6-0 New Data Flags

See Register 0x87 for a description.

0xC0 7-0 Audio Content Protection Packet (ACP Type)

These bits define which audio content protection is used.

Table 95.

| Code | ACP Type |
|-----------|------------------------------------|
| 0x00 | Generic audio |
| 0x01 | IEC 60958-identified audio |
| 0x02 | DVD-audio |
| 0x03 | Reserved for super audio CD (SACD) |
| 0x04—0xFF | Reserved |

0xC1 ACP Packet Byte 0 (ACP_PB0)

0xC2 7-0 ACP_PB1

0xC3 7-0 ACP_PB2

0xC4 7-0 ACP_PB3

0xC5 7-0 ACP_PB4

0xC7 6-0 New Data Flags

See Register 0x87 for a description.

0xC8 7 International Standard Recording Code (ISRC1) Continued

This bit indicates that a continuation of the 16 ISRC1 packet bytes (an ISRC2 packet) is being transmitted.

0xC8 6 ISRC1 Valid

This bit is an indication of the whether ISRC1 packet bytes are valid.

Table 96.

| ISRC1 Valid | Description |
|-------------|-------------------------------------|
| 0 | ISRC1 status bits and PBs not valid |
| 1 | ISRC1 status bits and PBs valid |

0xC8 2-0 ISRC Status

These bits define where in the ISRC track the samples are: at least two transmissions of 001 occur at the beginning of the track, while in the middle of the track, continuous transmission of 010 occurs followed by at least two transmissions of 100 near the end of the track.

0xC9 7-0 ISRC1 Packet Byte 0 (ISRC1_PB0)**0xCA 7-0 ISRC1_PB1****0xCB 7-0 ISRC1_PB2****0xCC 7-0 ISRC1_PB3****0xCD 7-0 ISRC1_PB4****0xCE 7-0 ISRC1_PB5****0xCF 6-0 New Data Flags**

See Register 0x87 for a description.

0xD0 7-0 ISRC1_PB6**0xD1 7-0 ISRC1_PB7****0xD2 7-0 ISRC1_PB8****0xD3 7-0 ISRC1_PB9****0xD4 7-0 ISRC1_PB10****0xD5 7-0 ISRC1_PB11****0xD6 7-0 ISRC1_PB12****0xD7 6-0 New Data Flags**

See Register 0x87 for a description.

0xD8 7-0 ISRC1_PB13**0xD9 7-0 ISRC1_PB14****0xDA 7-0 ISRC1_PB15****0xDB 7-0 ISRC1_PB16****0xDC 7-0 ISRC2 Packet Byte 0 (ISRC2_PB0)**

This is transmitted only when the ISRC continue bit (Register 0xC8 Bit 7) is set to 1.

0xDD 7-0 ISRC2_PB1**0xDE 7-0 ISRC2_PB2****0xDF 6-0 New Data Flags**

See Register 0x87 for a description.

0xE0 7-0 ISRC2_PB3**0xE1 7-0 ISRC2_PB4****0xE2 7-0 ISRC2_PB5****0xE3 7-0 ISRC2_PB6****0xE4 7-0 ISRC2_PB7****0xE5 7-0 ISRC2_PB8****0xE6 7-0 ISRC2_PB9****0xE7 6-0 New Data Flags**

See Register 0x87 for a description.

0xE8 7-0 ISRC2_PB10**0xE9 7-0 ISRC2_PB11****0xEA 7-0 ISRC2_PB12****0xEB 7-0 ISRC2_PB13****0xEC 7-0 ISRC2_PB14****0xED 7-0 ISRC2_PB15****0xEE 7-0 ISRC2_PB16**

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control interface is provided in the AD9880. Up to two AD9880 devices can be connected to the 2-wire serial interface, with a unique address for each device.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal
- Acknowledge (Ack)

When the serial interface is inactive (SCL and SDA are high) communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address (the first seven bits) and a single R/W\ bit (the eighth bit). The R/W\ bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA0 input pin as shown in Table 97), the AD9880 acknowledges by bringing SDA low on the 9th SCL pulse. If the addresses do not match, the AD9880 does not acknowledge.

Table 97. Serial Port Addresses

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 |
|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| A ₆ (MSB) | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9880 does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9880 during a read sequence, the AD9880 interprets this as end of data. The SDA remains high, so the master can generate a stop signal.

Writing data to specific control registers of the AD9880 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value. Any base address higher than the maximum value does not produce an acknowledge signal.

Data are read from the control registers of the AD9880 in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte low to set up a sequential read operation.

Reading (the $\overline{R/W}$ bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9880, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

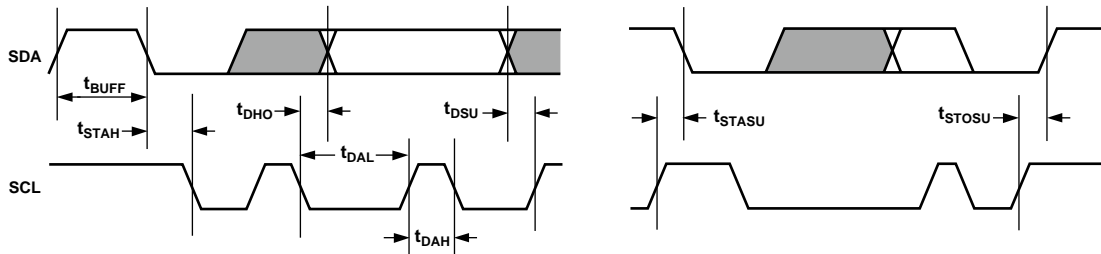


Figure 17. Serial Port Read/Write Timing

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Serial Interface Read/Write Examples

Write to one control register:

- Start signal
- Slave address byte (R/W\ bit = low)
- Base address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers:

- Start signal
- Slave address byte (R/W\ bit = LOW)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one control register:

- Start signal
- Slave address byte (R/W\ bit = low)
- Base address byte
- Start signal
- Slave address byte (R/W\ bit = high)
- Data byte from base address
- Stop signal

Read from four consecutive control registers:

- Start signal
- Slave address byte (R/W\ bit = low)
- Base address byte
- Start signal
- Slave address byte (R/W\ bit = high)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

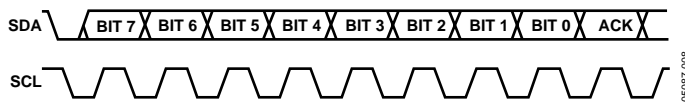


Figure 18. Serial Interface—Typical Byte Transfer

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PCB LAYOUT RECOMMENDATIONS

The AD9880 is a high-precision, high-speed analog device. To achieve the maximum performance from the part, it is important to have a well laid-out board. The following is a guide for designing a board using the AD9880.

Analog Interface Inputs

Using the following layout techniques on the graphics inputs is extremely important:

- Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9880 as close as possible to the graphics VGA connector. Long input trace lengths are undesirable, because they pick up more noise from the board and other external sources.
- Place the 75 Ω termination resistors (see Figure 3) as close to the AD9880 chip as possible. Any additional trace length between the termination resistors and the input of the AD9880 increases the magnitude of reflections, which corrupts the graphics signal.
- Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω also increase the chance of reflections.

The AD9880 has very high input bandwidth (300 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it also captures any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9880, sometimes low-pass filtering the analog inputs can help to reduce noise. For many applications, filtering is unnecessary. Experiments have shown that placing a series ferrite bead prior to the 75 Ω termination resistor is helpful in filtering out excess noise. Specifically, the part used was the Fair-Rite 2508051217Z0, but each application may work best with a different bead value. Alternatively, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor can also be beneficial.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1 μF capacitor. The exception is in the case where two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9880, since that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads down to the power plane is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_{DD} (the clock generator supply). Abrupt changes in PV_{DD} can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_{D} and PV_{DD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during Hsync and Vsync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_{DD} , from a different, cleaner, power source (for example, from a 12 V supply).

It is recommended to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental since each separate ground plane is smaller and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to place a single ground plane under the AD9880. The location of the split should be at the receiver of the digital outputs. In this case it is even more important to place components wisely because the current loops are much longer, (current takes the path of least resistance). An example of a current loop is power plane to AD9880 to digital output trace to digital data receiver to digital ground plane to analog ground plane .

PLL

Place the PLL loop filter components as close as possible to the FILT pin.

Do not place any digital or other high frequency traces near these components.

Use the values suggested in the datasheet with 10% tolerances or less.

Outputs (Both Data and Clocks)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which require more current that causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value $50\ \Omega$ to $200\ \Omega$ can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9880. If series resistors are used, place them as close as possible to the AD9880 pins (although try not to add vias or extra length to the output trace to move the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than $10\ \text{pF}$. This can be easily accomplished by

keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside of the AD9880 and creates more digital noise on its power supplies.

Digital Inputs

The digital inputs on the AD9880 were designed to work with $3.3\ \text{V}$ signals, but are tolerant of $5.0\ \text{V}$ signals. Therefore, no extra components need to be added if using $5.0\ \text{V}$ logic.

Any noise that enters the Hsync input trace can add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

COLOR SPACE CONVERTER (CSC) COMMON SETTINGS

Table 98. HDTV YCrCb (0 to 255) to RGB (0 to 255) (Default Setting for AD9880)

| | | | | | | | | |
|-----------------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x0C | 0x52 | 0x08 | 0x00 | 0x00 | 0x00 | 0x19 | 0xD7 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1C | 0x54 | 0x08 | 0x00 | 0x3E | 0x89 | 0x02 | 0x91 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x08 | 0x00 | 0x0E | 0x87 | 0x18 | 0xBD |

Table 99. HDTV YCrCb (16 to 235) to RGB (0 to 255)

| | | | | | | | | |
|-----------------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x47 | 0x2C | 0x04 | 0xA8 | 0x00 | 0x00 | 0x1C | 0x1F |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1D | 0xDD | 0x04 | 0xA8 | 0x1F | 0x26 | 0x01 | 0x34 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x04 | 0xA8 | 0x08 | 0x75 | 0x1B | 0x7B |

Table 100. SDTV YCrCb (0 to 255) to RGB (0 to 255)

| | | | | | | | | |
|-----------------|------------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x2A | 0xF8 | 0x08 | 0x00 | 0x00 | 0x00 | 0x1A | 0x84 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1A | 0x6A | 0x08 | 0x00 | 0x1D | 0x50 | 0x04 | 0x23 |
| Register | Blue/Cb Coeff. 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x08 | 0x00 | 0x0D | 0xDB | 0x19 | 0x12 |

Table 101. SDTV YCrCb (16 to 235) to RGB (0 to 255)

| | | | | | | | | |
|-----------------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x46 | 0x63 | 0x04 | 0xA8 | 0x00 | 0x00 | 0x1C | 0x84 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1C | 0xC0 | 0x04 | 0xA8 | 0x1E | 0x6F | 0x02 | 0x1E |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x04 | 0xA8 | 0x08 | 0x11 | 0x1B | 0xAD |

Table 102. RGB (0 to 255) to HDTV YCrCb (0 to 255)

| | | | | | | | | |
|-----------------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x08 | 0x2D | 0x18 | 0x93 | 0x1F | 0x3F | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x03 | 0x68 | 0x0B | 0x71 | 0x01 | 0x27 | 0x00 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1E | 0x21 | 0x19 | 0xB2 | 0x08 | 0x2D | 0x08 | 0x00 |

Table 103. RGB (0 to 255) to HDTV YCrCb (16 to 235)

| | | | | | | | | |
|-----------------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x07 | 0x06 | 0x19 | 0xA0 | 0x1F | 0x5B | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x02 | 0xED | 0x09 | 0xD3 | 0x00 | 0xFD | 0x01 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1E | 0x64 | 0x1A | 0x96 | 0x07 | 0x06 | 0x08 | 0x00 |

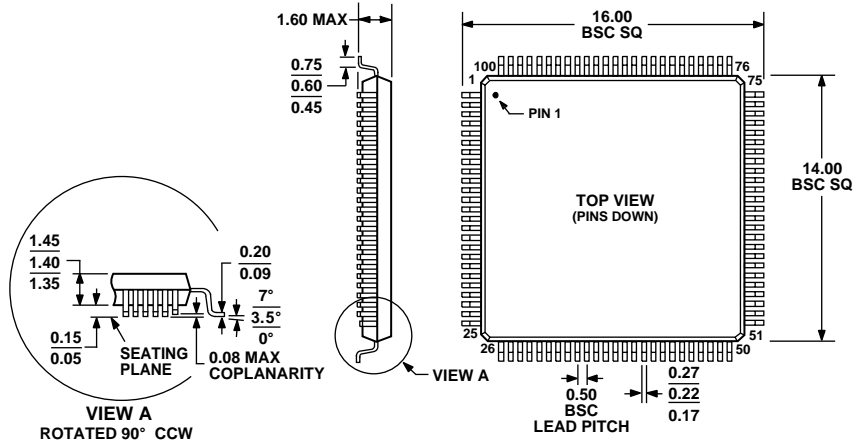
Table 104. RGB (0 to 255) to SDTV YCrCb (0 to 255)

| | | | | | | | | |
|-----------------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x08 | 0x2D | 0x19 | 0x27 | 0x1E | 0xAC | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x04 | 0xC9 | 0x09 | 0x64 | 0x01 | 0xD3 | 0x00 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1D | 0x3F | 0x1A | 0x93 | 0x08 | 0x2D | 0x08 | 0x00 |

Table 105. RGB (0 to 255) to SDTV YCrCb (16 to 235)

| | | | | | | | | |
|-----------------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x07 | 0x06 | 0x1A | 0x1E | 0x1E | 0xDC | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x04 | 0x1C | 0x08 | 0x11 | 0x01 | 0x91 | 0x01 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1D | 0xA3 | 0x1B | 0x57 | 0x07 | 0x06 | 0x08 | 0x00 |

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BED
 Figure 19. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model | Max Speeds (MHz) | | Temperature Range | Package Description | Package Option |
|-----------------------------|------------------|---------|-------------------|---------------------|----------------|
| | Analog | Digital | | | |
| AD9880KSTZ-100 ¹ | 100 | 100 | 0°C to 70°C | 100-Lead LQFP | ST-100 |
| AD9880KSTZ-150 ¹ | 150 | 150 | 0°C to 70°C | 100-Lead LQFP | ST-100 |
| AD9880/PCB | | | | Evaluation Board | |

¹ Z = Pb-free part.

NOTES

AD9880

NOTES