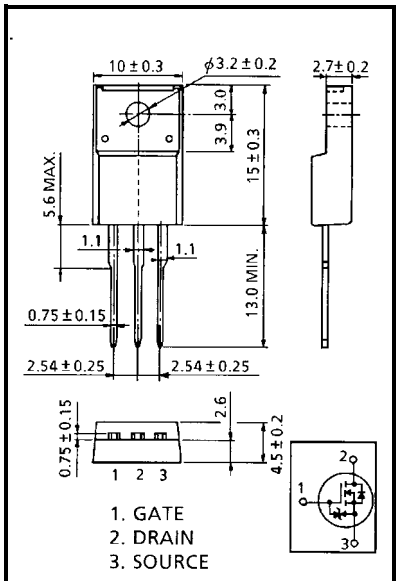
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L^2−π−MOSV)

2SK2507

Chopper Regulator, DC−DC Converter and Motor Drive Applications

- 4 V gate drive
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 0.034 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 16 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 50 V)
- Enhancement−mode : V_{th} = 0.8~2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-67
TOSHIBA	2-10R1B

Weight: 1.9 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	50	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	50	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	25	A
	Pulse (Note 1)	I_{DP}	75	
Drain power dissipation (Tc = 25°C)		P_D	30	W
Single pulse avalanche energy (Note 2)		E_{AS}	138	mJ
Avalanche current		I_{AR}	25	A
Repetitive avalanche energy (Note 3)		E_{AR}	3	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

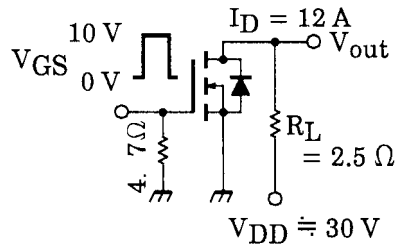
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	4.17	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	62.5	°C / W

Note 1: Please use devices on condition that the channel temperature is below 150°C.
Note 2: V_{DD} = 25 V, T_{ch} = 25°C (initial), L = 272 μH, R_G = 25 Ω, I_{AR} = 25 A
Note 3: Repetitive rating; Pulse width limited by maximum channel temperature.

This transistor is an electrostatic sensitive device.
Please handle with caution.

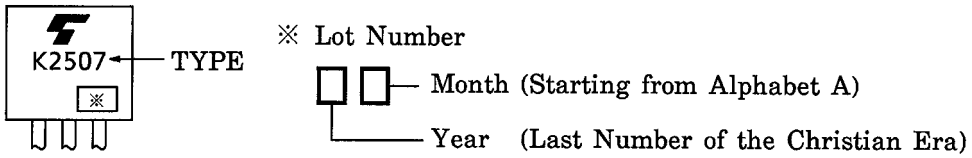
Electrical Characteristics (Ta = 25°C)

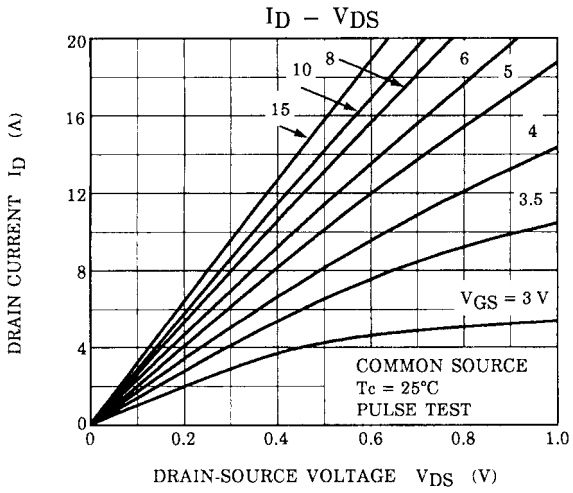
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	50	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 6 A	—	0.058	0.08	Ω
			V_{GS} = 10 V, I_D = 12 A	—	0.034	0.046	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 12 A	8.0	16	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	900	—	pF
Reverse transfer capacitance		C_{rss}		—	130	—	
Output capacitance		C_{oss}		—	370	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	15	—	ns
	Turn−on time	t_{on}		—	25	—	
	Fall time	t_f		—	30	—	
	Turn−off time	t_{off}		—	110	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 40 V, V_{GS} = 10 V, I_D = 25 A	—	25	—	nC
Gate−source charge		Q_{gs}		—	19	—	
Gate−drain (“miller”) charge		Q_{gd}		—	6	—	

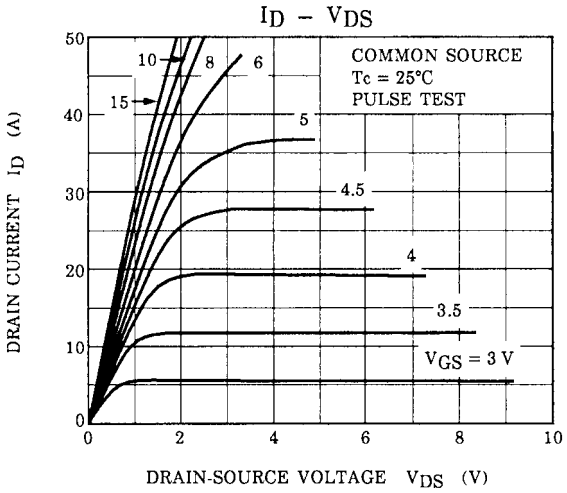
Source−Drain Ratings and Characteristics (Ta = 25°C)

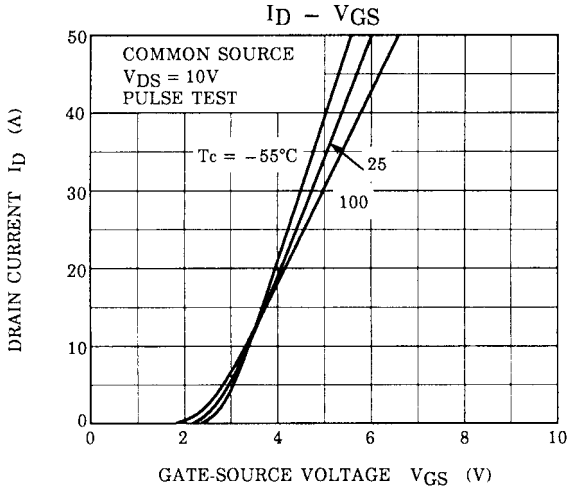
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	25	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	75	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 25 A, V_{GS} = 0 V	—	—	−1.6	V
Reverse recovery time	t_{rr}	I_{DR} = 25 A, V_{GS} = 0 V, dI_{DR} / dt = 50 A / μs	—	60	—	ns
Reverse recovery charge	Q_{rr}		—	45	—	μC

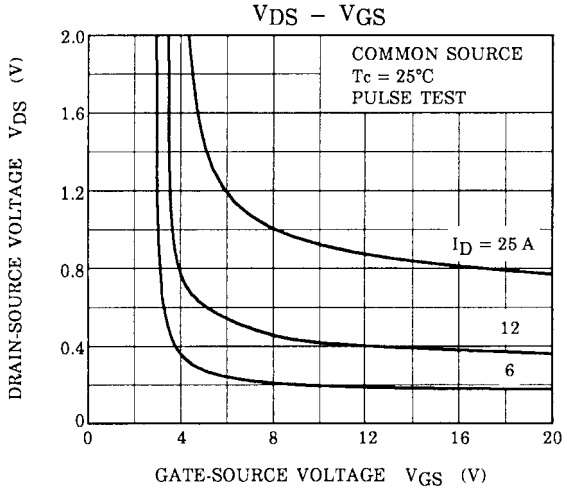
Marking

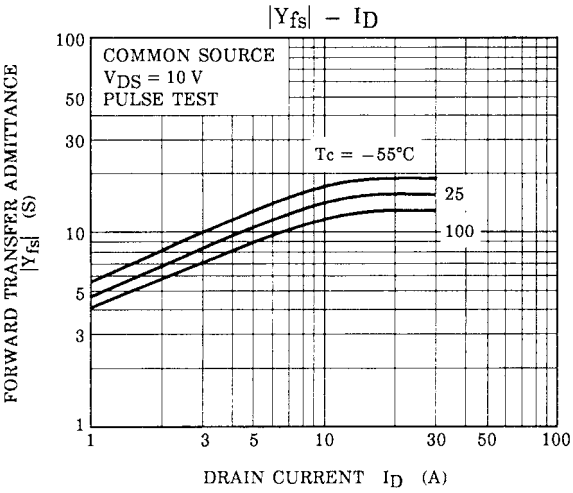


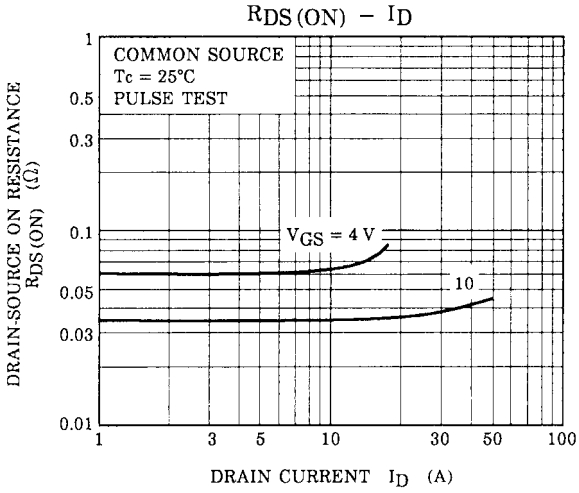

I_D – V_{DS}
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
10
8
6
5
15
4
3.5
V_{GS} = 3 V
COMMON SOURCE
Tc = 25°C
PULSE TEST


I_D – V_{DS}
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
COMMON SOURCE
Tc = 25°C
PULSE TEST
10
8
6
15
5
4.5
4
3.5
V_{GS} = 3 V

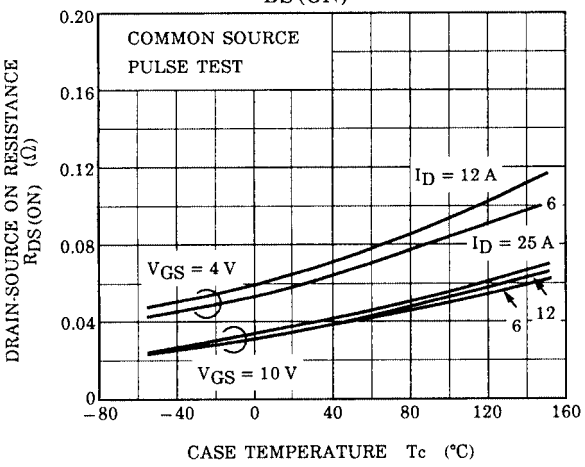

I_D – V_{GS}
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
V_{DS} = 10V
PULSE TEST
Tc = −55°C
25
100


V_{DS} – V_{GS}
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
Tc = 25°C
PULSE TEST
I_D = 25 A
12
6

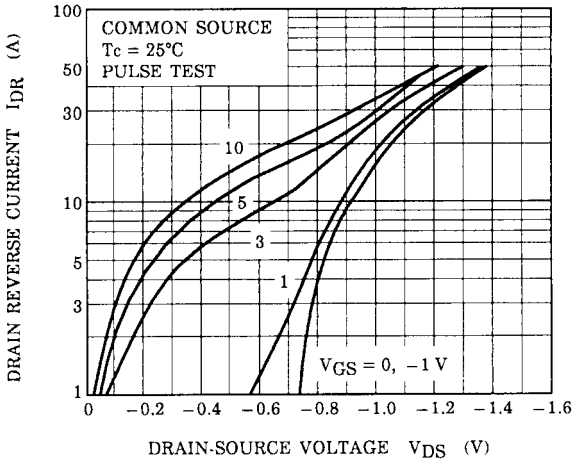

$|Y_{fs}|$ – I_D
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
Tc = −55°C
25
100


$R_{DS\,(ON)}$ – I_D
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (Ω)
DRAIN CURRENT I_D (A)
COMMON SOURCE
Tc = 25°C
PULSE TEST
V_{GS} = 4 V
10

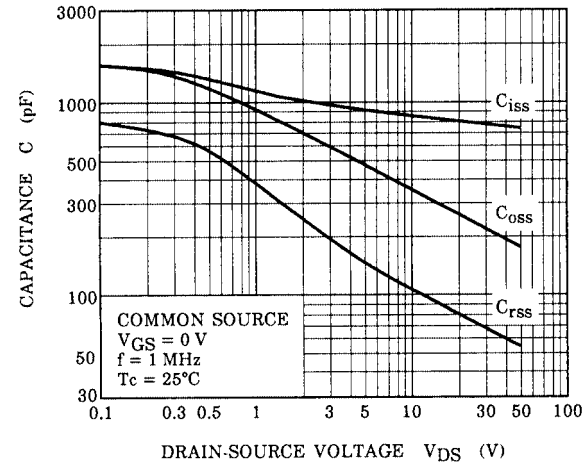
$R_{DS(ON)}$ – Tc



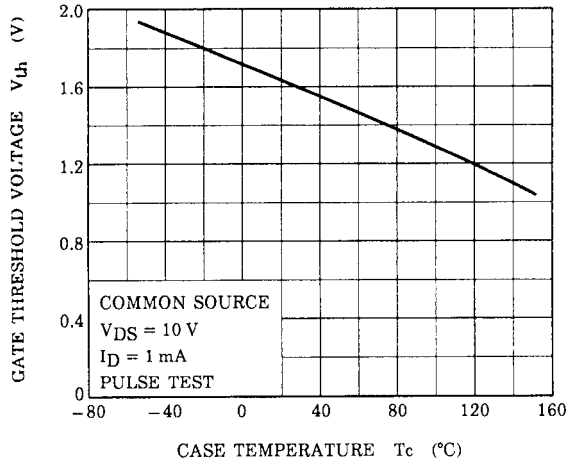
I_{DR} – V_{DS}



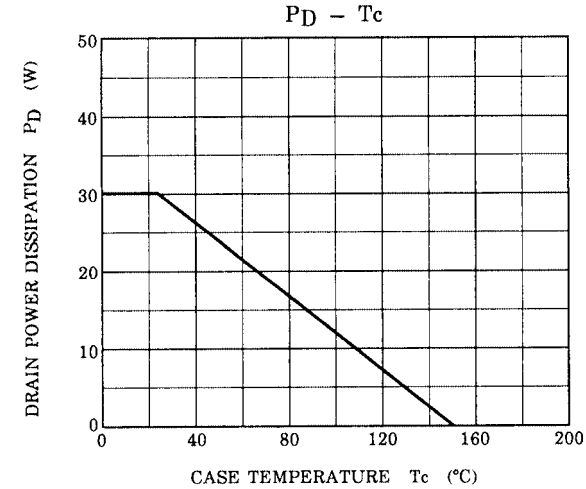
CAPACITANCE – V_{DS}



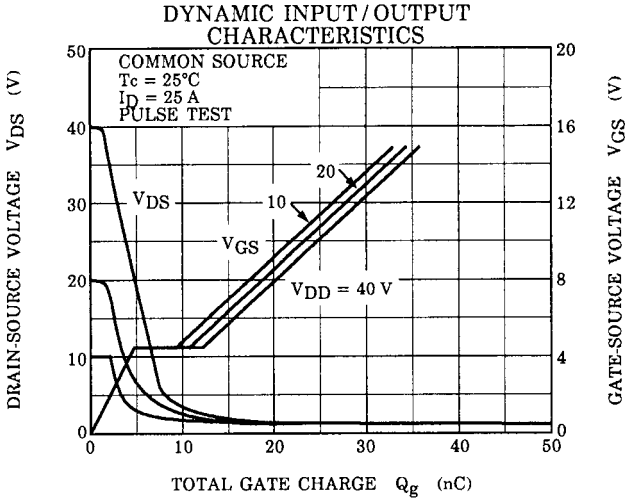
V_{th} – Tc



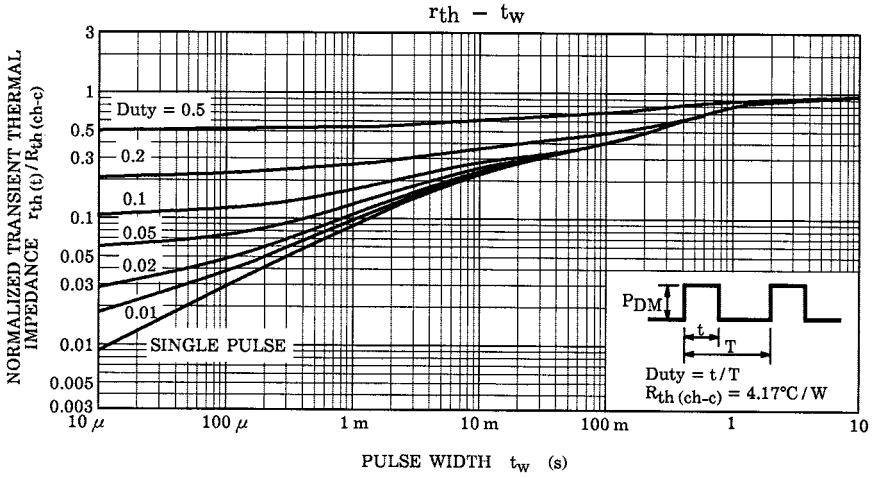
P_D – Tc



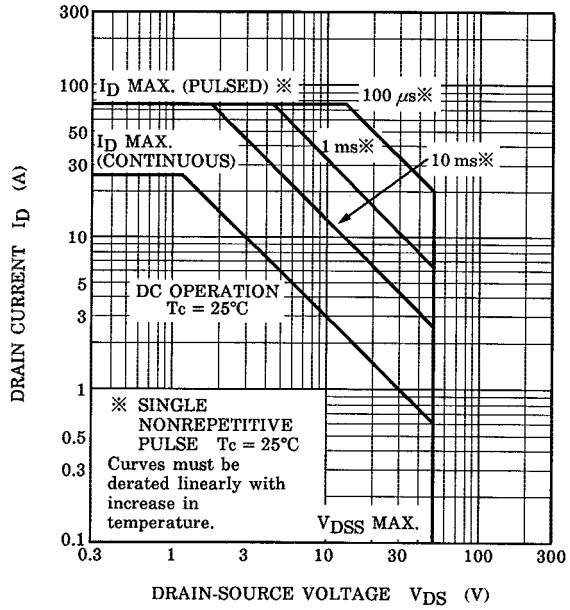
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



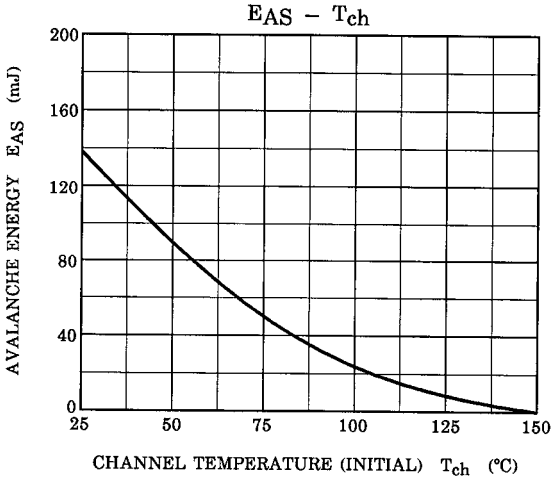
r_{th} – t_w

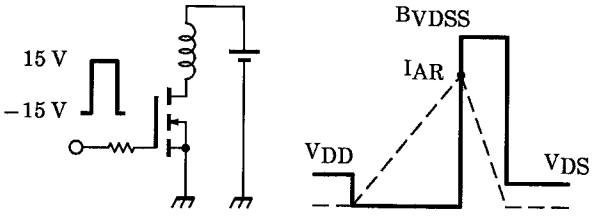


SAFE OPERATING AREA



E_{AS} – T_{ch}





$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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