AND8396/D

Implementing Power Factor Correction with the NCP1608

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APPLICATION NOTE

Introduction

The NCP1608 is a voltage mode power factor correction (PFC) controller designed to implement converters to comply with line current harmonic regulations. The device operates in critical conduction mode (CrM) for optimal performance in applications up to 350 W. Its voltage mode scheme enables it to obtain near unity power factor (PF) without the need for a line-sensing network. The output voltage is accurately controlled with an integrated high precision transconductance error amplifier. The controller also implements a comprehensive set of safety features that simplify system design.

This application note describes the design and implementation of a 400 V, 100 W, CrM boost PFC converter using the NCP1608. The converter exhibits high PF, low standby power dissipation, high active mode efficiency, and a variety of protection features.

The Need for PFC

Most electronic ballasts and switch−mode power supplies (SMPS) use a diode bridge rectifier and a bulk storage capacitor to produce a dc voltage from the utility ac line. This causes a non-sinusoidal current consumption and increases the stress on the power delivery infrastructure. Government regulations and utility requirements mandate control over line current harmonic content. Active PFC circuits are the most popular method to comply with these harmonic content requirements. System solutions consist of connecting a PFC pre−converter between the rectifier bridge and the bulk capacitor (Figure 1). The boost converter is the most popular topology for active PF correction. It produces a constant output voltage and consumes a sinusoidal input current from the line.

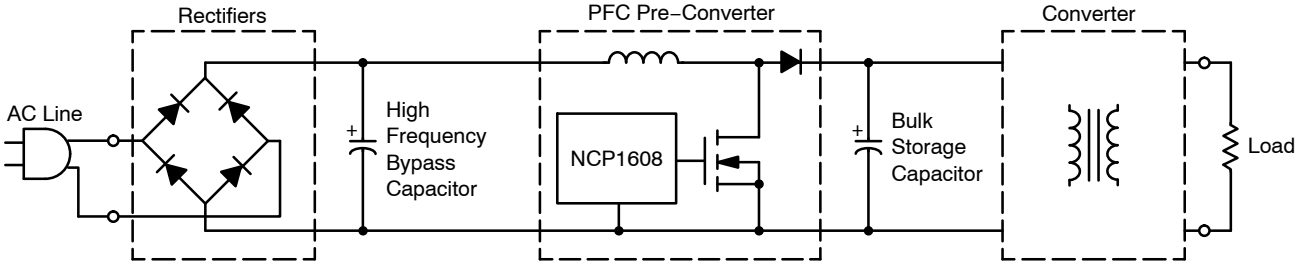

Figure 1. Active PFC Stage with the NCP1608

Basic Operation of a CrM Boost Converter

For medium power (< 350 W) applications, CrM is the preferred control method. CrM operates at the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In CrM, the drive on time begins when the inductor current reaches zero.

CrM combines the reduced peak current of CCM operation with the zero current switching of DCM operation. This control method causes the frequency to vary with the instantaneous line input voltage (V_{in}) and the output load. The operation and waveforms of a CrM PFC boost converter are illustrated in Figure 2. For detailed information on the operation of a CrM boost converter for PFC applications, please refer to AND8123 at www.onsemi.com.

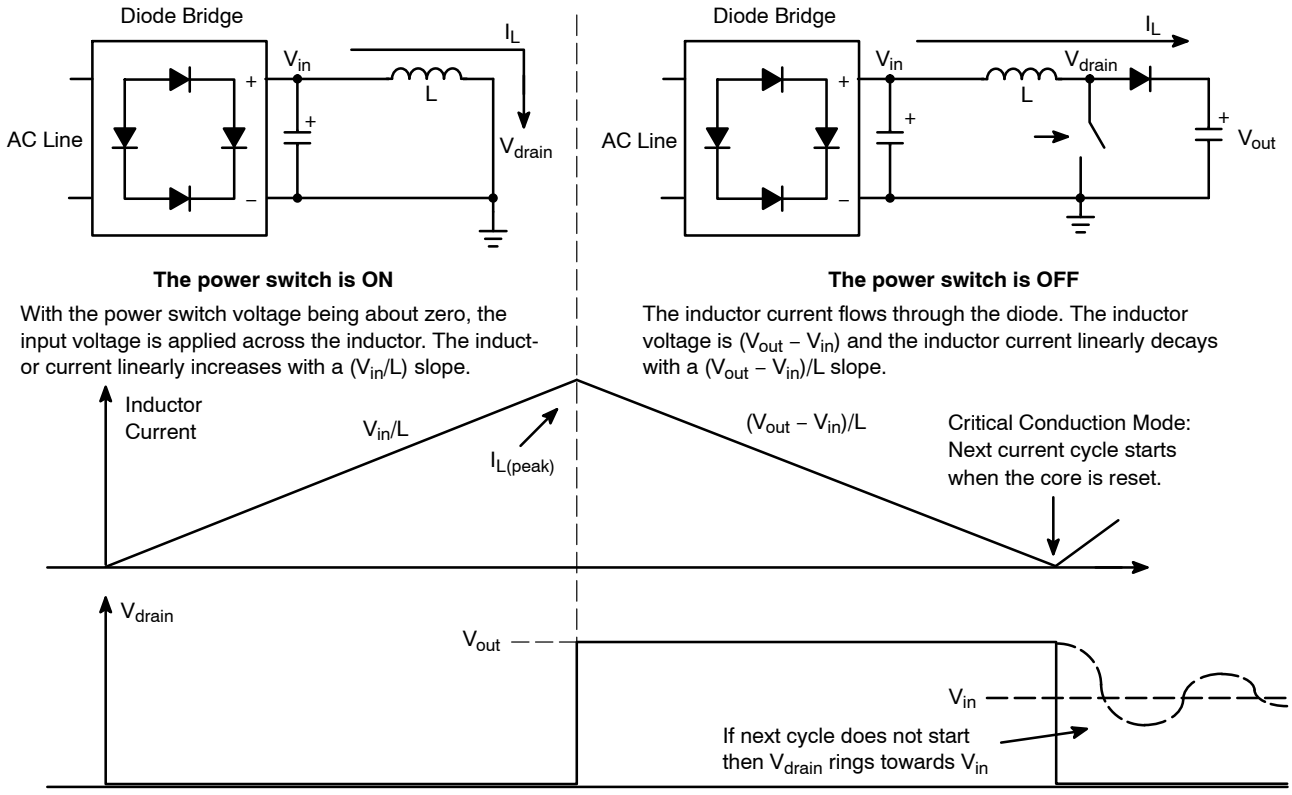

Figure 2. Schematic and Waveforms of an Ideal CrM Boost Converter

Features of the NCP1608

The NCP1608 is an excellent controller for robust medium power CrM boost PFC applications due to its integrated safety features, low impedance driver, high precision error amplifier, and low standby current consumption.

For detailed information on the operation of the NCP1608, please refer to NCP1608/D at www.onsemi.com.

A CrM boost pre-converter featuring the NCP1608 is shown in Figure 3.

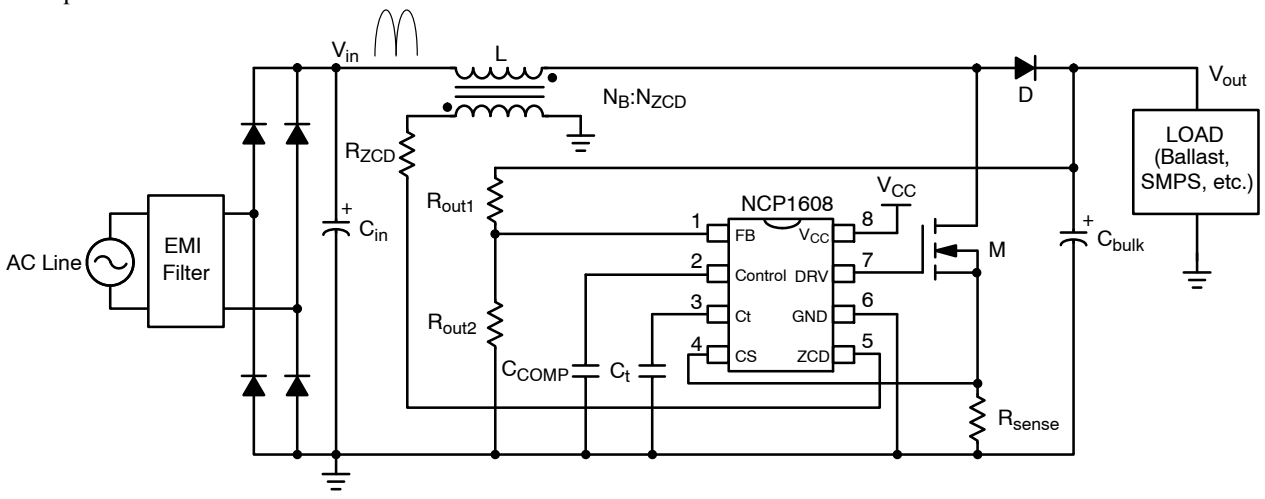

Figure 3. CrM Boost PFC Stage Featuring the NCP1608

The FB pin senses the boost output voltage through the resistor divider formed by R_{out1} and R_{out2}. The FB pin includes overvoltage protection (OVP), undervoltage protection (UVP), and floating pin protection (FPP). This pin is the input to the error amplifier. The output of the error amplifier is the Control pin.

A combination of resistors and capacitors connected between the Control and ground pins forms a compensation network that limits the bandwidth of the converter. For high PF, the bandwidth is set to less than 20 Hz. A capacitor connected to the Ct pin sets the maximum on time. The CS pin provides cycle−by−cycle overcurrent protection. The

internal comparator compares the voltage developed across R_{sense} (V_{CS}) to an internal reference (V_{ILIM}). The driver turns off when V_{CS} reaches V_{ILIM}. The ZCD pin senses the demagnetization of the boost inductor to turn on the drive. The drive on time begins after the ZCD pin voltage (V_{ZCD}) exceeds $V_{ZCD(ARM)}$ and then decreases to less than $V_{ZCD(TRIG)}$. A resistor in series with the ZCD winding limits the ZCD pin current.

The NCP1608 features a powerful output driver on the DRV pin. The driver is capable of switching the gates of large MOSFETs efficiently because of its low source and sink impedances. The driver includes active and passive pull−down circuits to prevent the output from floating high when the NCP1608 is disabled.

The V_{CC} pin is the supply pin of the controller. When V_{CC} is less than the turn on voltage ($V_{CC(on)}$), the current consumption of the device is less than 35 μA. This results in fast startup times and reduced standby power losses.

Design Procedure

The design of a CrM boost PFC converter is discussed in many ON Semiconductor application notes. Table 1 lists some examples.

This application note describes the design procedure for a 400 V, 100 W converter using the features of the NCP1608. A dedicated NCP1608 design tool that enables users to determine component values quickly is available at www.onsemi.com.

Table 1. Additional Resources for the Design and Understanding of CrM Boost PFC Circuits Available at www.onsemi.com.

AND8123	Power Factor Correction Stages Operating in Critical Conduction Mode
AND8016	Design of Power Factor Correction Circuits Using the MC33260
AND8154	NCP1230 90 W, Universal Input Adapter Power Supply with Active PFC
HBD853	Power Factor Correction Handbook

DESIGN STEP 1: Define the Required Parameters

The converter parameters are shown in Table 2.

Table 2. CONVERTER PARAMETERS

Parameter Name	Symbol	Value	Units
Minimum Line Input Voltage	Vac_{LL}	85	Vac
Maximum Line Input Voltage	Vac_{HL}	265	Vac
Minimum Line Frequency	$f_{line(MIN)}$	47	Hz
Maximum Line Frequency	$f_{line(MAX)}$	63	Hz
Output Voltage	V_{out}	400	V
Full Load Output Current	I_{out}	250	mA
Full Load Output Power	P_{out}	100	W
Maximum Output Voltage	$V_{out(MAX)}$	440	V
Minimum Switching Frequency	$f_{SW(MIN)}$	40	kHz
Minimum Full Load Efficiency	η	92	%
Minimum Full Load Power Factor	PF	0.9	–

DESIGN STEP 2: Calculate the Boost Inductor

The value of the boost inductor (L) is calculated using Equation 1:

$$L \le \frac{Vac^2 \cdot \left(\frac{V_{out}}{\sqrt{2}} - Vac\right) \cdot \eta}{\sqrt{2} \cdot V_{out} \cdot P_{out} \cdot f_{SW(MIN)}} \qquad \text{(eq. 1)}$$

To ensure that the switching frequency exceeds the minimum frequency, L is calculated at both the minimum and maximum rms input line voltage:

$$L_{LL} \le \frac{85^2 \cdot \left(\frac{400}{\sqrt{2}} - 85\right) \cdot 0.92}{\sqrt{2} \cdot 400 \cdot 100 \cdot 40\,k} = 581\ \mu H$$

Where L_{LL} is the inductor value calculated at Vac_{LL}.

$$L_{HL} \le \frac{265^2 \cdot \left(\frac{400}{\sqrt{2}} - 265\right) \cdot 0.92}{\sqrt{2} \cdot 400 \cdot 100 \cdot 40\,k} = 509\ \mu H$$

Where L_{HL} is the inductor value calculated at Vac_{HL}.

A value of 400 μH is selected. The inductance tolerance is ±15%. The maximum inductance (L_{MAX}) value is 460 μH. Equation 2 is used to calculate the minimum frequency at full load.

$$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L_{MAX} \cdot P_{out}} \cdot \left(1 - \frac{\sqrt{2} \cdot Vac}{V_{out}}\right) \qquad \text{(eq. 2)}$$

$$f_{SW(LL)} = \frac{85^2 \cdot 0.92}{2 \cdot 460\,\mu \cdot 100} \cdot \left(1 - \frac{\sqrt{2} \cdot 85}{400}\right) = 50.5\ \text{kHz}$$

$$f_{SW(HL)} = \frac{265^2 \cdot 0.92}{2 \cdot 460\,\mu \cdot 100} \cdot \left(1 - \frac{\sqrt{2} \cdot 265}{400}\right) = 44.3\ \text{kHz}$$

f_{SW} is equal to 50.5 kHz at Vac_{LL} and 44.3 kHz at Vac_{HL}.

DESIGN STEP 3: Size the Ct Capacitor

The Ct capacitor is sized to set the maximum on time for minimum line input voltage and maximum output power. The maximum on time is calculated using Equation 3:

$$t_{on(MAX)} = \frac{2 \cdot L_{MAX} \cdot P_{out}}{\eta \cdot Vac_{LL}^{\ 2}} \quad \text{(eq. 3)}$$

$$t_{on(MAX)} = \frac{2 \cdot 460\,\mu \cdot 100}{0.92 \cdot 85^2} = 13.8\ \mu\text{s}$$

Sizing Ct to an excessively large value causes the application to deliver excessive output power and reduces the control range at Vac_{HL} or low output power. It is recommended to size the Ct capacitor to a value slightly larger than that calculated by Equation 4:

$$Ct \geq \frac{2 \cdot P_{out} \cdot L_{MAX} \cdot I_{charge}}{\eta \cdot Vac_{LL}^{\ 2} \cdot V_{Ct(MAX)}} \quad \text{(eq. 4)}$$

Where I_{charge} and $V_{Ct(MAX)}$ are specified in the NCP1608 datasheet. To ensure that the controller sets the maximum on time to a value sufficient to deliver the required output power, the maximum I_{charge} and the minimum $V_{Ct(MAX)}$ values are used in the calculations for Ct.

From the NCP1608 datasheet:

– $V_{Ct(MAX)}$ = 4.775 V (minimum)

– I_{charge} = 297 μA (maximum)

Ct is equal to:

$$Ct \geq \frac{2 \cdot 100 \cdot 460\,\mu \cdot 297\,\mu}{0.92 \cdot 85^2 \cdot 4.775} = 860\ \text{pF}$$

A normalized value of 1 nF (±10%) provides sufficient margin. A value of 1.22 nF is selected for Total Harmonic Distortion (THD) reduction (see the **Additional THD Reduction** section of this application note for more information).

DESIGN STEP 4: Determine the ZCD Turns Ratio

To activate the ZCD detector of the NCP1608, the ZCD turns ratio is sized such that at least $V_{ZCD(ARM)}$ (1.55 V maximum) is applied to the ZCD pin during all operating conditions (see Figure 4). The boost winding to ZCD winding turns ratio ($N = N_B:N_{ZCD}$) is calculated using Equation 5.

$$N \leq \frac{V_{out} - \left(\sqrt{2} \cdot Vac_{HL}\right)}{V_{ZCD(ARM)}} \quad \text{(eq. 5)}$$

$$N \leq \frac{400 - \left(\sqrt{2} \cdot 265\right)}{1.55} = 16$$

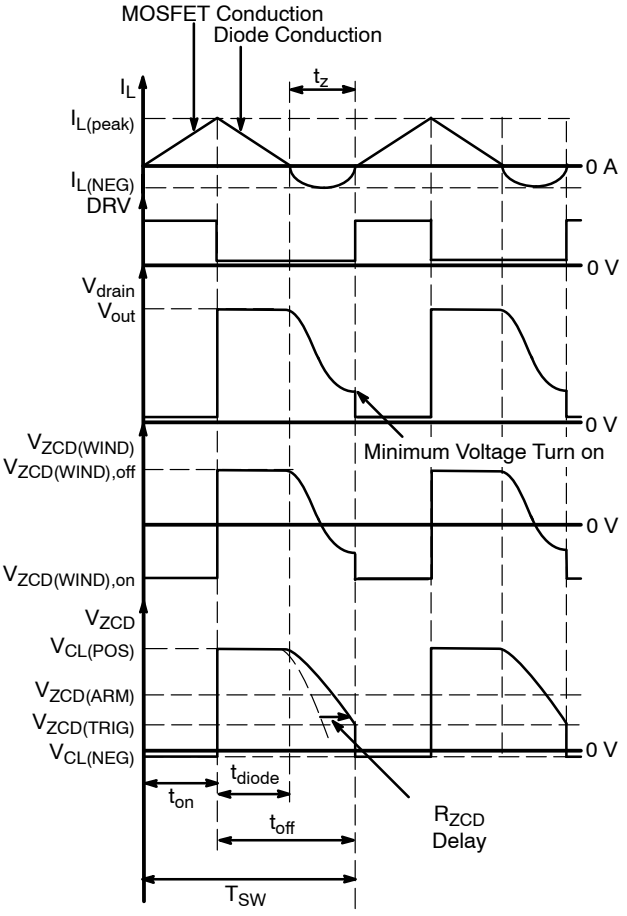

Figure 4. Realistic CrM Waveforms Using a ZCD Winding with R_{ZCD} and the ZCD Pin Capacitance

A turns ratio of 10 is selected for this design. R_{ZCD} is connected between the ZCD winding and the ZCD pin to limit the ZCD pin current. This current must be limited below 10 mA. R_{ZCD} is calculated using Equation 6:

$$R_{ZCD} \geq \frac{\sqrt{2} \cdot Vac_{HL}}{I_{ZCD(MAX)} \cdot N} \quad \text{(eq. 6)}$$

$$R_{ZCD} \geq \frac{\sqrt{2} \cdot 265}{10\ \text{m} \cdot 10} = 3.75\ \text{k}\Omega$$

The value of R_{ZCD} and the parasitic capacitance of the ZCD pin determine when the ZCD winding signal is detected and the drive turn on begins. A large R_{ZCD} value creates a long delay before detecting the ZCD event. In this case, the controller operates in DCM and the PF is reduced. If the R_{ZCD} value is too small, the drive turns on when the drain voltage is high and efficiency is reduced. A popular strategy for selecting R_{ZCD} is to use the R_{ZCD} value that achieves minimum drain voltage turn on. This value is found experimentally.

During the delay caused by R_{ZCD} and the ZCD pin capacitance, the equivalent drain capacitance ($C_{EQ(drain)}$) discharges through the path shown in Figure 5.

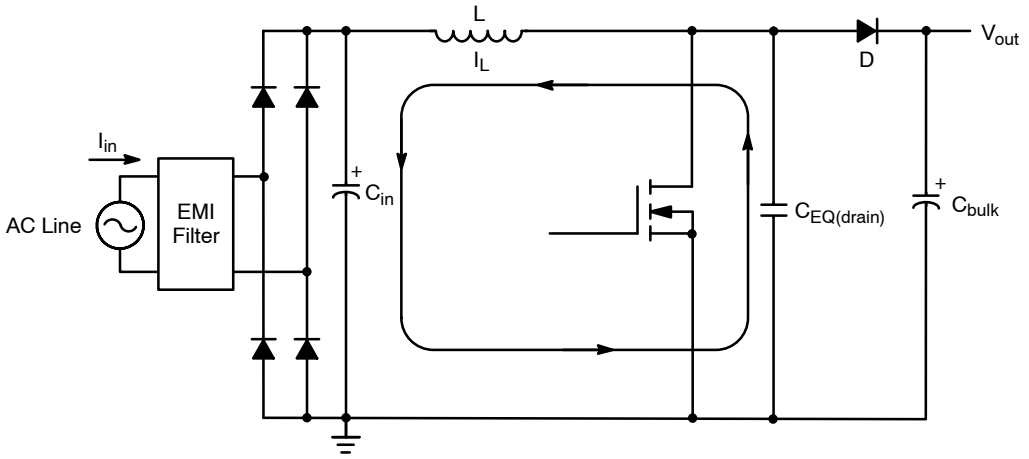

Figure 5. Equivalent Drain Capacitance Discharge Path

$C_{EQ(drain)}$ is the combined parasitic capacitances of the MOSFET, the diode, and the inductor. C_{in} is charged by the energy discharged by $C_{EQ(drain)}$. The charging of C_{in} reverse biases the bridge rectifier and causes the input current (I_{in}) to decrease to zero. The zero input current causes THD to increase. To reduce THD, the ratio (t_Z / T_{SW}) is minimized, where t_Z is the period from when I_L = 0 A to when the drive turns on. The ratio (t_Z / T_{SW}) is inversely proportional to the square root of L.

DESIGN STEP 5: Set the FB, OVP, and UVP Levels

R_{out1} and R_{out2} form a resistor divider that scales down V_{out} before it is applied to the FB pin. The error amplifier adjusts the on time of the drive to maintain the FB pin voltage equal to the error amplifier reference voltage (V_{REF}). The divider network bias current ($I_{bias(out)}$) selection is the first step in the calculation. The divider network bias current is selected to optimize the tradeoff of noise immunity and power dissipation. R_{out1} is calculated using the optimized bias current and output voltage using Equation 7:

$$R_{out1} = \frac{V_{out}}{I_{bias(out)}} \quad \text{(eq. 7)}$$

A bias current of 100 μA provides an acceptable tradeoff of power dissipation to noise immunity.

$$R_{out1} = \frac{400}{100\ \mu} = 4\ M\Omega$$

The output voltage signal is delayed before it is applied to the FB pin due to the time constant set by R_{out1} and the FB pin capacitance. R_{out1} must not be sized too large or this delay may cause overshoots of the OVP detection voltage.

R_{out2} is dependent on V_{out}, R_{out1}, and the internal feedback resistor (R_{FB}, shown in the NCP1608 specification table). R_{out2} is calculated using Equation 8:

$$R_{out2} = \frac{R_{out1} \cdot R_{FB}}{R_{FB} \cdot \left(\frac{V_{out}}{V_{REF}} - 1\right) - R_{out1}} \quad \text{(eq. 8)}$$

$$R_{out2} = \frac{4\ M \cdot 4.6\ M}{4.6\ M \cdot \left(\frac{400}{2.5} - 1\right) - 4\ M} = 25.3\ k\Omega$$

R_{out2} is selected as 25.5 kΩ for this design.

Using the selected resistor, the resulting output voltage is calculated using Equation 9:

$$V_{out} = V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right) \quad \text{(eq. 9)}$$

$$V_{out} = 2.5 \cdot \left(4\ M \cdot \frac{25.5\ k + 4.6\ M}{25.5\ k \cdot 4.6\ M} + 1\right) = 397\ V$$

The low bandwidth of the PFC stage causes overshoots during transient loads or during startup. The NCP1608 includes an integrated OVP circuit to prevent the output from exceeding a safe voltage. The OVP circuit compares V_{FB} to the internal overvoltage detect threshold voltage to determine if an OVP fault occurs. The OVP detection voltage is calculated using Equation 10:

$$V_{out(OVP)} = \frac{V_{OVP}}{V_{REF}} \cdot V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right) \quad \text{(eq. 10)}$$

$$V_{out(OVP)} = 1.06 \cdot 2.5 \cdot \left(4\ M \cdot \frac{25.5\ k + 4.6\ M}{25.5\ k \cdot 4.6\ M} + 1\right) = 421\ V$$

The output capacitor (C_{bulk}) value is sized to be large enough so that the peak-to-peak output voltage ripple ($V_{ripple(peak-peak)}$) is less than the OVP detection voltage. C_{bulk} is calculated using Equation 11:

$$C_{bulk} \geq \frac{P_{out}}{2 \cdot \pi \cdot V_{ripple(peak-peak)} \cdot f_{line} \cdot V_{out}} \quad \text{(eq. 11)}$$

Where f_{line} = 47 Hz is the worst case for the ripple voltage and $V_{ripple(peak-peak)}$ < 42 V.

$$C_{bulk} \geq \frac{100}{2 \cdot \pi \cdot 42 \cdot 47 \cdot 400} = 20\ \mu F$$

The value of C_{bulk} is selected as 68 μF to reduce $V_{ripple(peak-peak)}$ to less than 15 V. This results in a peak output voltage of 406.25 V, which is less than the peak output OVP detection voltage (421 V).

The NCP1608 includes undervoltage protection (UVP). During startup, C_{bulk} charges to the peak of the ac line voltage. If C_{bulk} does not charge to a minimum voltage, the NCP1608 detects an UVP fault. The UVP detection voltage is calculated using Equation 12:

$$V_{out(UVP)} = V_{UVP} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1 \right) \quad \text{(eq. 12)}$$

$$V_{out(UVP)} = 0.31 \cdot \left(4\ M \cdot \frac{25.5\ k + 4.6\ M}{25.5\ k \cdot 4.6\ M} + 1 \right) = 49\ V$$

The UVP feature protects against open loop conditions in the feedback loop. If the FB pin is inadvertently floating (perhaps due to a bad solder joint), the coupling within the system may cause V_{FB} to be within the regulation range (i.e. $V_{UVP} < V_{FB} < V_{REF}$). The controller responds by delivering maximum power. The output voltage increases and over stresses the components. The NCP1608 includes a feature to protect the system if FB is floating. The internal pull-down resistor (R_{FB}) ensures that V_{FB} is below the UVP threshold if the FB pin is floating.

If the FB pin floats during operation, V_{FB} begins decreasing from V_{REF}. The rate of decrease depends on R_{FB} and the FB pin parasitic capacitance. As V_{FB} decreases, $V_{Control}$ increases, which causes the on time to increase until $V_{FB} < V_{UVP}$. When $V_{FB} < V_{UVP}$, the UVP fault is detected and the controller is disabled. The sequence is depicted in Figure 6.

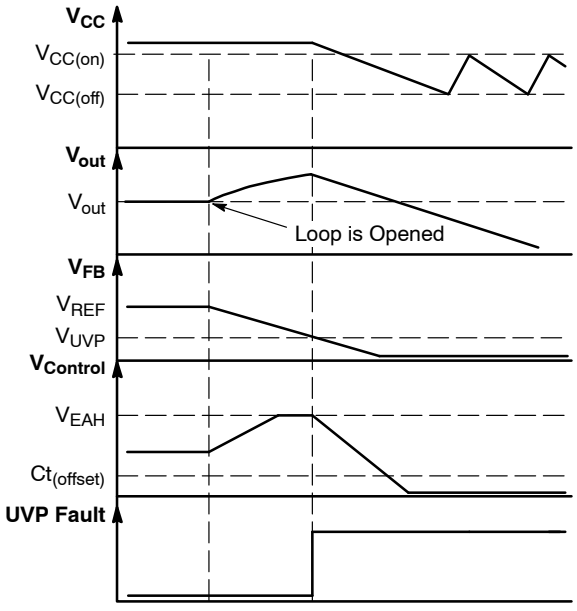

Figure 6. UVP Operation if Loop is Opened During Operation

DESIGN STEP 6: Size the Power Components

The power components are sized such that there is sufficient margin to sustain the currents and voltages applied to them. At minimum line input voltage and maximum output power the inductor peak current is at the maximum, which causes the greatest stress to the power components. The components are referenced in Figure 3.

1. The inductor peak current ($I_{L(peak)}$) is calculated using Equation 13:

$$I_{L(peak)} = \frac{\sqrt{2} \cdot 2 \cdot P_{out}}{\eta \cdot Vac} \quad \text{(eq. 13)}$$

$$I_{L(peak)} = \frac{\sqrt{2} \cdot 2 \cdot 100}{0.92 \cdot 85} = 3.62\ A$$

The inductor rms current ($I_{L(RMS)}$) is calculated using Equation 14:

$$I_{L(RMS)} = \frac{2 \cdot P_{out}}{\sqrt{3} \cdot Vac \cdot \eta} \quad \text{(eq. 14)}$$

$$I_{L(RMS)} = \frac{2 \cdot 100}{\sqrt{3} \cdot 85 \cdot 0.92} = 1.48\ A$$

2. The output diode (D) rms current ($I_{D(RMS)}$) is calculated using Equation 15:

$$I_{D(RMS)} = \frac{4}{3} \cdot \sqrt{\frac{\sqrt{2} \cdot 2}{\pi}} \cdot \frac{P_{out}}{\eta \cdot \sqrt{Vac \cdot V_{out}}} \quad \text{(eq. 15)}$$

$$I_{D(RMS)} = \frac{4}{3} \cdot \sqrt{\frac{\sqrt{2} \cdot 2}{\pi}} \cdot \frac{100}{0.92 \cdot \sqrt{85 \cdot 400}} = 0.75\ A$$

The diode maximum voltage is equal to V_{OVP} (421 V) plus the overshoot caused by parasitic contributions. For this demonstration board, the maximum voltage is 450 V. A 600 V diode provides a 25% derating factor. The MUR460 (4 A/600 V) diode is selected for this design.

3. The MOSFET (M) rms current ($I_{M(RMS)}$) is calculated using Equation 16:

$$I_{M(RMS)} = \frac{2}{\sqrt{3}} \cdot \left(\frac{P_{out}}{\eta \cdot Vac} \right) \cdot \sqrt{1 - \left(\frac{\sqrt{2} \cdot 8 \cdot Vac}{3 \cdot \pi \cdot V_{out}} \right)}$$

$$I_{M(RMS)} = \frac{2}{\sqrt{3}} \cdot \left(\frac{100}{0.92 \cdot 85} \right) \cdot \sqrt{1 - \left(\frac{\sqrt{2} \cdot 8 \cdot 85}{3 \cdot \pi \cdot 400} \right)} = 1.27\ A \quad \text{(eq. 16)}$$

The MOSFET maximum voltage is equal to V_{OVP} (421 V) plus the overshoot caused by parasitic contributions. For this demonstration board, the maximum voltage is 450 V. A 560 V MOSFET provides a 20% derating factor. The SPP12N50C3 (11.6 A/560 V) MOSFET is selected for this design.

4. The current sense resistor (R_{sense}) limits the maximum inductor peak current of the MOSFET and is calculated using Equation 17:

$$R_{sense} = \frac{V_{ILIM}}{I_{L(peak)}} \quad \text{(eq. 17)}$$

Where V_{ILIM} is specified in the NCP1608 datasheet.

$$R_{sense} = \frac{0.5}{3.62} = 0.138\ \Omega$$

The current sense resistor is selected as 0.125 Ω for decreased power dissipation. The resulting maximum inductor peak current is 4 A. Since the MOSFET continuous current rating is 7 A (for T_C = 100°C as specified in the manufacturer's datasheet) and the inductor saturation current is 4.7 A, the maximum peak inductor current of 4 A is sufficiently low.

The power dissipated by R_{sense} is calculated using Equation 18:

$$P_{R_{sense}} = I_{M(RMS)}{}^2 \cdot R_{sense} \qquad \text{(eq. 18)}$$

$$P_{R_{sense}} = 1.27^2 \cdot 0.125 = 0.202\ W$$

5. The output capacitor (C_{bulk}) rms current is calculated using Equation 19:

$$I_{C(RMS)} = \sqrt{\frac{\sqrt{2} \cdot 32 \cdot P_{out}{}^2}{9 \cdot \pi \cdot Vac \cdot V_{out} \cdot \eta^2} - I_{load(RMS)}{}^2} \qquad \text{(eq. 19)}$$

$$I_{C(RMS)} = \sqrt{\frac{\sqrt{2} \cdot 32 \cdot 100^2}{9 \cdot \pi \cdot 85 \cdot 400 \cdot 0.92^2} - 0.25^2} = 0.7\ A$$

The value of C_{bulk} is calculated in Step 5 to ensure a ripple voltage that is sufficiently low to not trigger OVP. The value of C_{bulk} may need to be increased so that the rms current does not exceed the ratings of C_{bulk}.

The voltage rating of C_{bulk} is required to be greater than $V_{out(OVP)}$. Since $V_{out(OVP)}$ is 421 V, C_{bulk} is selected to have a voltage rating of 450 V.

DESIGN STEP 7: Supply V_{CC} Voltage

The typical method to charge the V_{CC} capacitor (C_{Vcc}) to $V_{CC(on)}$ is to connect a resistor between V_{in} and V_{CC}. The low startup current consumption of the NCP1608 enables most of the resistor current to charge C_{Vcc} during startup. The low startup current consumption enables faster startup times and reduces standby power dissipation. The startup time ($t_{startup}$) is approximated with Equation 20:

$$t_{startup} = \frac{C_{V_{CC}} \cdot V_{CC(on)}}{\frac{\sqrt{2} \cdot Vac}{R_{start}} - I_{CC(startup)}} \qquad \text{(eq. 20)}$$

Where $I_{CC(startup)}$ = 24 μA (typical).

If C_{Vcc} is selected as a 47 μF capacitor and R_{start} is selected as 660 kΩ, $t_{startup}$ is equal to:

$$t_{startup} = \frac{47\ \mu \cdot 12}{\frac{\sqrt{2} \cdot 85}{660\ k} - 24\ \mu} = 3.57\ s$$

Once V_{CC} reaches $V_{CC(on)}$, the internal references and logic of the NCP1608 turn on. The NCP1608 includes an undervoltage lockout (UVLO) feature that ensures that the NCP1068 remains enabled unless V_{CC} decreases to less than $V_{CC(off)}$. This hysteresis ensures sufficient time for another supply to power V_{CC}.

The ZCD winding is a possible solution, but the voltage induced on the winding may be less than the required voltage. An alternative is to implement a charge pump to supply V_{CC}. A schematic is illustrated in Figure 7.

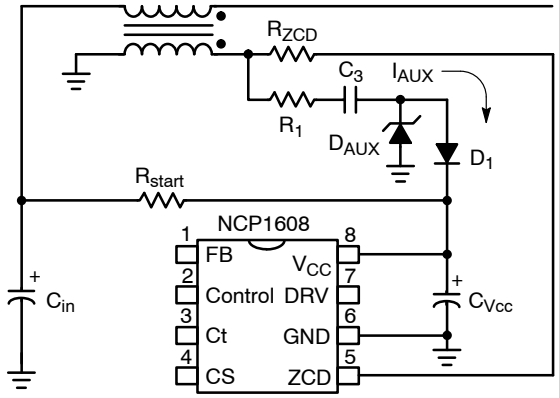

Figure 7. The ZCD Winding Supplies V_{CC} using a Charge Pump Circuit

C3 stores the energy for the charge pump. R1 limits the current by reducing the rate of voltage change. D_{AUX} supplies current to C3 when its cathode is negative. When its cathode is positive it limits the maximum voltage applied to V_{CC}.

The voltage change across C3 over one period is calculated using Equation 21:

$$\Delta V_{C3} = \frac{V_{out}}{N} - V_{CC} \qquad \text{(eq. 21)}$$

The current that charges C_{Vcc} is calculated using Equation 22:

$$I_{AUX} = C3 \cdot f_{SW} \cdot \Delta V_{C3} = C3 \cdot f_{SW} \cdot \left(\frac{V_{out}}{N} - V_{CC}\right) \qquad \text{(eq. 22)}$$

For off−line ac-dc applications that require PFC, a 2-stage approach is typically used. The first stage is the CrM boost PFC. This supplies the 2nd stage, which is traditionally an isolated flyback or forward converter. This solution is cost−effective and exhibits excellent performance. During low output power conditions the PFC stage is not required and reduces efficiency. Advanced controllers, such as the NCP1230 and NCP1381 detect the low output power condition and shut down the PFC stage by removing PFC(V_{CC}) (Figure 8).

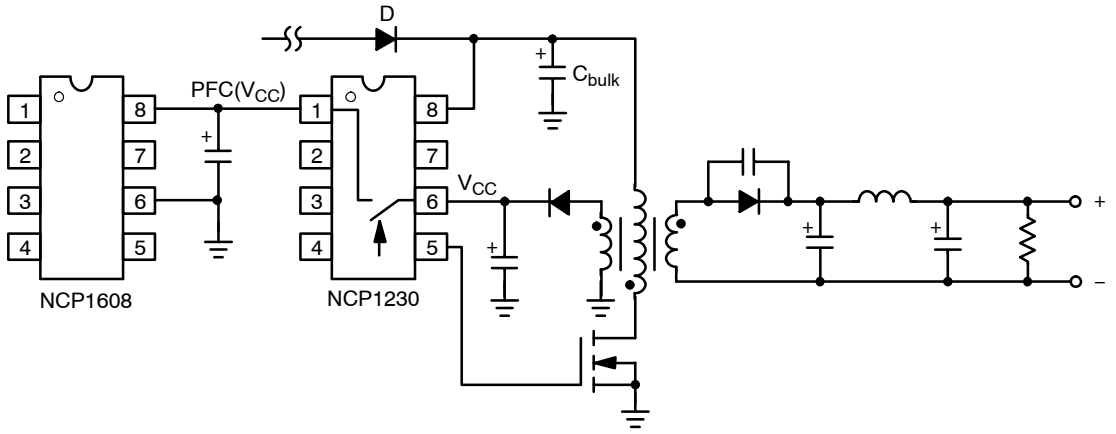

Figure 8. Using the SMPS Controller to Supply Power to the NCP1608

DESIGN STEP 8: Limit the Inrush Current

The sudden application of the ac line voltage to the PFC pre−converter causes an inrush current and a resonant voltage overshoot that is several times the normal value. Resizing the power components to handle inrush current and a resonant voltage overshoot is cost prohibitive.

1. External Inrush Current Limiting Resistor

A NTC (negative temperature coefficient) thermistor connected in series with the diode limits the inrush current (Figure 9). The resistance of the NTC decreases from a few ohms to a few milliohms as the NTC is heated by the I^2R power dissipation. However, an NTC resistor may not be sufficient to protect the inductor and C_{bulk} from inrush current during a brief interruption of the ac line voltage, such as during ac line dropout and recovery.

2. Startup Bypass Rectifier

A rectifier is connected from V_{in} to V_{out} (Figure 10). This bypasses the inductor and diverts the startup current directly to C_{bulk}. C_{bulk} is charged to the peak ac line voltage without resonant overshoot and without excessive inductor current. After startup, D_{bypass} is reverse biased and does not interfere with the boost converter.

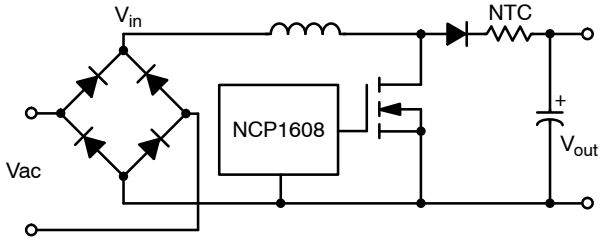

Figure 9. Use a NTC to Limit the Inrush Current Through the Inductor

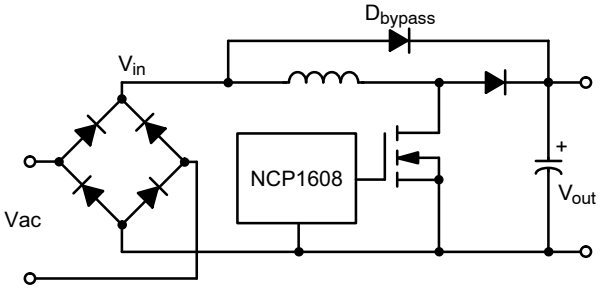

Figure 10. Use a Second Diode to Route the Inrush Current Away from the Inductor

DESIGN STEP 9: Develop the Compensation Network

The pre−converter is compensated to ensure stability over the input voltage and output power range. To compensate the loop, a compensation network is connected between the Control and ground pins. To ensure high PF, the bandwidth of the loop is set below 20 Hz. A type 2 compensation network is selected for this design to increase the phase margin. The type 2 compensation network is shown in Figure 11.

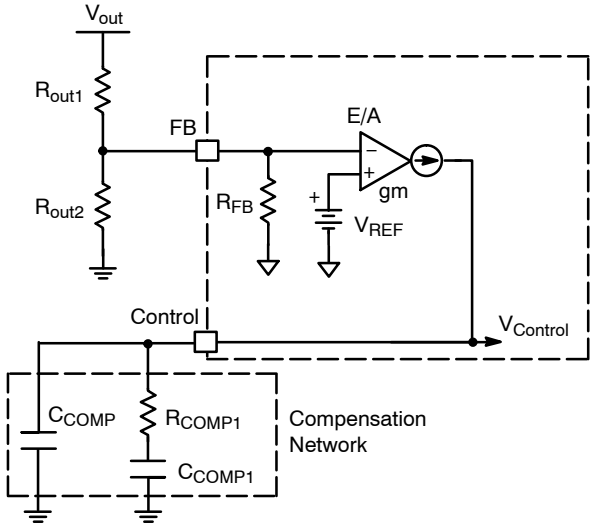

Figure 11. Type 2 Compensation Network

The type 2 network is composed of C_{COMP}, C_{COMP1}, and R_{COMP1}. C_{COMP1} sets the crossover frequency (f_{CROSS}) and is calculated using Equation 23:

$$C_{COMP1} = \frac{gm}{2 \cdot \pi \cdot f_{CROSS}} \quad \text{(eq. 23)}$$

For this design, f_{CROSS} is set to 5 Hz at the average input voltage (175 Vac) to decrease THD and gm is specified in the NCP1608 datasheet:

$$C_{COMP1} = \frac{110\ \mu}{2 \cdot \pi \cdot 5} = 3.5\ \mu F$$

A normalized value of 3.3 μF is selected, which sets f_{CROSS} to 5.3 Hz.

The addition of R_{COMP1} causes a zero in the loop response. The zero frequency (f_{zero}) is typically set to half the crossover frequency, which is 2.5 Hz for this case. R_{COMP1} is calculated using Equation 24:

$$R_{COMP1} = \frac{1}{2 \cdot \pi \cdot f_{zero} \cdot C_{COMP}} \quad \text{(eq. 24)}$$

$$R_{COMP1} = \frac{1}{2 \cdot \pi \cdot 2.5 \cdot 3.3\ \mu} = 19.3\ k\Omega$$

R_{COMP1} is selected as 20 kΩ.

C_{COMP} is used to filter high frequency noise and is set to between 1/10 and 1/5 of C_{COMP1}. For this design, C_{COMP} is selected to be 1/5 of C_{COMP1}.

$$C_{COMP} = \left(\frac{1}{5}\right) \cdot 3.3\ \mu = 0.66\ \mu F$$

C_{COMP} is selected as 0.68 μF.

The phase margin and crossover frequency change with the ac line voltage. It is critical that the gain and phase are measured for all operating conditions. The measurement setup using a network analyzer is shown in Figure 12.

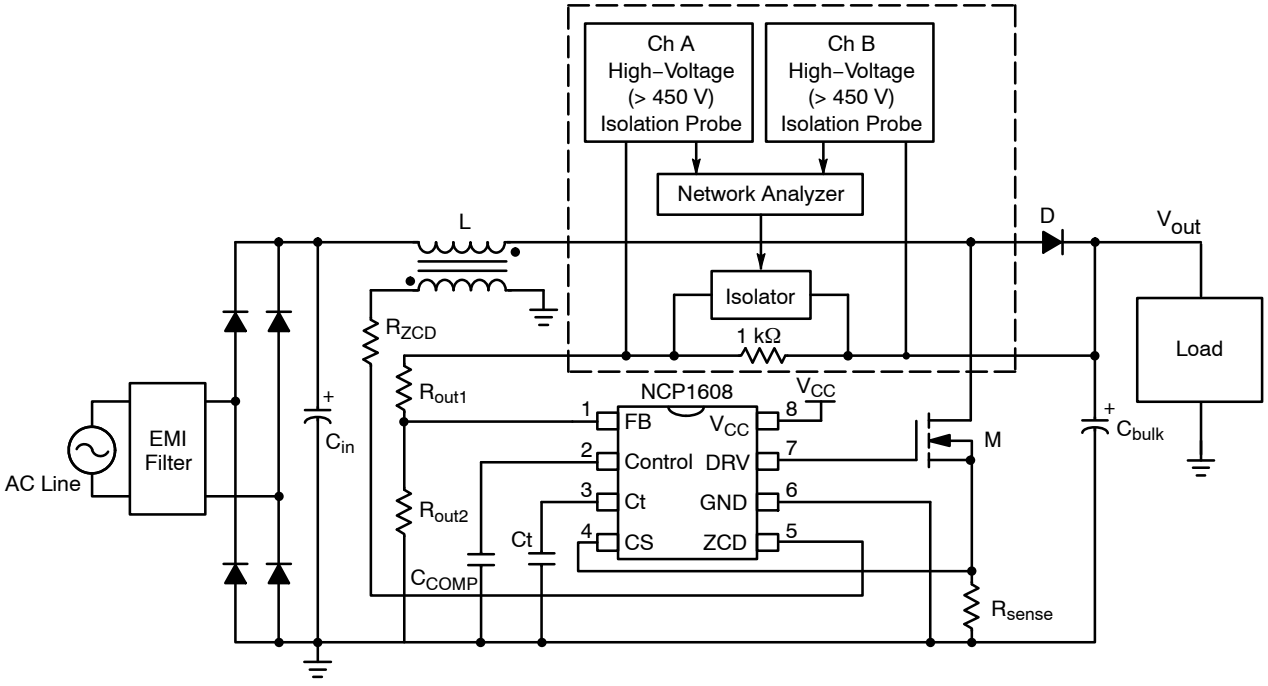

Figure 12. Gain-Phase Measurement Setup for a Boost PFC Pre−Converter

There is a tradeoff of transient response for PF and THD. The low bandwidth of the feedback loop reduces the Control pin ripple voltage. The reduction of the Control pin ripple voltage increases PF and reduces THD, but increases the magnitude of overshoots and undershoots.

Additional THD Reduction

The constant on time architecture of the NCP1608 provides flexibility in optimizing each design.

The following design guidelines provide methods to further improve PF and THD.

1. Improve the THD/PF at Maximum Output Power by Increasing the On Time at the Zero Crossing:

One disadvantage of constant on time CrM control is that at the zero crossing of the ac line, the instantaneous input voltage is not large enough to store sufficient energy in the inductor during the constant on time. Minimal energy is processed and “zero crossing distortion” is produced as shown in Figure 13.

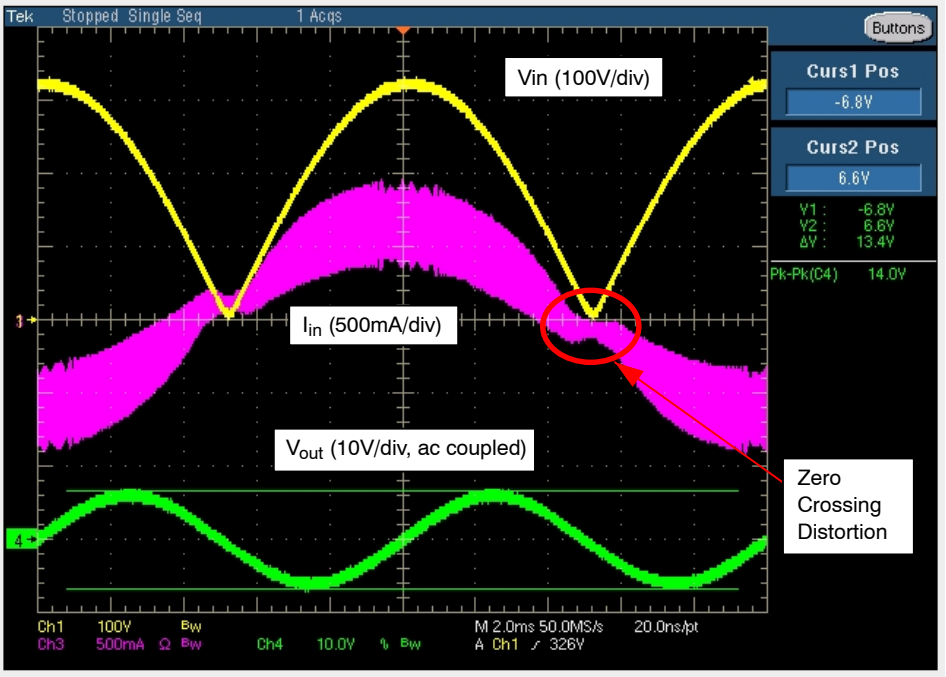

Figure 13. Full Load Input Current (V_{in} = 230 Vac 50 Hz, I_{out} = 250 mA)

The zero crossing distortion increases the THD and decreases the PF of the pre-converter. To meet IEC61000-3-2 requirements, this is generally not an issue as the NCP1608 reduces input current distortion with sufficient margin. If improved THD or PF is required, then zero crossing distortion must be reduced. To reduce the zero crossing distortion, the on time is increased as the instantaneous input voltage is decreasing to zero. This increases the time for the inductor current to build up and reduces the instantaneous input voltage at which the distortion begins.

This method is implemented by connecting a resistor from V_{in} to Ct as shown in Figure 14. The resistor current (I_{CTUP}) is proportional to the instantaneous line voltage and is summed with I_{charge} to increase the charging current of Ct.

I_{CTUP} is maximum at the peak of V_{in} and is approximately zero at the zero crossing.

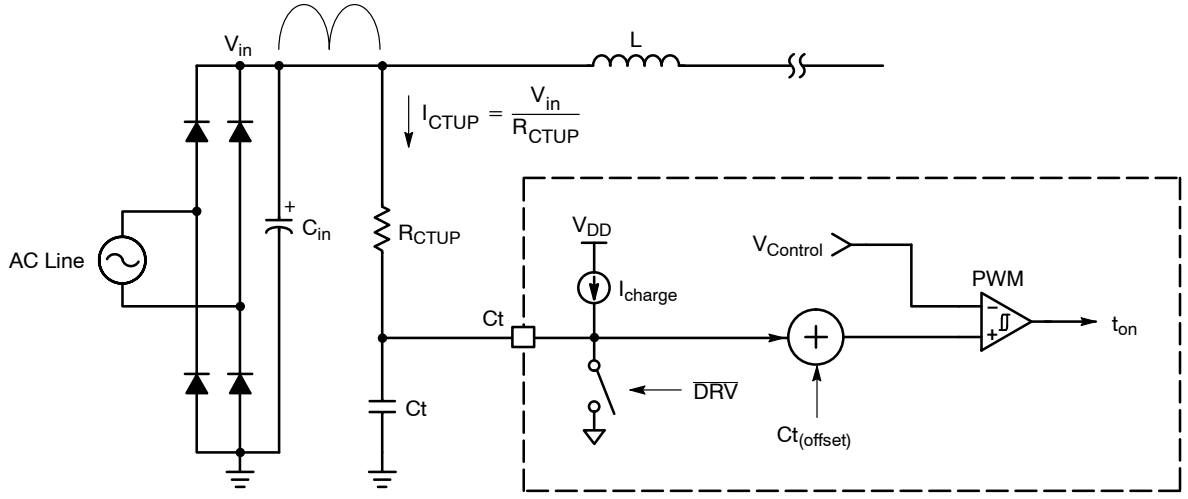

Figure 14. .Add R_{CTUP} to Modulate the On Time and Reduce Zero Crossing Distortion

The increased charging current at the peak of V_{in} enables the increased sizing of the Ct capacitor without reducing the control range at Vac_{HL} or low output power. The larger value of the Ct capacitor increases the on time near the zero crossing and reduces the zero crossing distortion as shown in Figure 15. This reduces the frequency variation over the ac line cycle. The tradeoff is that the standby power dissipation is increased by R_{CTUP}. The designer must balance the desired THD and PF performance with the standby power dissipation requirements.

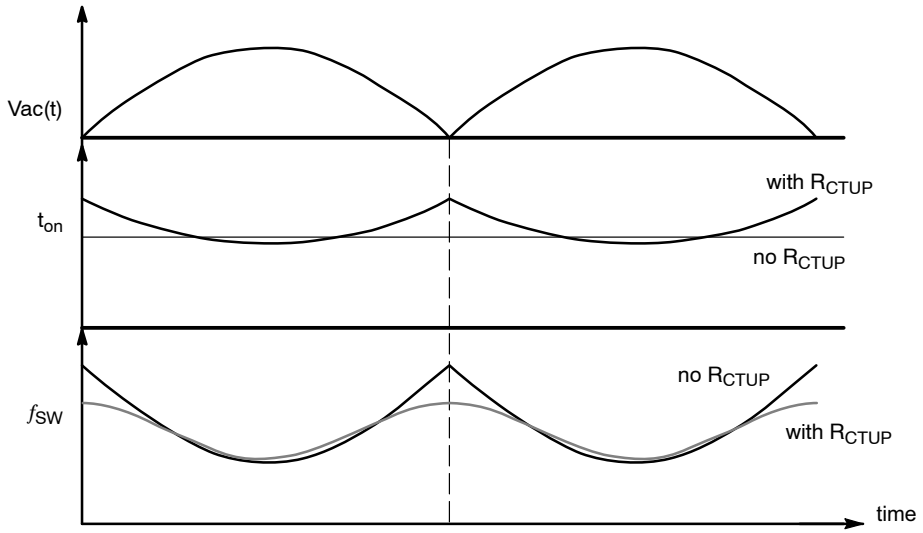

Figure 15. On Time and Switching Frequency With and Without R_{CTUP}

The dependency of THD on R_{CTUP} is illustrated in Figure 16.

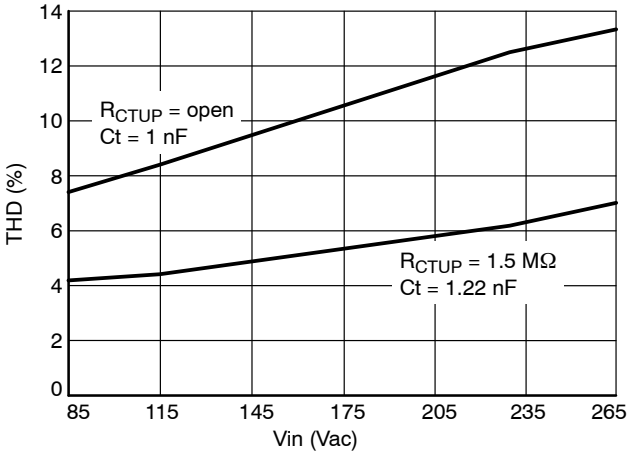

Figure 16. Dependency of THD on R_{CTUP} (I_{out} = 250 mA)

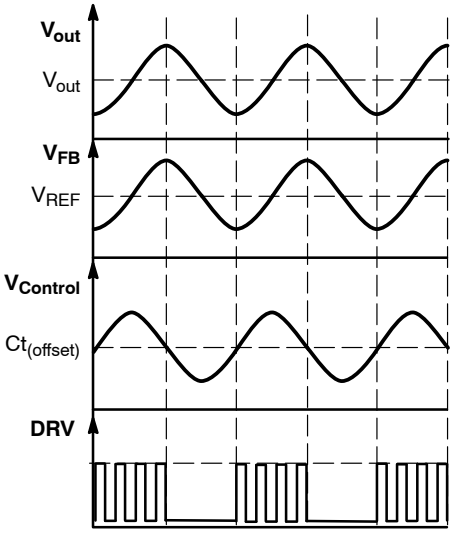

Figure 17. Required On Time Less Than the Minimum On Time

2. Improve the THD/PF at Maximum Input Voltage or Low Output Current:

If the required on time at maximum input voltage or low output current is less than the minimum on time (t_{PWM}), then DRV pulses must be skipped to prevent excessive power delivery to the output. This results in the following sequence:

1. The excessive on time causes $V_{Control}$ to decrease to $Ct_{(offset)}$.
2. When $V_{Control} < Ct_{(offset)}$, the drive is disabled.
3. The drive is disabled and V_{out} decreases.
4. As V_{out} decreases, $V_{Control}$ increases.
5. The sequence repeats. Figure 17 depicts the sequence:

This sequence increases the input current distortion. There are two solutions to improve THD/PF at maximum input voltage or low output current:

1. Properly size the Ct capacitor. As previously mentioned, the Ct capacitor is sized to set the maximum on time for minimum line input voltage and maximum output power. Sizing Ct to an excessively large value reduces the control range at Vac_{HL} or low output power.
2. Compensate for propagation delays. If optimizing the Ct capacitor does not achieve the desired performance, then it may be necessary to compensate for the PWM propagation delay by connecting a resistor (R_{CT}) in series with Ct. When the Ct voltage reaches the $V_{Control}$ setpoint, the PWM comparator sends a signal to end the on time of the driver as shown in Figure 18.

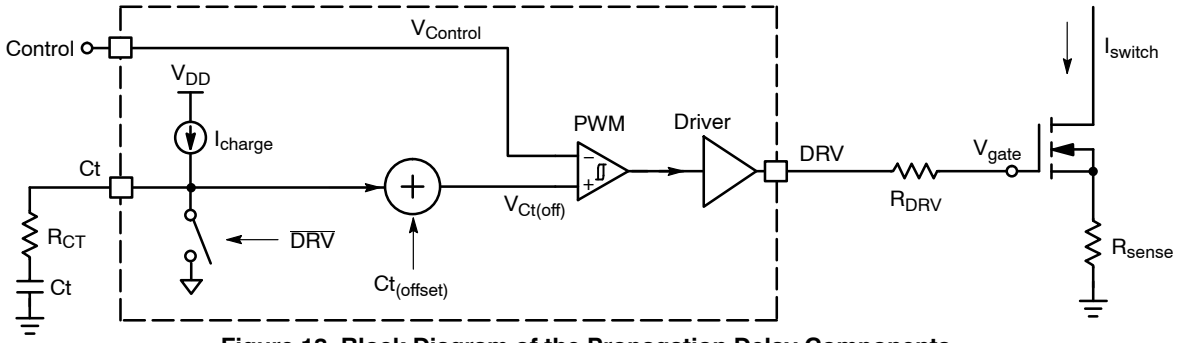

Figure 18. Block Diagram of the Propagation Delay Components

There is a delay (t_{delay}) from when $V_{Ct(off)}$ is reached to when the MOSFET completely turns off. t_{delay} is caused by the propagation delay of the PWM comparator (t_{PWM}) and the time for the gate voltage of the MOSFET to decrease to zero (t_{gate}). The delays are illustrated in Figure 19.

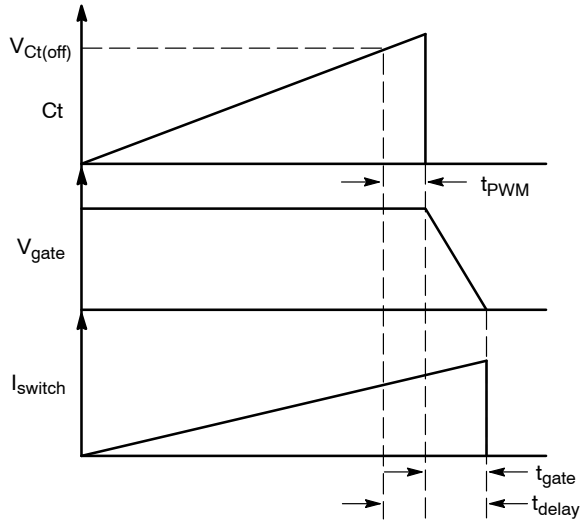

Figure 19. Turn Off Propagation Delays

The total delay is calculated using Equation 25:

$$t_{delay} = t_{PWM} + t_{gate} \qquad \text{(eq. 25)}$$

t_{delay} increases the effective on time of the MOSFET.

If a resistor (R_{CT}) is connected in series with the Ct capacitor, then the total on time reduction is calculated using Equation 26:

$$\Delta t_{on} = Ct \cdot \frac{\Delta V_{RCT}}{\Delta I_{RCT}} = Ct \cdot R_{CT} \qquad \text{(eq. 26)}$$

The value of R_{CT} to compensate for the propagation delay is calculated using Equation 27:

$$R_{CT} = \frac{t_{delay}}{Ct} \qquad \text{(eq. 27)}$$

The NCP1608 datasheet specifies the maximum t_{PWM} as 130 ns. t_{gate} is a dependent on the gate charge of the MOSFET and R_{DRV}. For this demo board, the gate delay is measured as 230 ns.

$$R_{CT} = \frac{360\ n}{1\ n} = 360\ \Omega$$

A value of R_{CT} = 365 Ω compensates for the propagation delays. Figure 20 shows the decrease of THD at Vac_{HL} and low output power by compensating for the propagation delay.

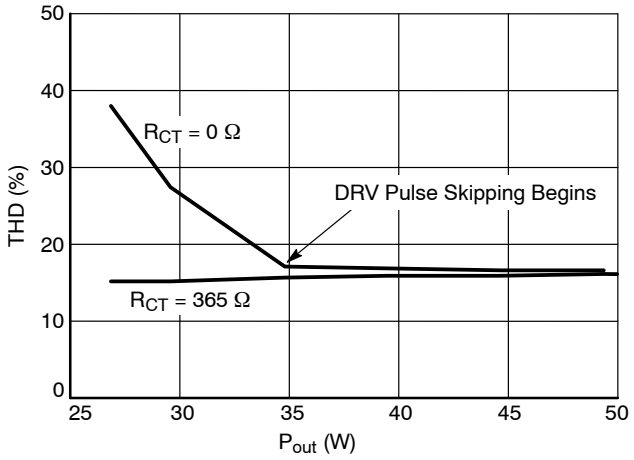

Figure 20. Low Output Power THD Reduction with R_{CT} (V_{in} = 265 Vac 50 Hz, R_{CTUP} = open, Ct = 1 nF)

Both THD reduction techniques can be combined to decrease the THD for the entire output power range. Figure 21 shows the decreased THD at the maximum input voltage across the output power range by decreasing zero crossing distortion and by compensating for the propagation delay.

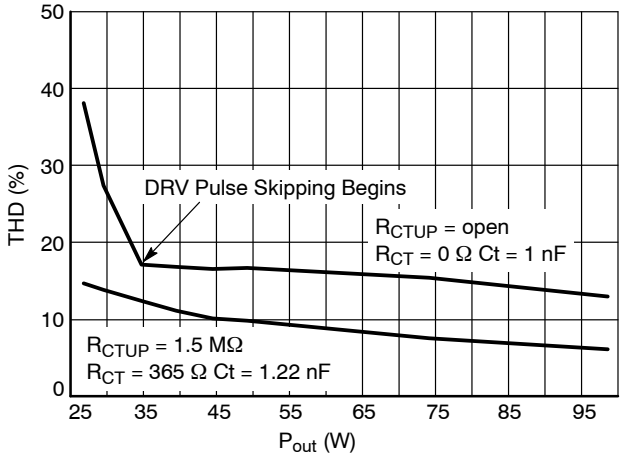

Figure 21. THD Reduction with R_{CTUP} and R_{CT} (V_{in} = 265 Vac 50 Hz)

Design Results

The completed demonstration board schematic is shown in Figure 22.

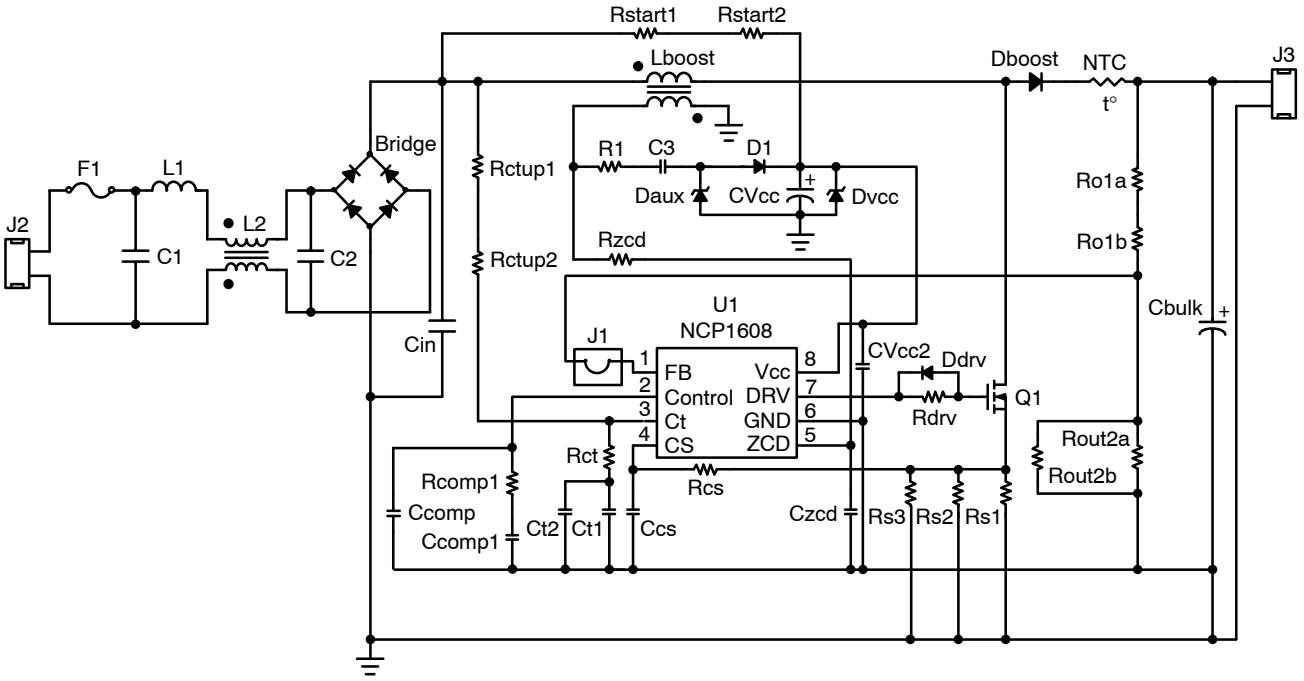

Figure 22. 100 W Pre−Converter Using the NCP1608

The bill of materials (BOM), layout, and summary of boost equations are shown in Appendix 1, Appendix 2, and Appendix 3 respectively. This pre−converter exhibits excellent THD (Figure 23 and Figure 24), PF (Figure 25), and efficiency (Figure 26). All measurements are performed with the following conditions:

− After the board is operated at full load and minimum line input voltage for 30 minutes

− At an ambient temperature of 25°C, open frame, and without forced air flow

− The input power, PF, and THD are measured using a PM3000A power meter

− The output voltage is measured using a HP34401A multimeter

− The output current is set using a PLZ1003WH electronic load

− The output current is measured using a HP34401A multimeter

− The output power is calculated by multiplying the output voltage and output current

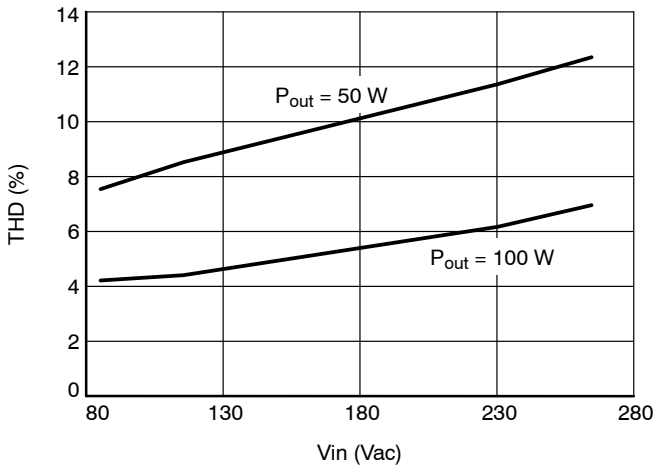

Figure 23. THD vs. Input Voltage

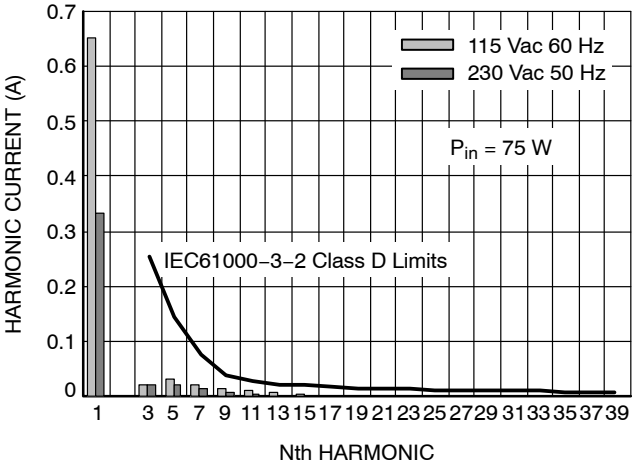

Figure 24. Individual Harmonic Current

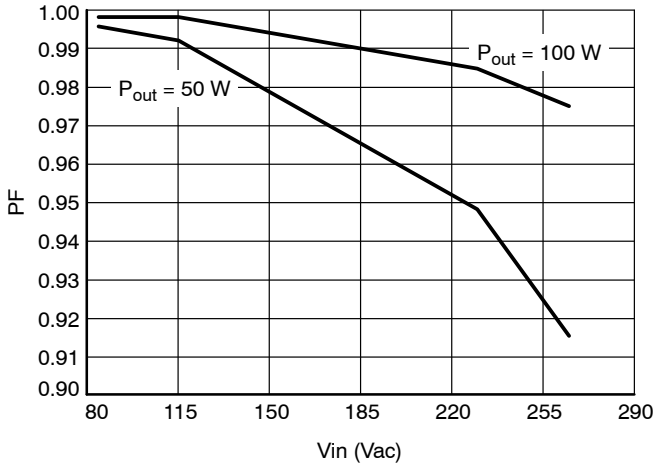

Figure 25. PF vs. Input Voltage

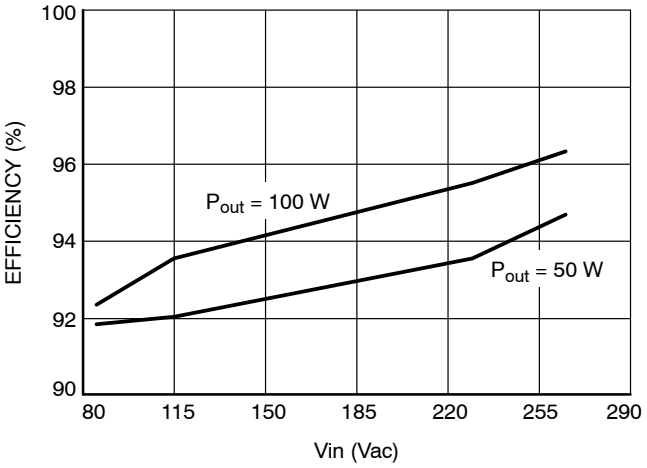

Figure 26. Efficiency vs. Input Voltage

Input Current and Output Voltage

The input current and output voltage ripple are shown in Figure 27. The overvoltage protection is observed by starting up the pre-converter with no load as shown in Figure 28. The NCP1608 detects an OVP fault when V_{out} reaches 421 V and restarts when V_{out} decreases to 410 V.

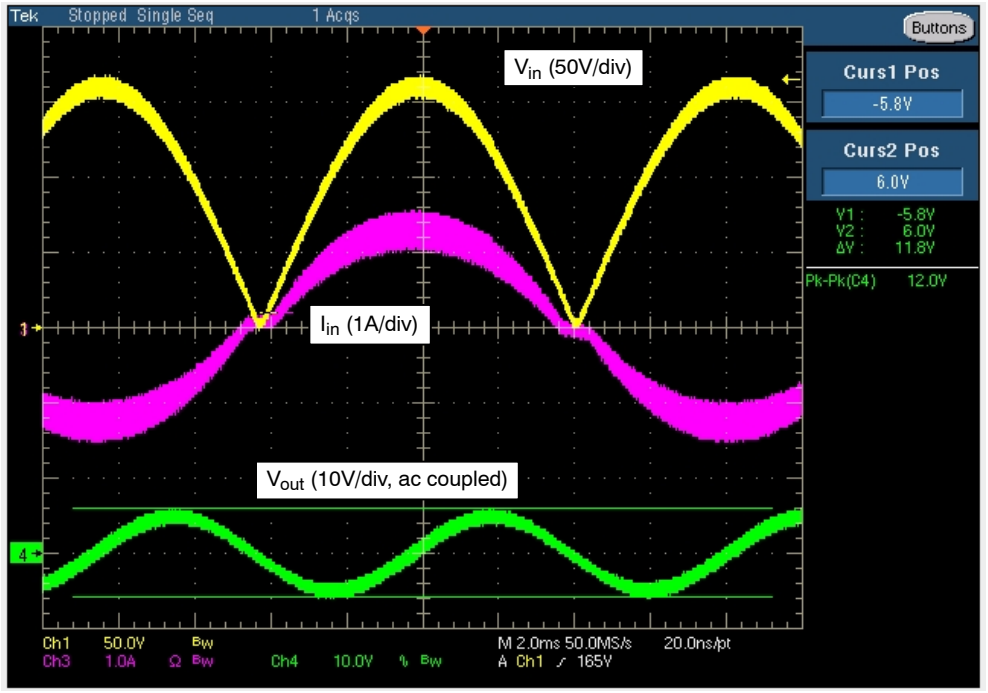

Figure 27. Input Current and Output Voltage Ripple (V_{in} = 115 Vac 60 Hz, I_{out} = 250 mA)

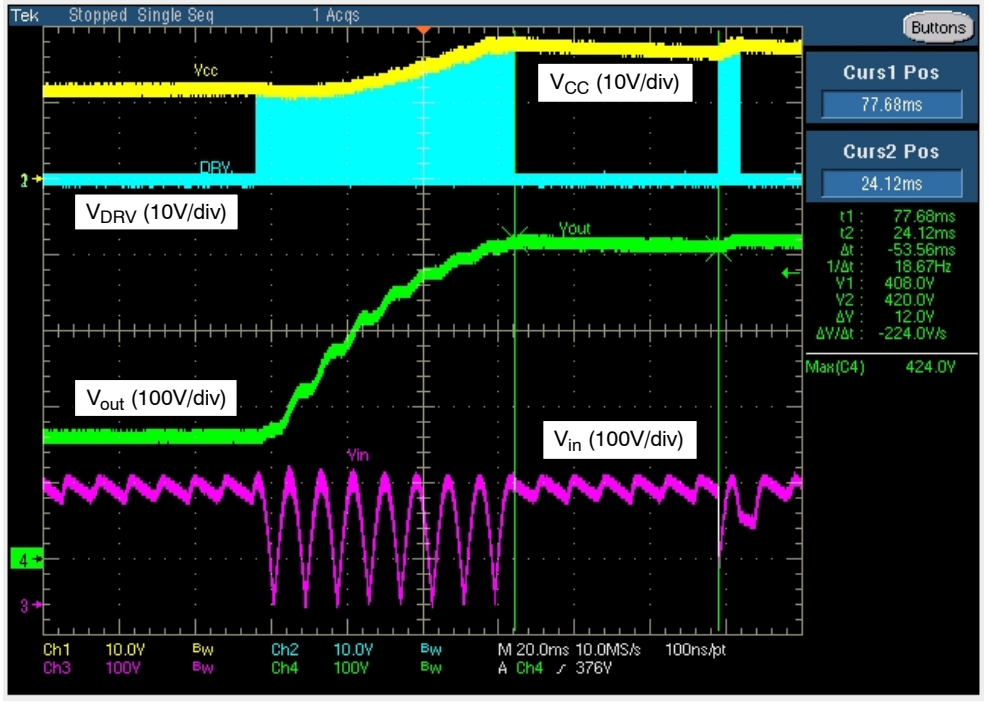

Figure 28. Startup Transient Showing OVP Detection and Recovery (V_{in} = 115 Vac 60 Hz, I_{out} = 0 mA)

Frequency Response

The frequency response is measured at the minimum and maximum input voltages and maximum output power. Figure 29 shows that at minimum input voltage, the crossover frequency is 2 Hz and the phase margin is 71°. Figure 30 shows that at maximum input voltage, the crossover frequency is 10 Hz and the phase margin is 53°.

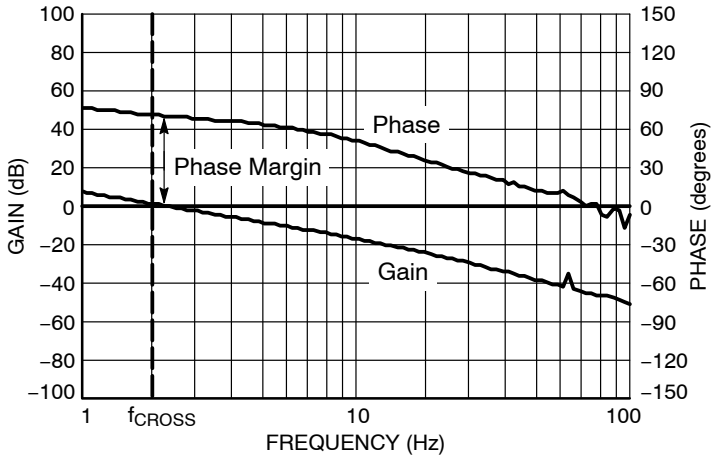

Figure 29. Frequency Response V_{in} = 85 Vac 60 Hz I_{out} = 250 mA

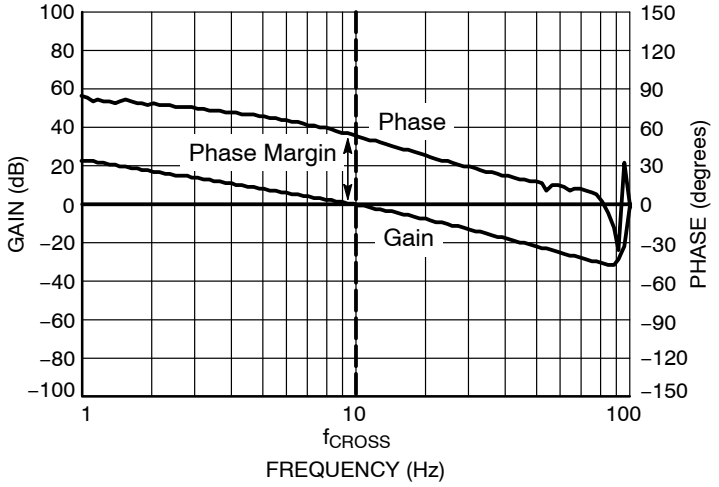

Figure 30. Frequency Response V_{in} = 265 Vac 50 Hz I_{out} = 250 mA

Floating Pin Protection (FPP) Jumper

The demonstration board includes a jumper (J1) between the FB pin and the feedback network to demonstrate the FPP feature of the NCP1608. If J1 is removed before applying the line input voltage, the drive is never enabled as shown in Figure 31. If J1 is removed during operation, the drive is disabled as shown in Figure 32. J1 is for FPP demonstration purposes only and should not be included in manufactured systems.

Figure 31. Startup with Jumper Removed (V_{in} = 265 Vac 50 Hz, I_{out} = 0 mA)

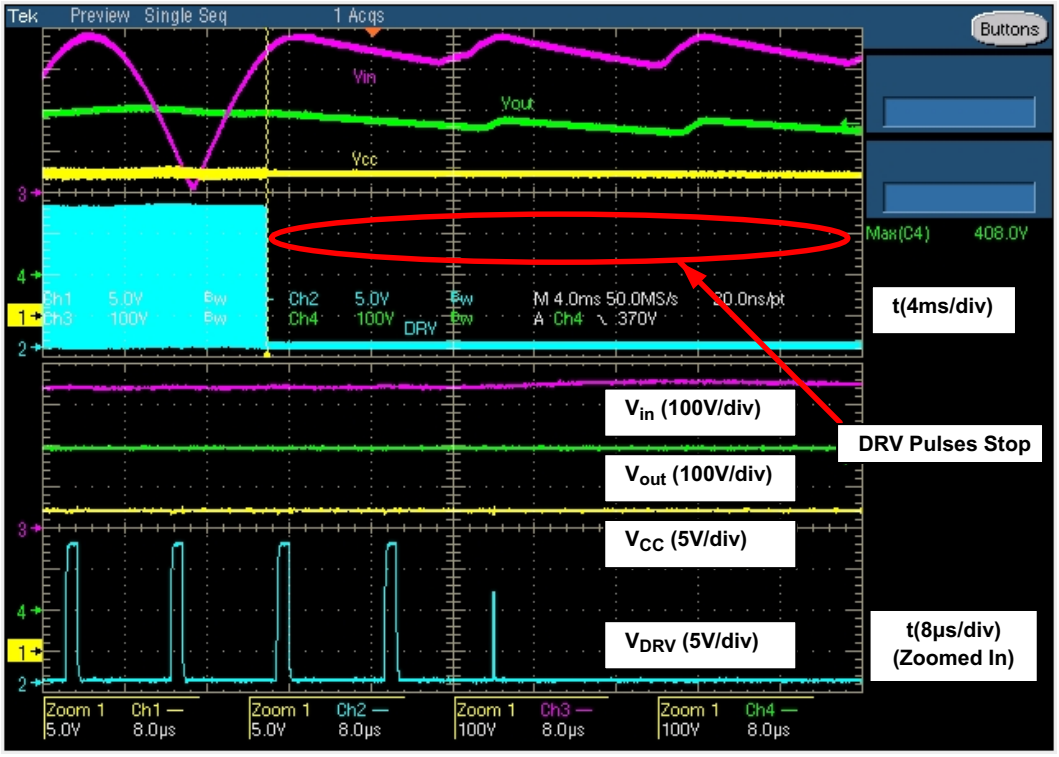

Figure 32. Removing the Jumper During Operation (V_{in} = 265 Vac 50 Hz, I_{out} = 250 mA)

The demonstration board can be configured for THD reduction or power dissipation reduction. Table 3 shows the configuration results.

Table 3. DEMONSTRATION BOARD CONFIGURATION RESULTS

R_{CTUP}	Ct (R_{CT} = 0 Ω)	Shutdown Power Dissipation (V_{FB} = 0 V) (V_{in} = 265 Vac 50 Hz)	Efficiency (P_{out} = 100 W)		THD (P_{out} = 100 W)	
			115 Vac 60 Hz	230 Vac 50 Hz	115 Vac 60 Hz	230 Vac 50 Hz
open	1 nF	224 mW	93.5%	95.7%	8.4%	12.5%
1.5 MΩ	1.22 nF	294 mW	93.5%	95.5%	4.4%	6.2%

Safety Precautions

Since the FPP feature is only intended to protect the system in the case of a floating FB pin, care must be taken when removing the jumper. **Do not attach any wires to the jumper pins with the jumper removed.** Connecting wires to the FB pin couples excessive noise to the FB pin. This prevents the correct operation of FPP and causes maximum power to be delivered to the output. This can cause excessive voltage to be applied to C_{bulk}. **Always wear proper eye protection when the jumper is removed.**

The jumper is located next to high voltage components. Do not remove the jumper during operation with bare fingers or non-insulated metal tools.

Layout Considerations

Careful consideration must be given to the placement of components during layout of switching power supplies. Noise generated by the large voltages and currents can be coupled to the pins of the NCP1608. The following guidelines reduce the probability of excessive coupling:

1. Place the following components as close as possible to the NCP1608:
   a. Ct capacitor
   b. V_{CC} decoupling capacitor
   c. Control pin compensation components
2. Minimize trace length, especially for high current loops.
3. Use wide traces for high current connections.
4. Use a single point ground connection between power ground and signal ground.

The demonstration board includes the following unpopulated footprints to enable user experimentation:

1. CCS to add a decoupling capacitor to the CS pin.
2. CZCD to add a decoupling capacitor to the ZCD pin.
3. DDRV to add a diode for faster turn off of Q1.
4. DVCC to add a diode to clamp V_{CC}.
5. ROUT2B to add a resistor for a more accurate output voltage.
6. RS3 to add a resistor for a more accurate inductor peak current limit or to reduce the heating of the current sense resistors.

Summary

A universal input voltage 100 W converter is designed using the boost topology. The converter is implemented with the NCP1608. Over the input voltage range and with an output power of 100 W, the PF, THD, and efficiency are measured as greater than 0.97, less than 8%, and greater than 92% respectively. The converter complies with IEC61000−3−2 Class D limits for an input power of 75 W. The converter is stable over the input voltage range with a measured phase margin greater than 50 degrees. Finally, the overvoltage protection and floating pin protection features protect the converter from excessive output voltage.

The demonstration board is designed to showcase the features and flexibility of the NCP1608. This design is a guideline only and does not guarantee performance for any manufacturing or production purposes.

Appendix 1: BILL OF MATERIALS (BOM)*

Designator	Qty	Description	Value	Tolerance	Manufacturer	Manufacturer Part Number
BRIDGE	1	Bridge Rectifier, 4 A, 600 V	–	–	Vishay	KBL06−E4/51
C1, C2	2	Capacitor, EMI Suppression, 305 Vac	0.47 μF	20%	EPCOS	B32923C3474M
C3	1	Capacitor, Ceramic, SMD, 50 V	8.2 nF	5%	TDK Corporation	C3216C0G1H822J
CBULK	1	Capacitor, Electrolytic, 450 V	68 μF	20%	United Chemi−Con	EKXG451ELL680MMN3S
CCOMP	1	Capacitor, Ceramic, SMD, 25 V	0.68 μF	10%	TDK Corporation	C3216X7R1E684K
CCOMP1	1	Capacitor, Ceramic, SMD, 25 V	3.3 μF	10%	TDK Corporation	C3216X7R1E335K
CCS, CZCD	2	Capacitor, Ceramic, SMD	open	–	–	–
CIN	1	Capacitor, EMI Suppression, 305 Vac	0.1 μF	20%	EPCOS	B32921A2104M
CT1	1	Capacitor, Ceramic, SMD, 50 V	1 nF	10%	Yageo	CC1206KRX7R9BB102
CT2	1	Capacitor, Ceramic, SMD, 50 V	220 pF	10%	Yageo	CC1206KRX7R9BB221
CVCC	1	Capacitor, Electrolytic, 25 V	47 μF	20%	Panasonic	EEU−FC1E470
CVCC2	1	Capacitor, Ceramic, SMD, 50 V	0.1 μF	10%	Yageo	CC1206KRX7R9BB104
D1	1	Diode, Switching, 100 V	–	–	ON Semiconductor	MMSD4148T1G
DAUX	1	Diode, Zener, 18 V	–	–	ON Semiconductor	MMSZ4705T1G
DBOOST	1	Diode, Ultrafast, 4 A, 600 V	–	–	ON Semiconductor	MUR460RLG
DDRV	1	Diode, Switching	open	–	–	–
DVCC	1	Diode, Zener	open	–	–	–
F1	1	Fuse, SMD, 2 A, 600 V	–	–	Littelfuse	0461002.ER
J1	1	Header 1 Row of 2, 100 mil	–	–	3M	929400−01−36−RK
J2, J3	2	Connector, 156 mil 3 pin	–	–	MOLEX	26−60−4030
L1	1	Inductor, Radial, 4 A	180 μH	10%	Coilcraft	PCV−2−184−05L
L2	1	Line Filter, 2.7 A	4.7 mH	–	Panasonic	ELF−20N027A
LBOOST	1	Inductor, 400 μH, N_B:N_{ZCD} = 10:1	–	–	Coilcraft	JA4224−AL
MECHANICAL	1	Shorting Jumper	–	–	3M	929955−06
MECHANICAL	1	Heatsink	–	–	Aavid	590302B03600
MECHANICAL	1	Screw, Phillips, 4−40, 1/4″, Steel	–	–	Building Fasteners	PMSSS 440 0025 PH
MECHANICAL	1	Nut, Hex 4−40, Steel	–	–	Building Fasteners	HNSS440
MECHANICAL	1	Shoulder Washer #4, Nylon	–	–	Keystone	3049
MECHANICAL	1	TO−220 Thermal Pad, 9 mil	–	–	Wakefield	173−9−240P
MECHANICAL	4	Standoffs, Hex 4−40, 0.75″, Nylon	–	–	Keystone	4804K
MECHANICAL	4	Nut, Hex 4−40, Nylon	–	–	Building Fasteners	NY HN 440
NTC	1	Thermistor, Inrush Current Limiter	4.7 Ω	20%	EPCOS	B57238S479M
Q1	1	MOSFET, N−Channel, 11.6 A, 560 V	–	–	Infineon	SPP12N50C3
R1	1	Resistor, SMD	100 Ω	1%	Vishay	CRCW1206100RFKEA
RCOMP1	1	Resistor, SMD	20 kΩ	1%	Vishay	CRCW120620K0FKEA
RCS	1	Resistor, 0.25 W Axial	510 Ω	5%	Yageo	CFR−25JB−510R
RCT	1	Resistor, SMD	0 Ω	–	Vishay	CRCW12060000Z0EA
RCTUP1, RCTUP2	2	Resistor, 0.25 W Axial	750 kΩ	5%	Yageo	CFR−25JB−750K
RDRV	1	Resistor, SMD	10 Ω	1%	Vishay	CRCW120610R0FKEA
RO1A, RO1B	2	Resistor, SMD	2 MΩ	1%	Vishay	CRCW12062M00FKEA
ROUT2A	1	Resistor, SMD	25.5 kΩ	1%	Vishay	CRCW120625K5FKEA
ROUT2B	1	Resistor, SMD	open	–	–	–
RS1, RS2	2	Resistor, SMD, 1 W	0.25 Ω	1%	Vishay	WSL2512R2500FEA
RS3	1	Resistor, SMD	open	–	–	–
RSTART1, RSTART2	2	Resistor, 0.25 W Axial	330 kΩ	5%	Yageo	CFR−25JB−330K
RZCD	1	Resistor, 0.25 W Axial	100 kΩ	5%	Yageo	CFR−25JB−100K
U1	1	CrM PFC Controller	NCP1608	–	ON Semiconductor	NCP1608BDR2G

*All products listed are Pb−Free.

Appendix 2: LAYOUT

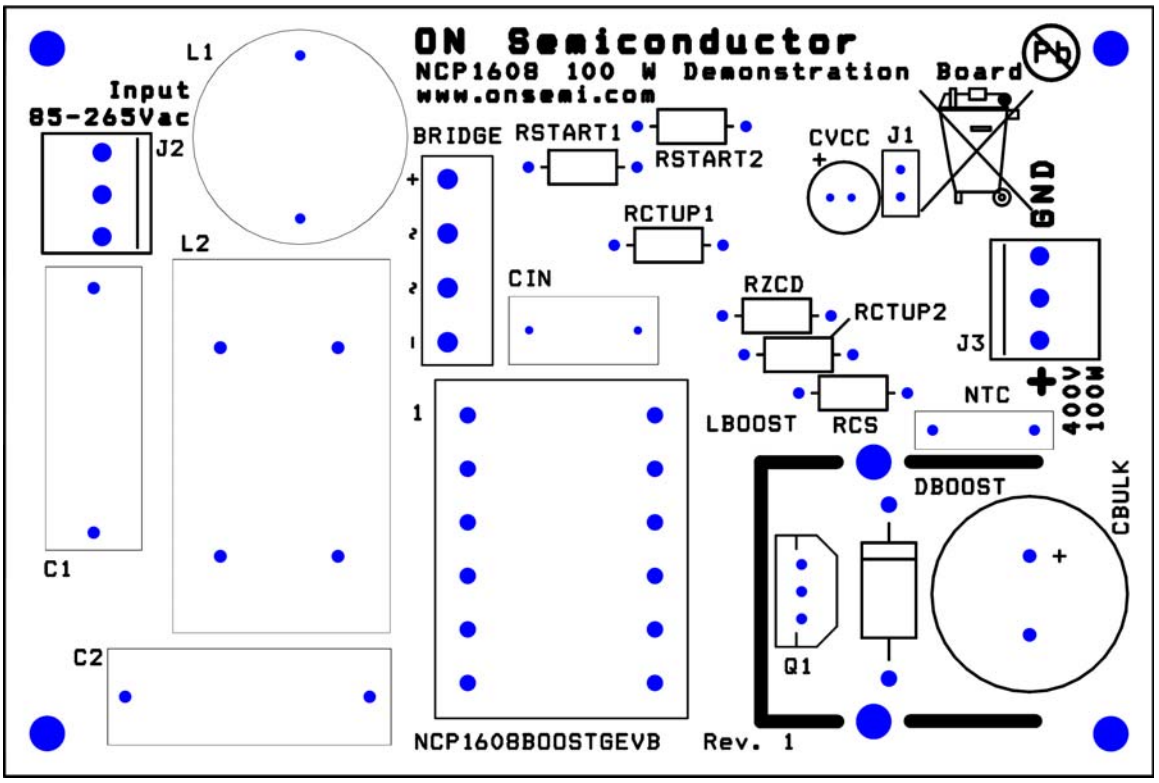

Figure 33. Top View of the Layout

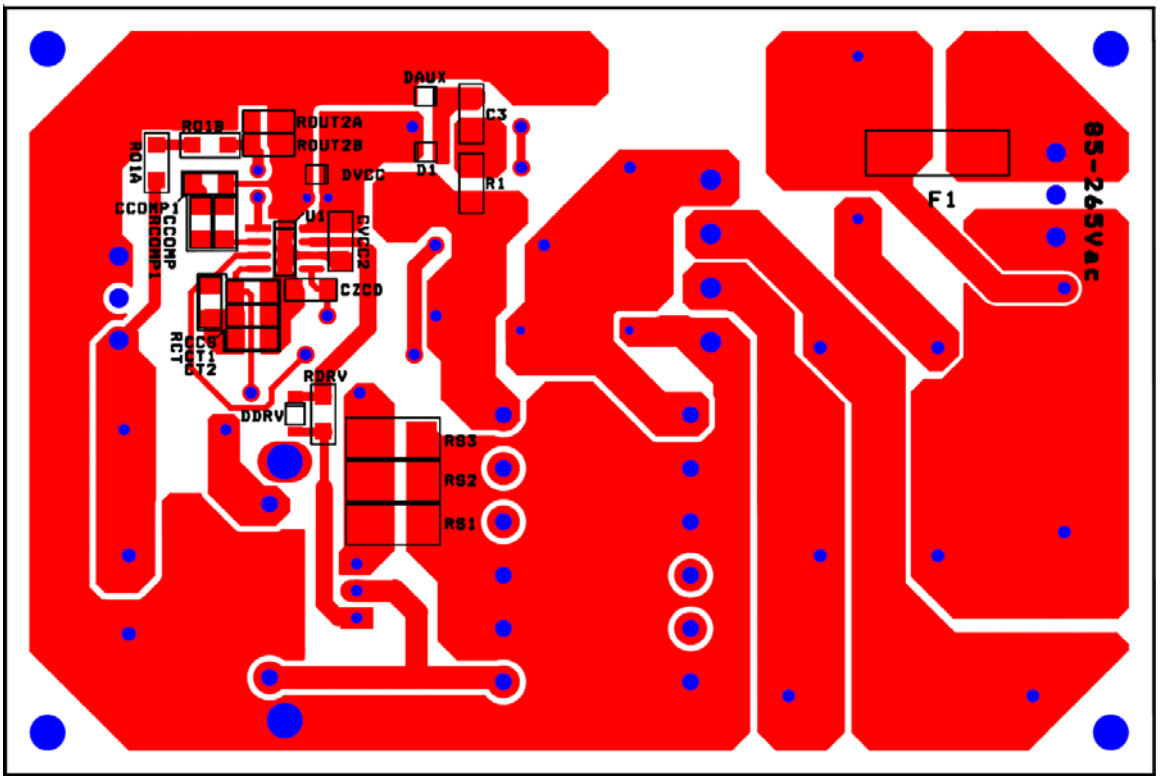

Figure 34. Bottom View of the Layout

Appendix 3: SUMMARY OF BOOST EQUATIONS Components are identified in Figure 3

Input rms Current	$Iac = \frac{P_{out}}{\eta \cdot Vac}$	η (the efficiency of only the PFC stage) is generally in the range of 90 – 95%. Vac is the rms ac line input voltage.
Inductor Peak Current	$I_{L(peak)} = \frac{\sqrt{2} \cdot 2 \cdot P_{out}}{\eta \cdot Vac}$	The maximum inductor peak current occurs at the minimum line input voltage and maximum output power.
Inductor Value	$L \le \frac{Vac^2 \cdot \left(\frac{V_{out}}{\sqrt{2}} - Vac\right) \cdot \eta}{\sqrt{2} \cdot V_{out} \cdot P_{out} \cdot f_{SW(MIN)}}$	$f_{SW(MIN)}$ is the minimum desired switching frequency. The maximum L is calculated at both the minimum line input voltage and maximum line input voltage.
On Time	$t_{on} = \frac{2 \cdot L \cdot P_{out}}{\eta \cdot Vac^2}$	The maximum on time occurs at the minimum line input voltage and maximum output power.
Off Time	$t_{off} = \frac{t_{on}}{\frac{V_{out}}{Vac \cdot \lvert\sin\theta\rvert \cdot \sqrt{2}}} - 1$	The off time is a maximum at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.
Switching Frequency	$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L \cdot P_{out}} \cdot \left(1 - \frac{Vac \cdot \lvert\sin\theta\rvert \cdot \sqrt{2}}{V_{out}}\right)$	
On Time Capacitor	$Ct \ge \frac{2 \cdot P_{out} \cdot L_{MAX} \cdot I_{charge}}{\eta \cdot Vac_{LL}^2 \cdot V_{Ct(MAX)}}$	Where Vac_{LL} is the minimum line input voltage and L_{MAX} is the maximum inductor value. I_{charge} and $V_{Ct(MAX)}$ are shown in the specification table.
Inductor Turns to ZCD Turns Ratio	$N_B : N_{ZCD} \le \frac{V_{out} - \left(\sqrt{2} \cdot Vac_{HL}\right)}{V_{ZCD(ARM)}}$	Where Vac_{HL} is the maximum line input voltage. $V_{ZCD(ARM)}$ is shown in the specification table.
Resistor from ZCD Winding to the ZCD pin	$R_{ZCD} \ge \frac{\sqrt{2} \cdot Vac_{HL}}{I_{ZCD(MAX)} \cdot (N_B : N_{ZCD})}$	Where $I_{ZCD(MAX)}$ is maximum rated current for the ZCD pin (10 mA).
Output Voltage and Output Divider	$V_{out} = V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right)$ $R_{out1} = \frac{V_{out}}{I_{bias(out)}}$ $R_{out2} = \frac{R_{out1} \cdot R_{FB}}{R_{FB} \cdot \left(\frac{V_{out}}{V_{REF}} - 1\right) - R_{out1}}$	Where V_{REF} is the internal reference voltage and R_{FB} is the pull–down resistor used for FPP. V_{REF} and R_{FB} are shown in the specification table. $I_{bias(out)}$ is the bias current of the output voltage divider.
Output Voltage OVP Detection and Recovery	$V_{out(OVP)} = \frac{V_{OVP}}{V_{REF}} \cdot V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right)$ $V_{out(OVPL)} = \left(\left(\frac{V_{OVP}}{V_{REF}} \cdot V_{REF}\right) - V_{OVP(HYS)}\right) \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right)$	V_{OVP}/V_{REF} and $V_{OVP(HYS)}$ are shown in the specification table.
Output Voltage Ripple and Output Capacitor Value	$V_{ripple(peak-peak)} < 2 \cdot \left(V_{out(OVP)} - V_{out}\right)$ $C_{bulk} \ge \frac{P_{out}}{2 \cdot \pi \cdot V_{ripple(peak-peak)} \cdot f_{line} \cdot V_{out}}$	Where f_{line} is the ac line frequency and $V_{ripple(peak-peak)}$ is the peak–to–peak output voltage ripple. Use f_{line} = 47 Hz for universal input worst case.
Output Capacitor rms Current	$I_{C(RMS)} = \sqrt{\frac{\sqrt{2} \cdot 32 \cdot P_{out}^2}{9 \cdot \pi \cdot Vac \cdot V_{out} \cdot \eta^2} - I_{load(RMS)}^2}$	Where $I_{load(RMS)}$ is the rms load current.

Appendix 3: SUMMARY OF BOOST EQUATIONS Components are identified in Figure 3 (Continued)

Output Voltage UVP Detection	$V_{out(UVP)} = V_{UVP} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1 \right)$	V_{UVP} is shown in the specification table.
Inductor rms Current	$I_{L(RMS)} = \frac{2 \cdot P_{out}}{\sqrt{3} \cdot Vac \cdot \eta}$	
Output Diode rms Current	$I_{D(RMS)} = \frac{4}{3} \cdot \sqrt{\frac{\sqrt{2} \cdot 2}{\pi}} \cdot \frac{P_{out}}{\eta \cdot \sqrt{Vac \cdot V_{out}}}$	
MOSFET rms Current	$I_{M(RMS)} = \frac{2}{\sqrt{3}} \cdot \left(\frac{P_{out}}{\eta \cdot Vac} \right) \cdot \sqrt{1 - \left(\frac{\sqrt{2} \cdot 8 \cdot Vac}{3 \cdot \pi \cdot V_{out}} \right)}$	
Current Sense Resistor	$R_{sense} = \frac{V_{ILIM}}{I_{L(peak)}}$ $P_{R_{sense}} = I_{M(RMS)}^{2} \cdot R_{sense}$	V_{ILIM} is shown in the specification table.
Type 1 Compensation	$C_{COMP} = \frac{gm}{2 \cdot \pi \cdot f_{CROSS}}$	Where f_{CROSS} is the crossover frequency and is typically less than 20 Hz. gm is shown in the specification table.

The products described herein (NCP1608) may be covered by one or more of the following U.S. patents: 6,362,067, 5,359,281, 5,073,850. There may be other patents pending.

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