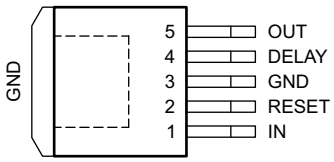
5-V LOW-DROPOUT VOLTAGE REGULATOR

Check for Samples: TLE4275-Q1

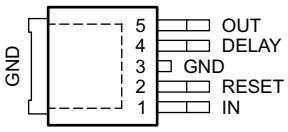
FEATURES

- **Qualified for Automotive Applications**
- **Output Voltage 5 V ± 2%**
- **Very Low Current Consumption**
- **Power-On and Undervoltage Reset**
- **Reset Low-Level Output Voltage < 1 V**
- **Very Low Dropout Voltage**
- **Short-Circuit Proof**
- **Reverse-Polarity Proof**

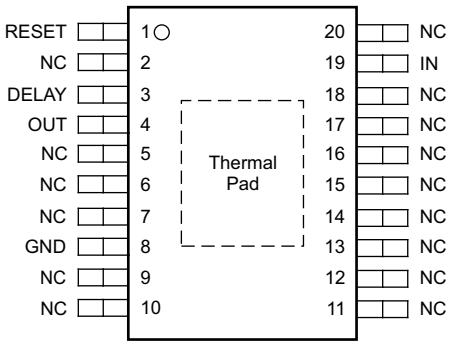
KTT (TO-263-5) Package
(Top View)



KVU (TO-252-5) Package
(Top View)



PWP (HTSSOP) Package
(Top View)



DESCRIPTION

The TLE4275 is a monolithic integrated low-dropout voltage regulator offered in a 5-pin TO package. The device regulates an input voltage up to 45 V to V_{OUT} = 5 V (typ). The device can drive loads up to 450 mA and is short-circuit proof. At overtemperature, the incorporated temperature protection turns off the TLE4275. The device generates a reset signal for an output voltage, $V_{OUT,rt}$, of 4.65 V (typ). By the use of an external delay capacitor, one can program the reset delay time.

The input capacitor, C_{IN}, compensates for line fluctuation. Using a resistor of approximately 1 Ω in series with C_{IN} dampens the oscillation of input inductance and input capacitance. The output capacitor, C_{OUT}, stabilizes the regulation circuit. The specification for stability is at C_{OUT} ≥ 22 µF and ESR ≤ 5 Ω, within the operating temperature range. Stability for electrolytic capacitors specifically is at C_{OUT} ≥ 68 µF within the operating temperature range. See the application report on low-temperature stability, SLVA501, for further details.

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The device also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

ORDERING INFORMATION

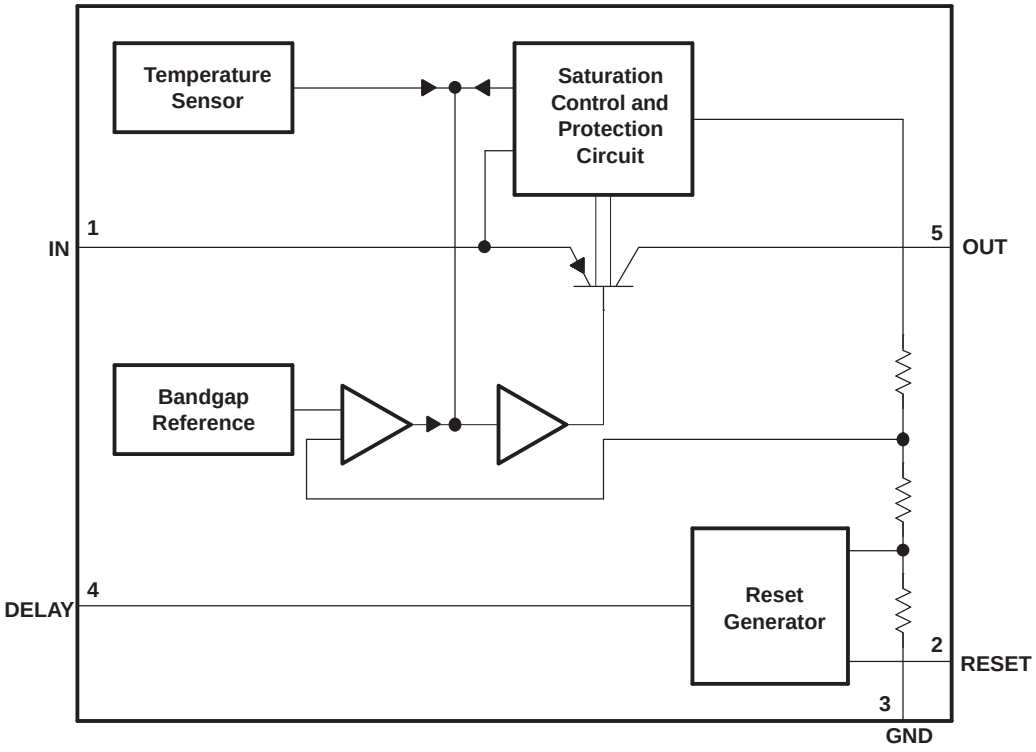
For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN FUNCTIONS

NAME	NO.			DESCRIPTION
	KTT	KVU	PWP	
DELAY	4	4	3	Reset delay. Connect to ground with a capacitor to set delay time.
GND	3	3	8	Ground. Internally connected to heatsink
IN	1	1	19	Input. Connect to ground as close to device as possible, through a ceramic capacitor.
NC	–	–	2, 5–7, 9–18, 20	Not connected
OUT	5	5	4	Output. Connect to ground with ≥ 22-µF capacitor, ESR < 5 Ω at 10 kHz.
RESET	2	2	1	Reset output. Open-collector output

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range(2)	IN	–42	45	V
		DELAY	–0.3	7	
V_O	Output voltage range	OUT	–1	16	V
		RESET	–0.3	25	
I_I	Input current	DELAY		±2	mA
I_O	Output current	RESET		±5	mA
T_J	Operating junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C
ESD	Electrostatic discharge rating	Human-body model (HBM)(3)		6000	V
		Machine model (MM)(4)		400	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) HBM ESD rating tested per JESD22-A114.
(4) MM ESD rating tested per JESD22-A115.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage	5.5	42	V
T_J	Junction temperature	–40	150	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TLE4275-Q1			UNIT
		KTT	KVU	PWP	
		5 PINS	5 PINS	20 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	28.8	40.3	39.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	43.1	31.8	22.7	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	0.8	17.2	19.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	3.7	2.8	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	0.7	17.1	18.9	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.2	0.7	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, T_J = −40°C to 150°C (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	I_O = 5 mA to 400 mA, V_I = 6 V to 28 V		4.9	5	5.1	V
		I_O = 5 mA to 200 mA, V_I = 6 V to 40 V		4.9	5	5.1	
I_O	Output current limit			450	700	950	mA
I_q	Current consumption $I_q = I_I - I_O$	I_O = 1 mA	T_J = 25°C		150	200	µA
			$T_J \le$ 85°C		150	220	
		I_O = 250 mA			5	10	mA
		I_O = 400 mA			12	22	
V_{DO}	Dropout voltage(1)	I_O = 300 mA, $V_{do} = V_I - V_O$			250	500	mV
	Load regulation	I_O = 5 mA to 400 mA			15	30	mV
	Line regulation	ΔV_I = 8 V to 32 V, I_O = 5 mA		–15	5	15	mV
PSRR	Power-supply ripple rejection	f_r = 100 Hz, V_r = 0.5 V_{pp}			60		dB
$\frac{\Delta V_O}{\Delta T}$	Temperature output-voltage drift				0.5		mV/K
$V_{O,rt}$	RESET switching threshold			4.5	4.65	4.8	V
V_{ROL}	RESET output low voltage	$R_{ext} \ge$ 5 kΩ, V_O > 1 V			0.2	0.4	V
I_{ROH}	RESET output leakage current	V_{ROH} = 5 V			0	10	µA
$I_{D,c}$	RESET charging current	V_D = 1 V		3	5.5	9	µA
V_{DU}	RESET upper timing threshold			1.5	1.8	2.2	V
V_{DRL}	RESET lower timing threshold			0.2	0.4	0.7	V

(1) Measured when the output voltage V_O has dropped 100 mV from the nominal value obtained at V_I = 13.5 V

SWITCHING CHARACTERISTICS

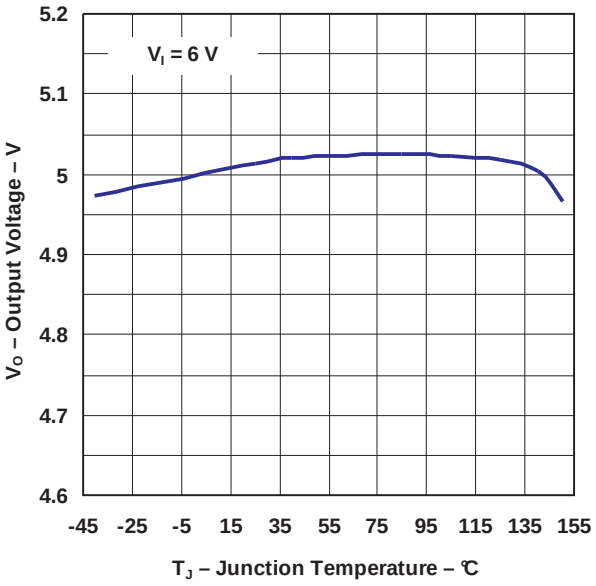
over operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rd}	RESET delay time	C_D = 47 nF	10	16	22	ms
t_{rr}	RESET reaction time	C_D = 47 nF		0.5	2	µs

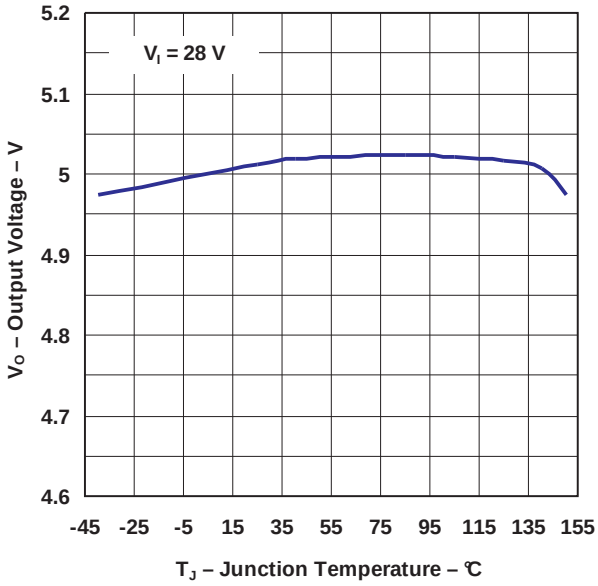
TYPICAL CHARACTERISTICS

At T_A = 25ºC

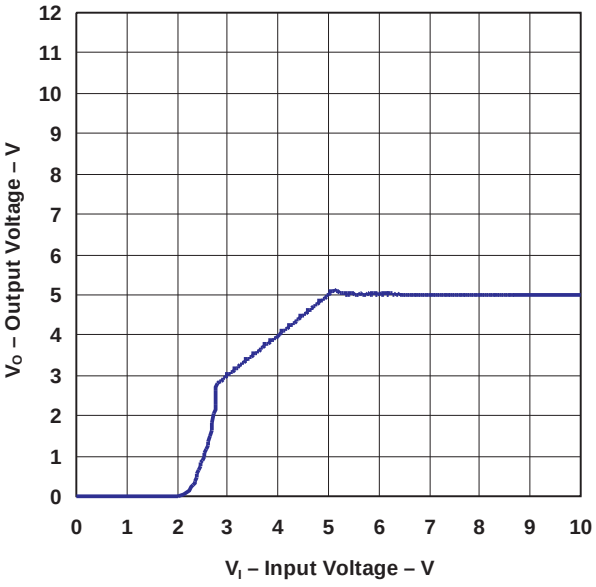
OUTPUT VOLTAGE versuss JUNCTION TEMPERATURE



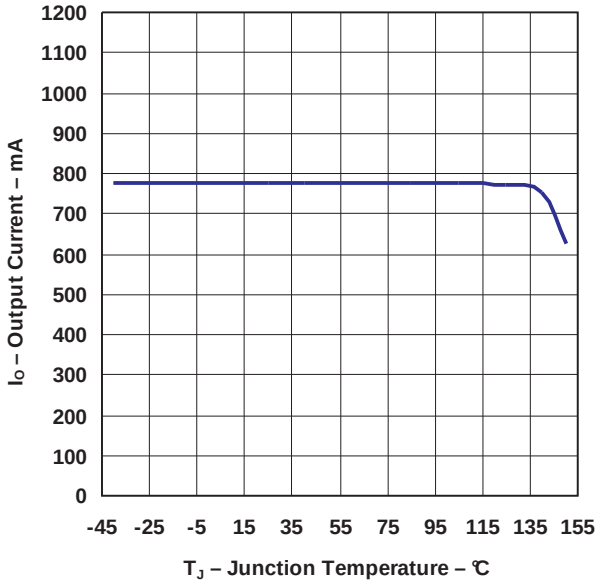
OUTPUT VOLTAGE versus JUNCTION TEMPERATURE



OUTPUT VOLTAGE versus INPUT VOLTAGE



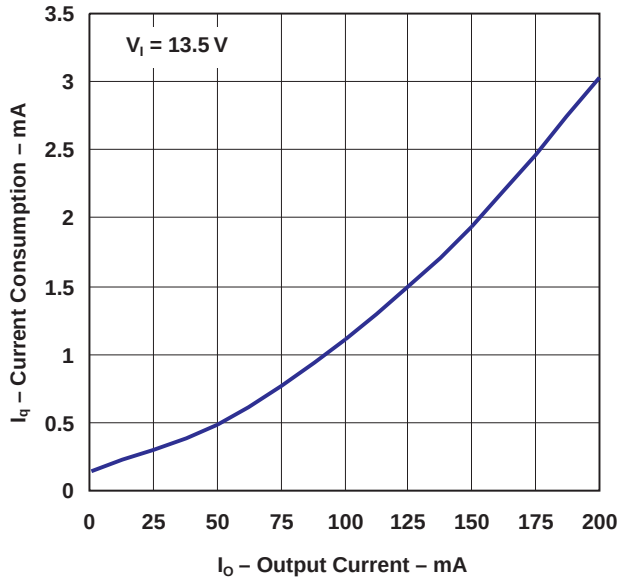
OUTPUT CURRENT versus JUNCTION TEMPERATURE



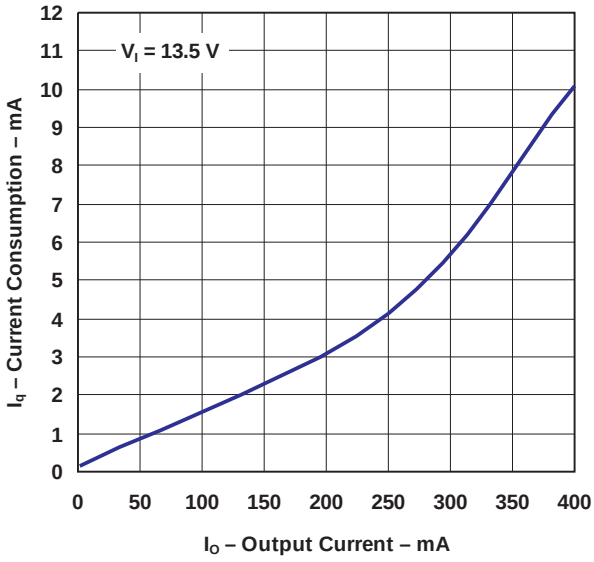
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C

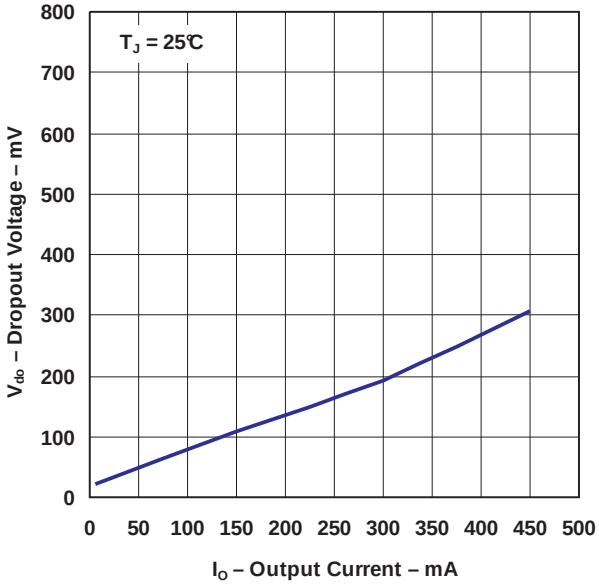
CURRENT CONSUMPTION versus OUTPUT CURRENT



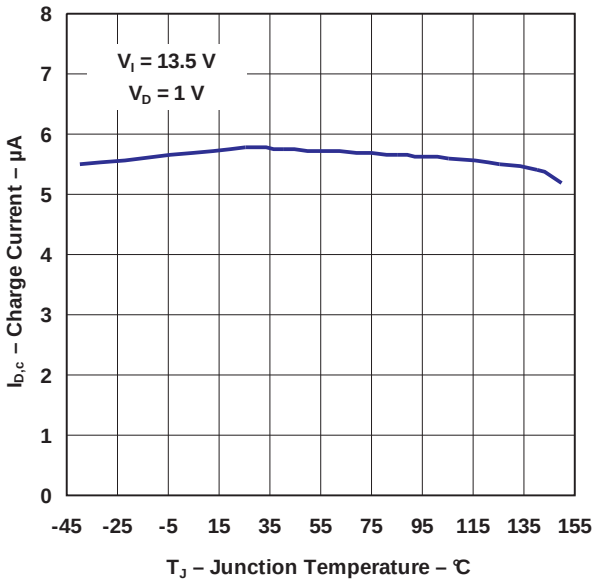
CURRENT CONSUMPTION versus OUTPUT CURRENT



DROPOUT VOLTAGE versus OUTPUT CURRENT



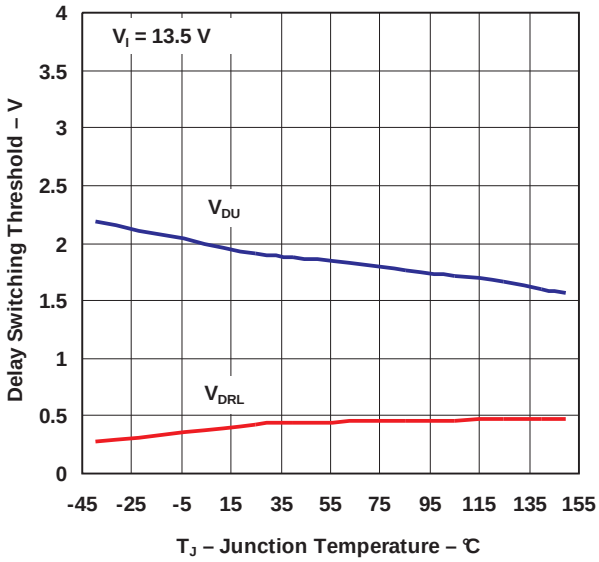
CHARGE CURRENT versus JUNCTION TEMPERATURE



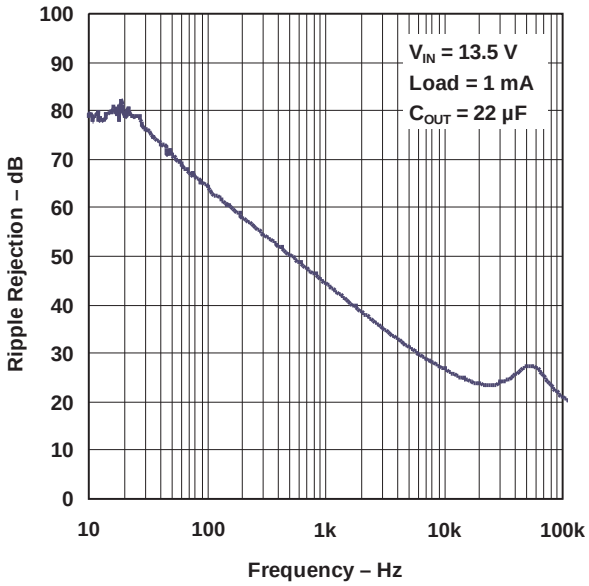
TYPICAL CHARACTERISTICS (continued)

At T_A = 25ºC

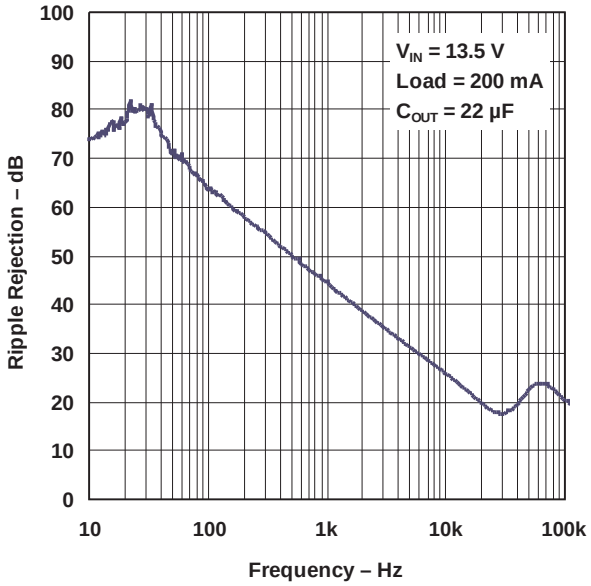
DELAY SWITCHING THRESHOLD versus JUNCTION TEMPERATURE



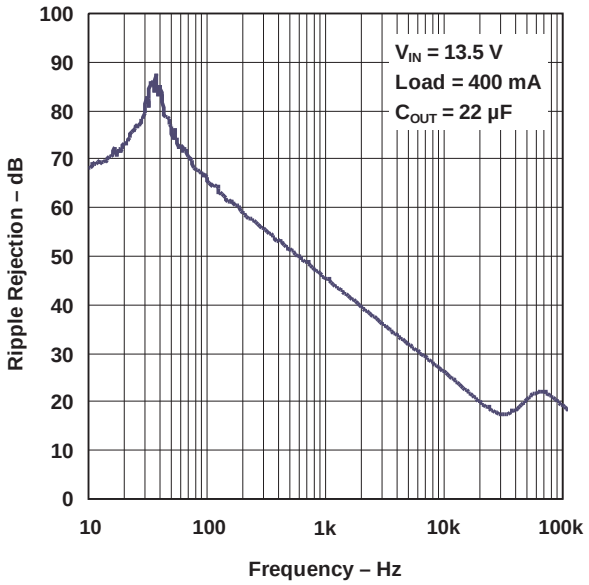
POWER-SUPPLY RIPPLE REJECTION versus FREQUENCY



POWER-SUPPLY RIPPLE REJECTION versus FREQUENCY

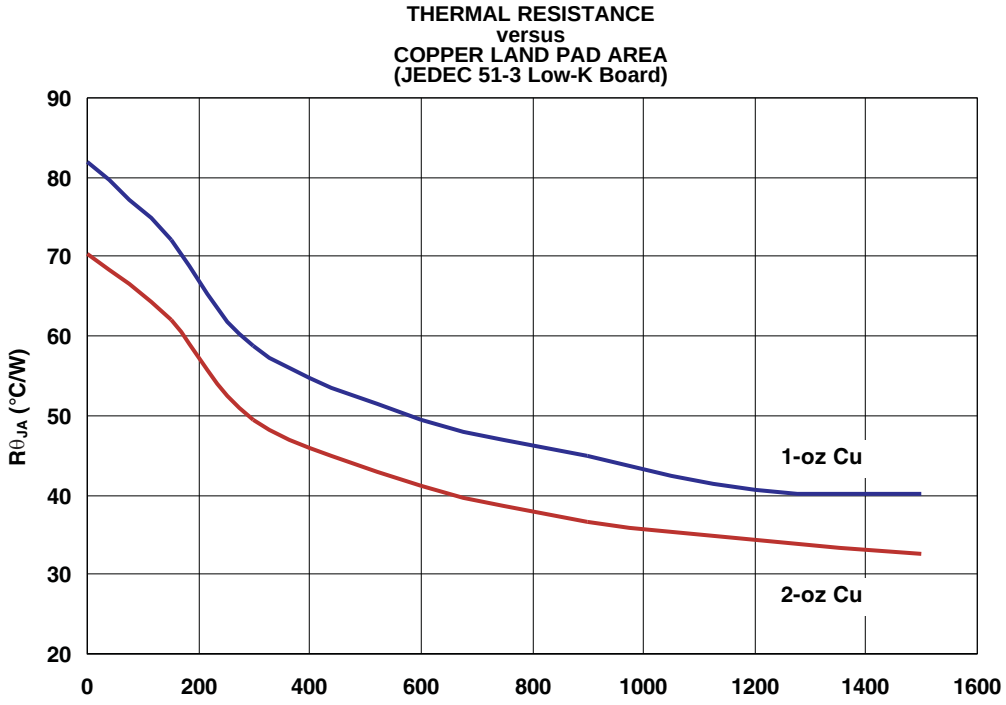


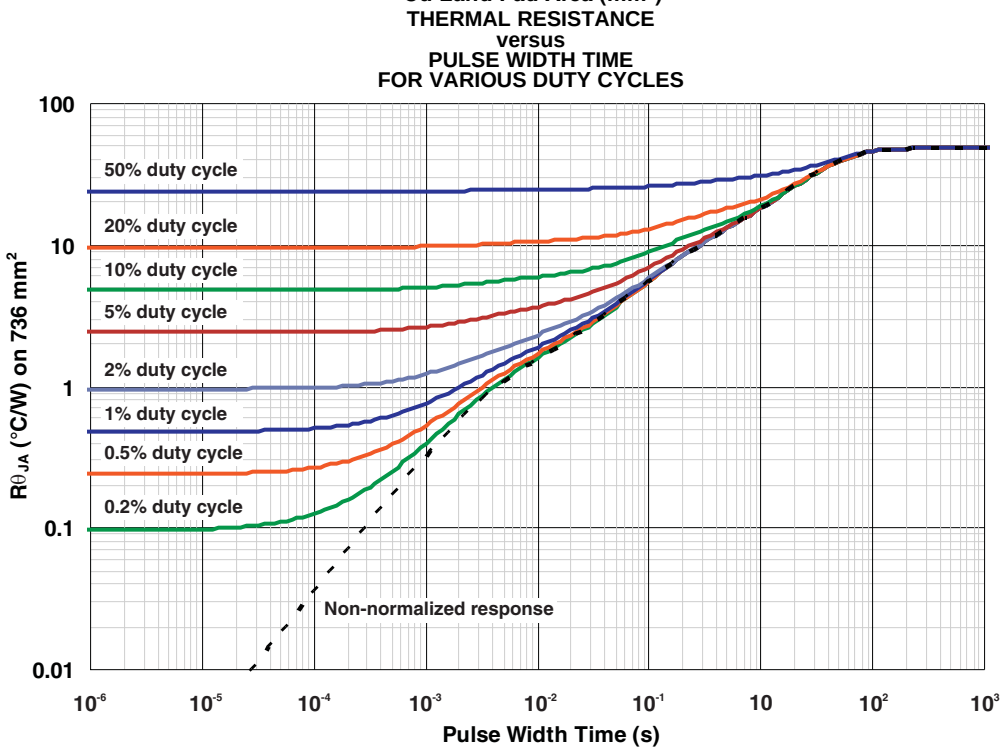
POWER-SUPPLY RIPPLE REJECTION versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

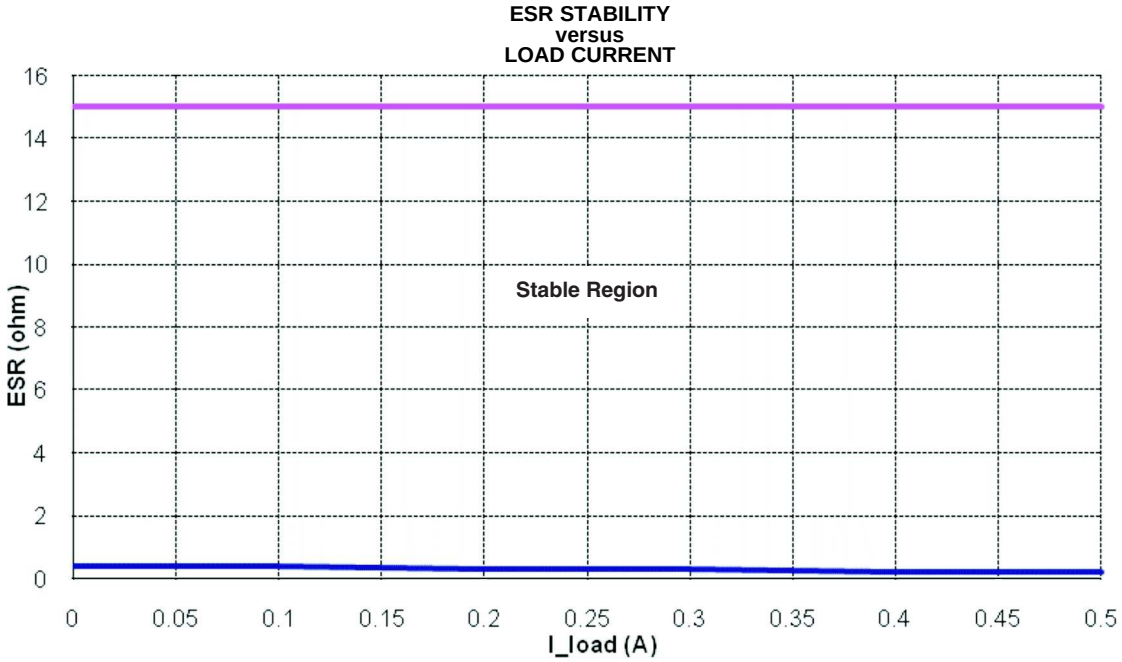
At T_A = 25ºC

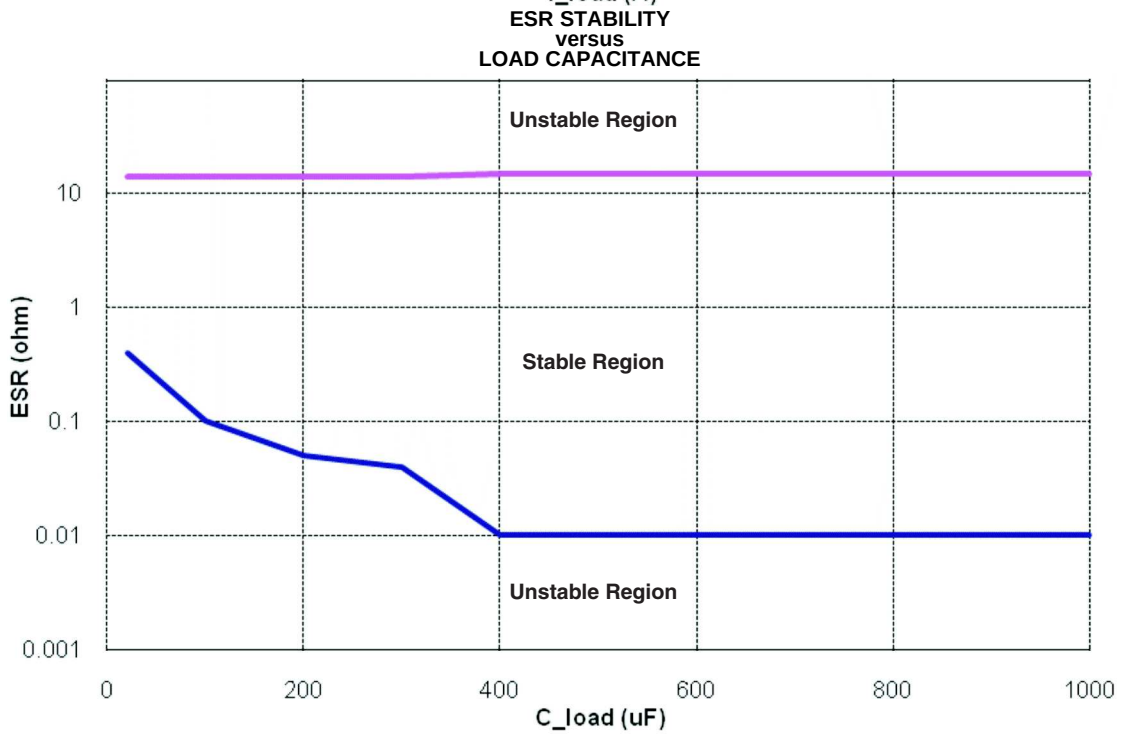




TYPICAL CHARACTERISTICS (continued)

At T_A = 25ºC





PARAMETER MEASUREMENT INFORMATION

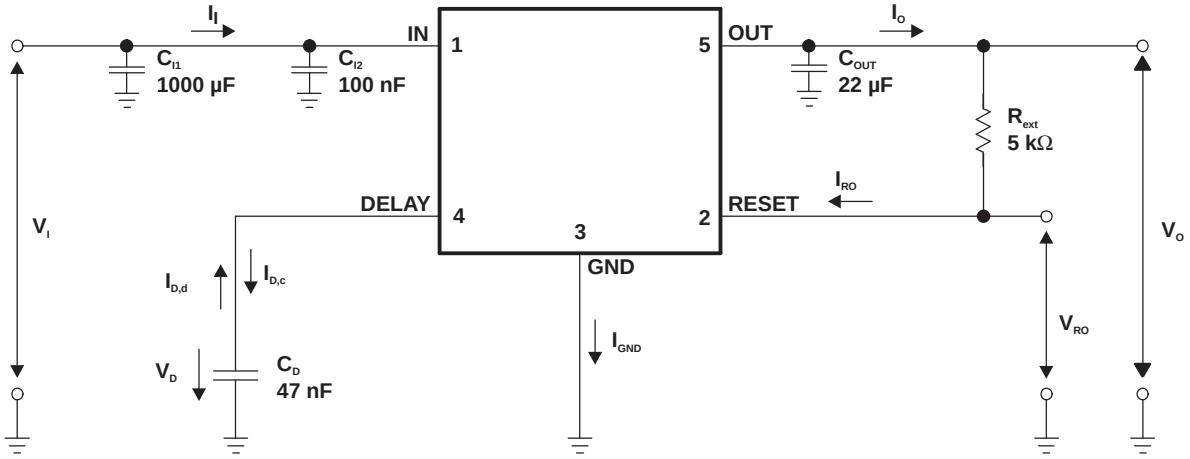


Figure 1. Test Circuit

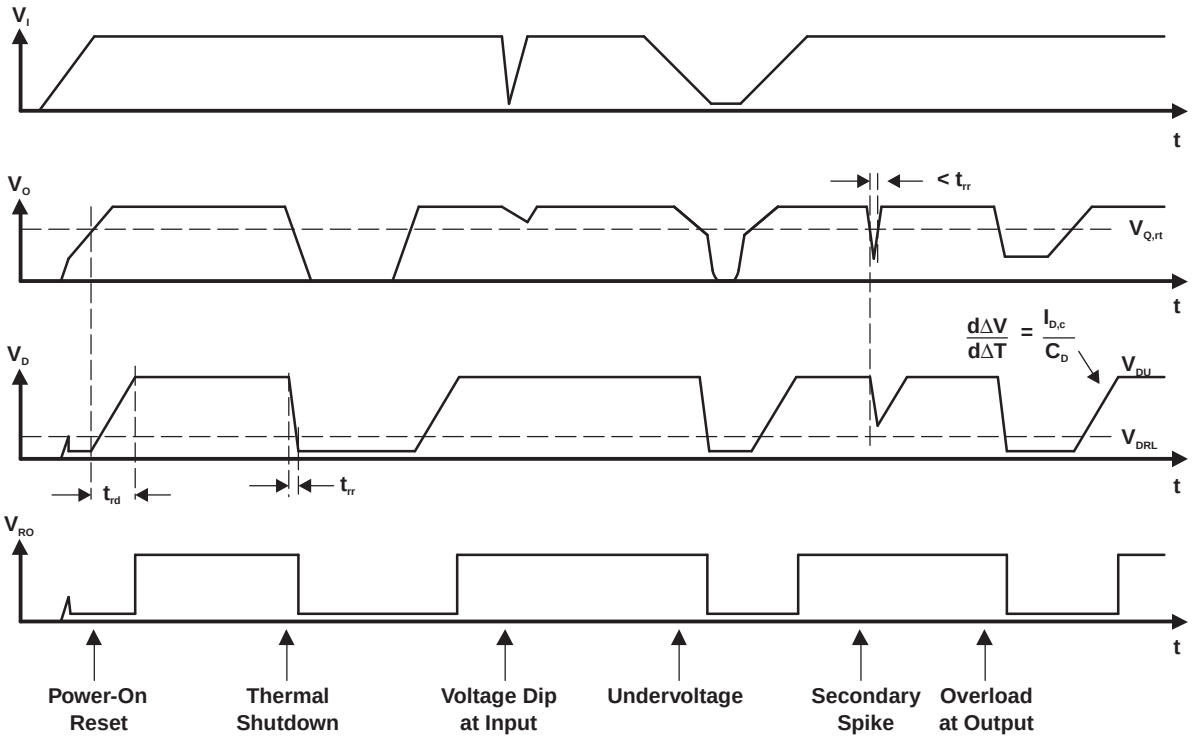


Figure 2. Reset Timing

REVISION HISTORY

Changes from Revision G (January 2013) to Revision H **Page**

- Deleted Ordering Information table 1
- Deleted row for θ_{JA} from Absolute Maximum Ratings table 3
- Added Thermal Information table 3

Changes from Revision F (May 2011) to Revision G **Page**

- Added pin out image for PWP package. 1
- Deleted package column from ordering information table, added orderable part number for PWP package and changed top-side marking to preview. 1
- Updated pin functions table with PWP package pin information. 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE4275QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TLE4275Q	Samples
TLE4275QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	TLE4275Q	Samples
TLE4275QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLE4275Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

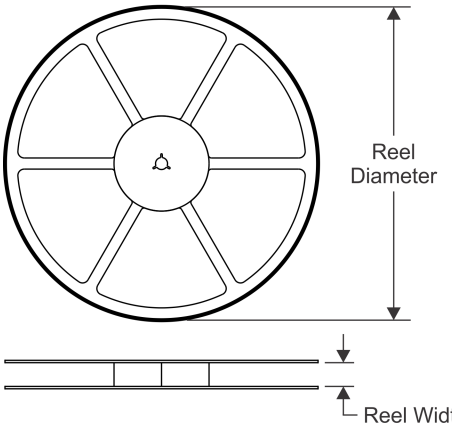
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

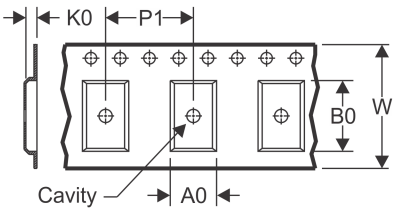
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

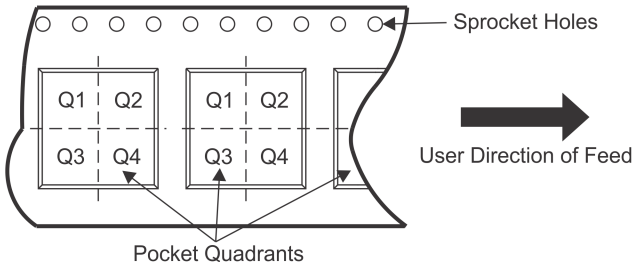


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

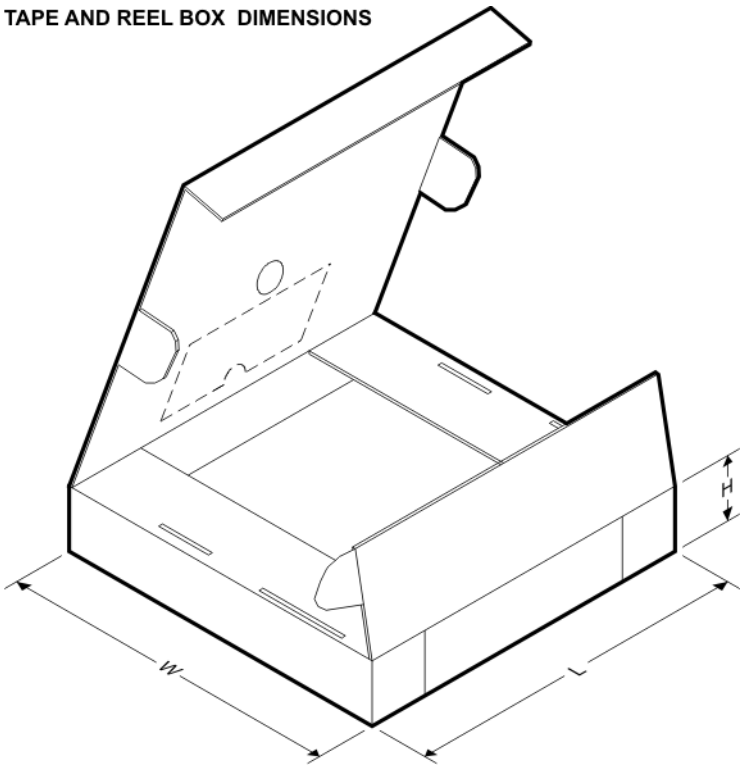
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE4275QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TLE4275QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLE4275QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

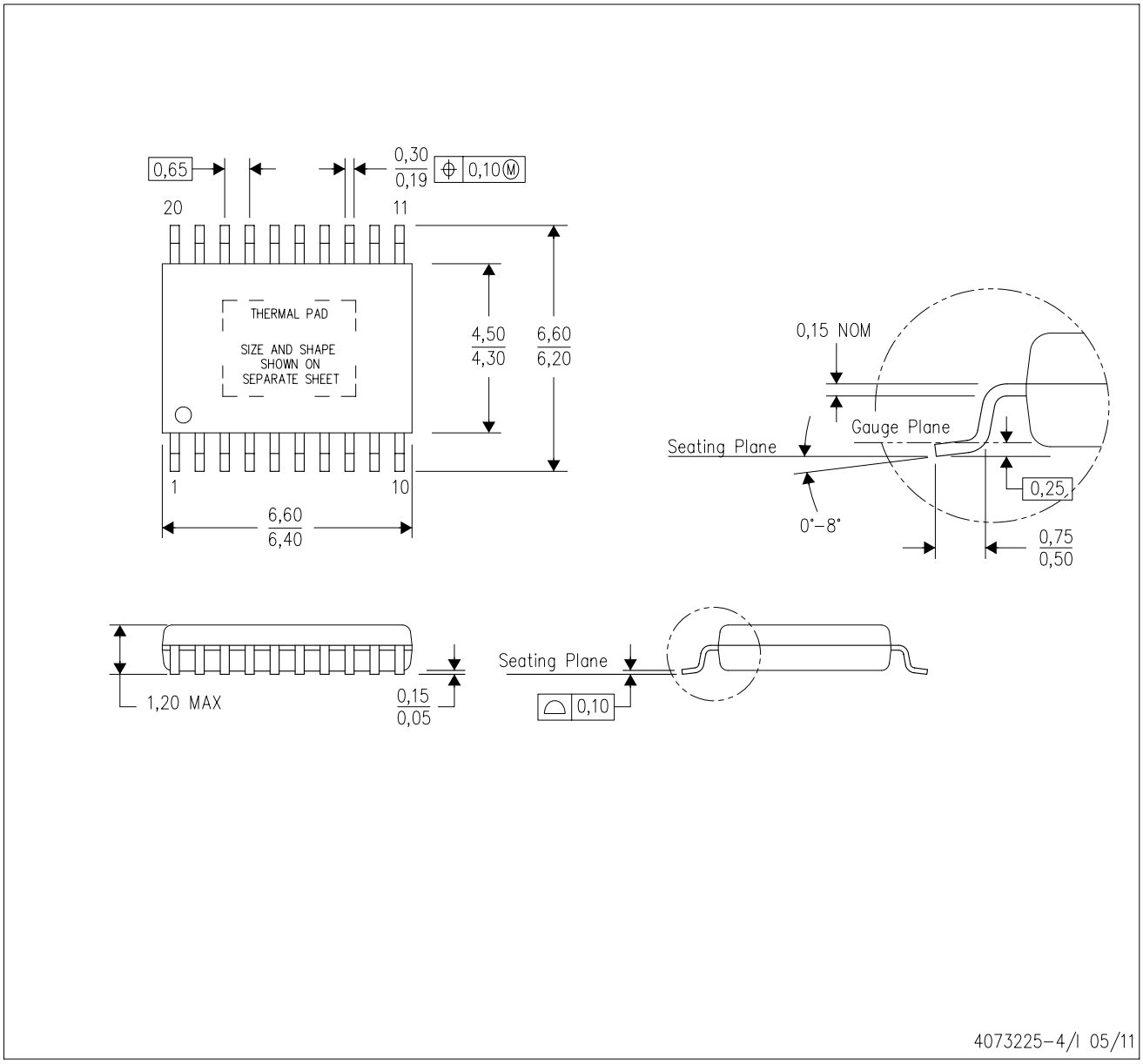
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE4275QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TLE4275QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TLE4275QPWPRQ1	HTSSOP	PWP	20	2000	367.0	367.0	38.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

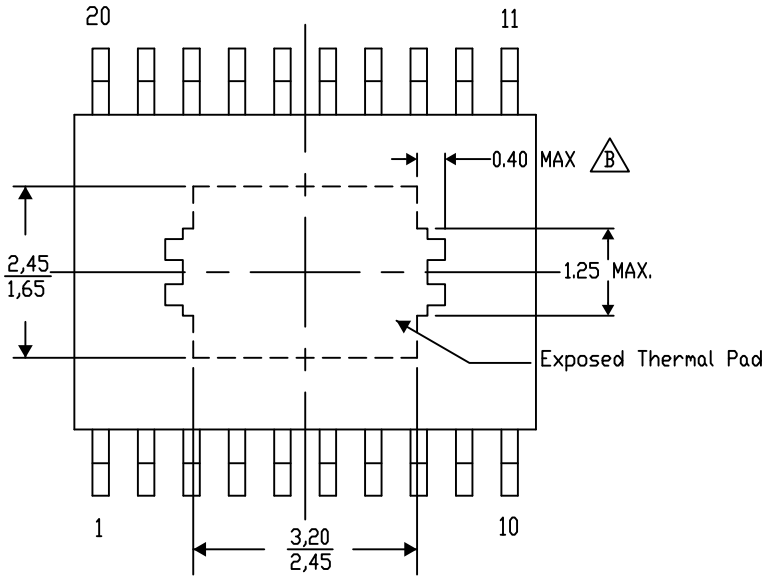
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

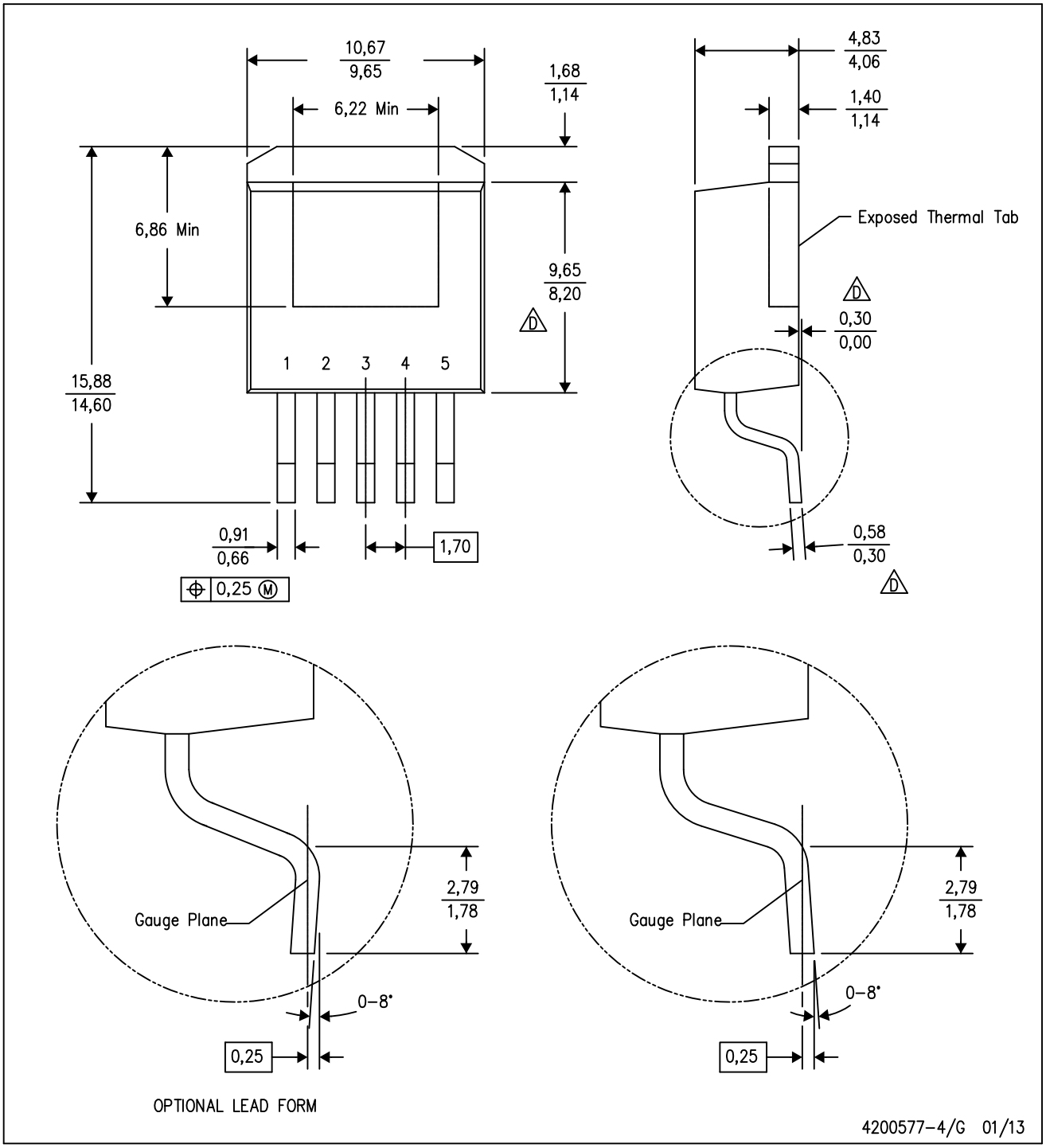
4206332–18/AF 06/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

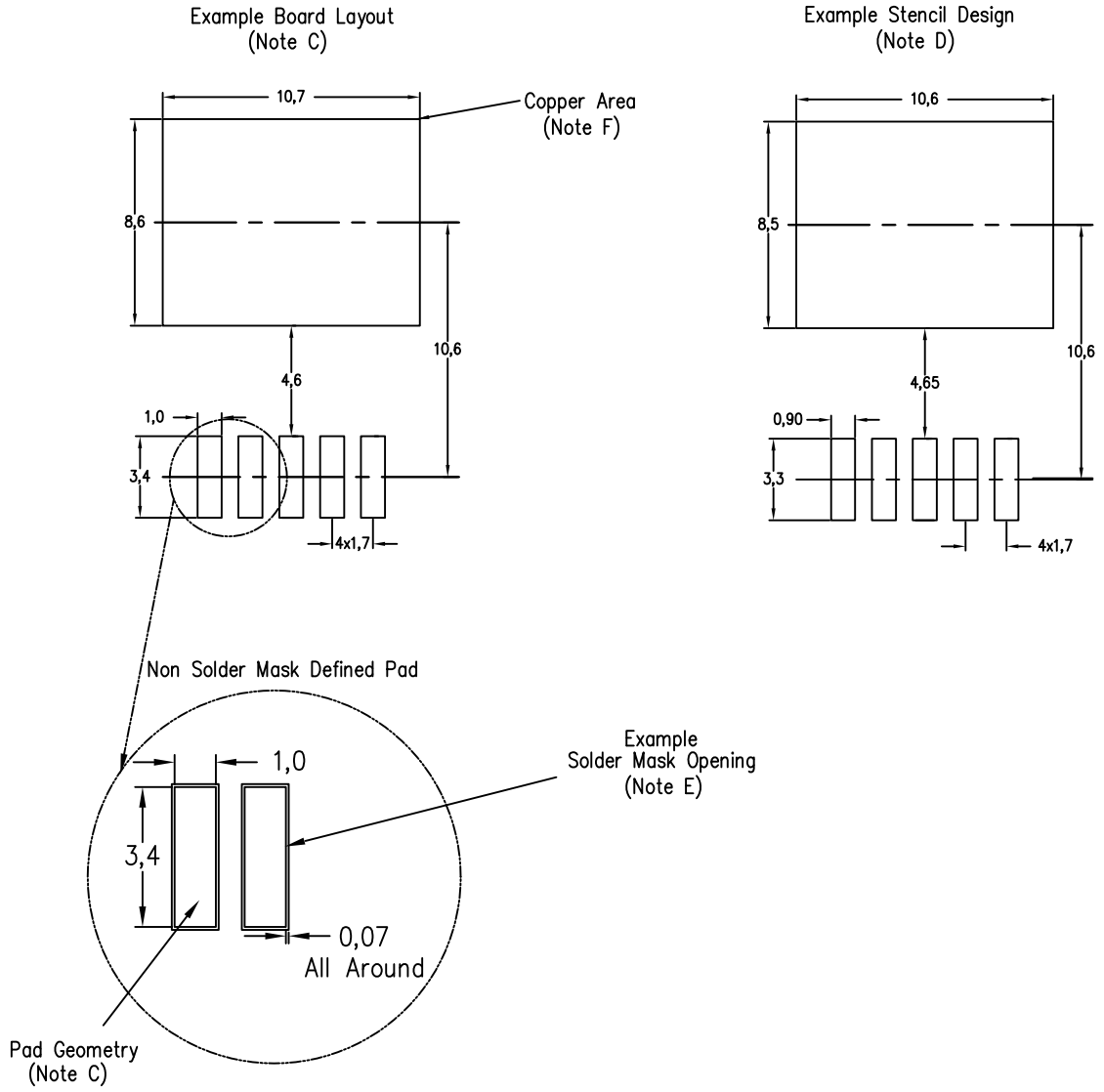
PowerPAD is a trademark of Texas Instruments

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



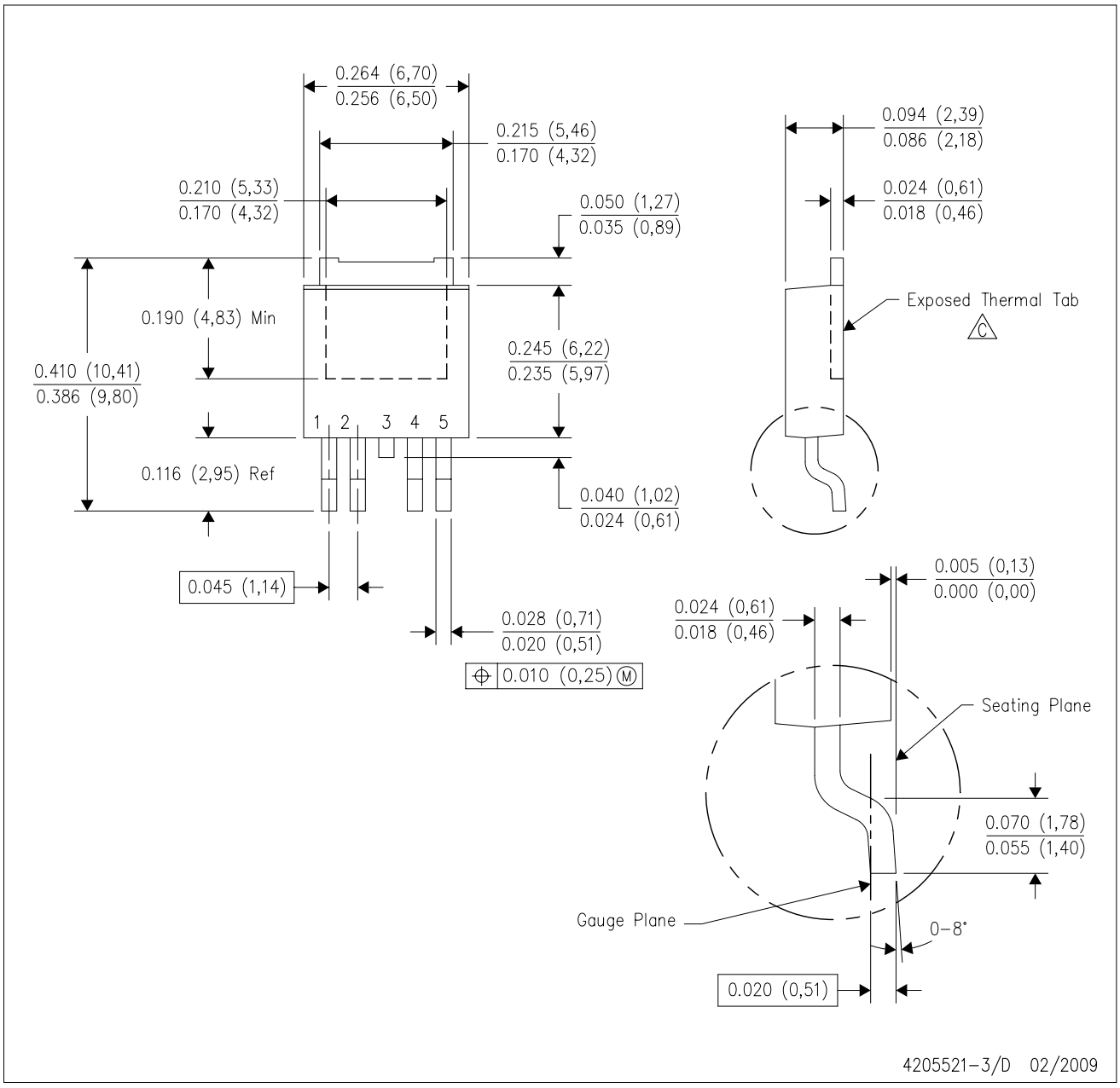
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

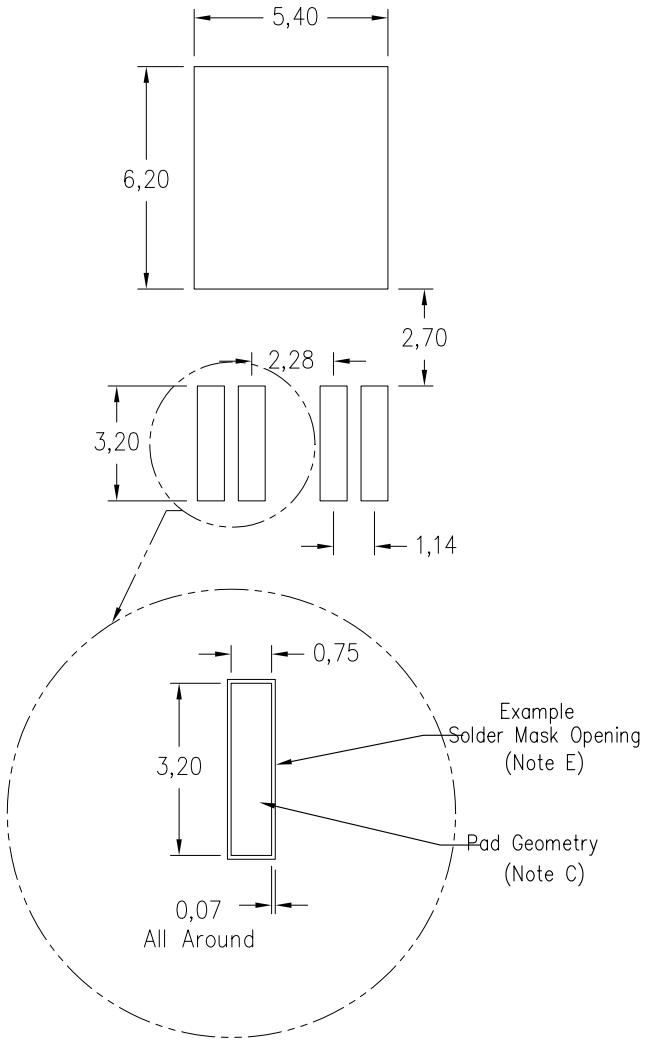
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



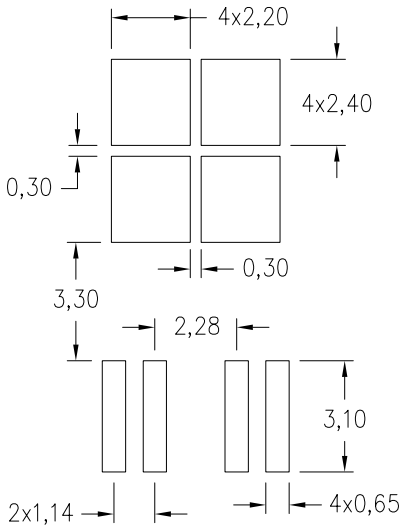
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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