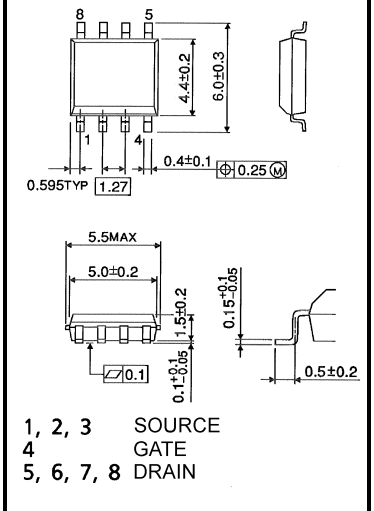
TOSHIBA Field Effect Transistor Silicon P-Channel MOS Type (Ultra-High-Speed U-MOSIII)

TPC8116-H

High Efficiency DC／DC Converter Applications
Notebook PC Applications
Portable Equipment Applications
CCFL Inverter Applications

- Small footprint due to a small and thin package
- High speed switching
- Small gate charge: Q_{SW} = 9.7 nC (typ.)
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 24mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ =14 S (typ.)
- Low leakage current: I_{DSS} = −10 μA (max) (V_{DS} = −40 V)
- Enhancement mode: V_{th} =−0.8 to−2.0 V (V_{DS} =−10 V, I_D =−1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-6J1B

Weight: 0.085 g (typ.)

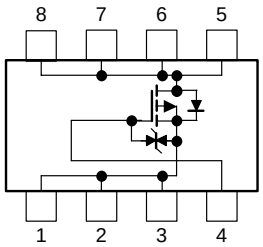
Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−40	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−40	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	−7.5	A
	Pulsed (Note 1)	I_{DP}	−30	
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.9	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	1.0	W
Single-pulse avalanche energy (Note 3)		E_{AS}	26	mJ
Avalanche current		I_{AR}	−7.5	A
Repetitive avalanche energy (Note 2a) (Note 4)		E_{AR}	0.12	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For Notes 1 to 4, refer to the next page.

This transistor is an electrostatic-sensitive device. Handle with care.

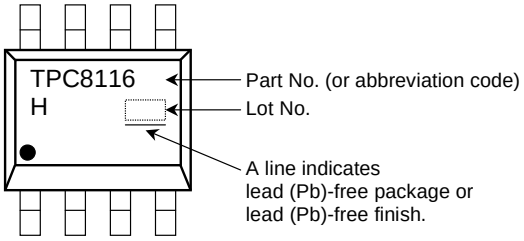
Circuit Configuration



Thermal Characteristics

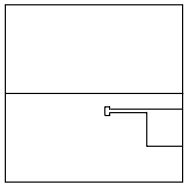
Characteristic	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	65.8	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	125	°C/W

Marking (Note 5)

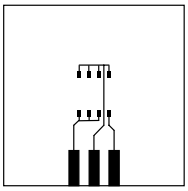


Note 1: The channel temperature should not exceed 150°C during use.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



(a)



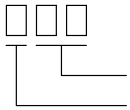
(b)

Note 3: V_{DD} = −24 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = −7.5 A

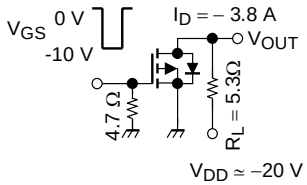
Note 4: Repetitive rating: pulse width limited by max channel temperature

Note 5: • on the lower left of the marking indicates Pin 1.

* Weekly code: (Three digits)



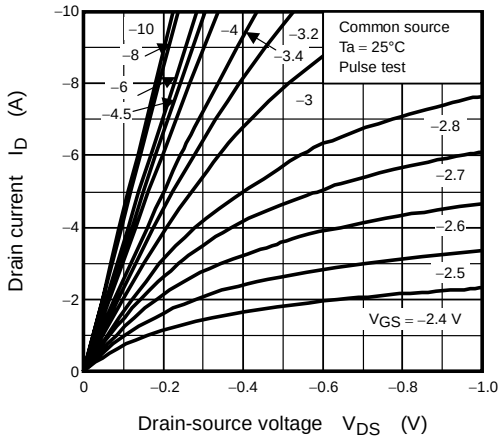
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I_{DSS}	V_{DS} = −40 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−40	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 20 V	−20	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−0.8	—	−2.0	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = −4.5 V, I_D = − 3.8 A	—	29	37	mΩ
			V_{GS} = −10 V, I_D = − 3.8 A	—	24	30	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = − 3.8 A	7	14	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	1190	—	pF
Reverse transfer capacitance		C_{rss}		—	170	—	
Output capacitance		C_{oss}		—	250	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	5	—	ns
	Turn-on time	t_{on}		—	12	—	
	Fall time	t_f		—	12	—	
	Turn-off time	t_{off}		—	43	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ −32 V, V_{GS} =−10V, I_D = −7.5A	—	27	—	nC
			V_{DD} ≃ −32 V, V_{GS} = −5 V, I_D = − 7.5A	—	15	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≃ −32 V, V_{GS} = −10 V, I_D = − 7.5A	—	3.2	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	8.1	—	
Gate switch charge		Q_{SW}		—	9.7	—	

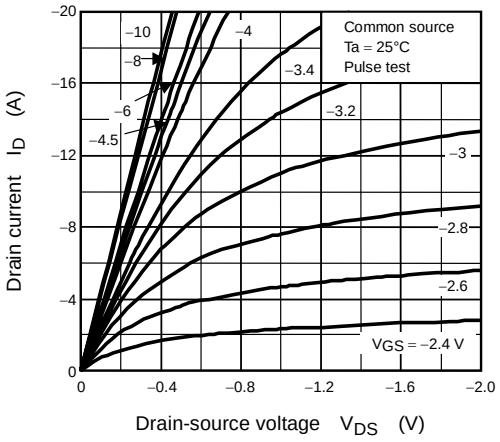
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−30	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −7.5 A, V_{GS} = 0 V	—	—	1.2	V

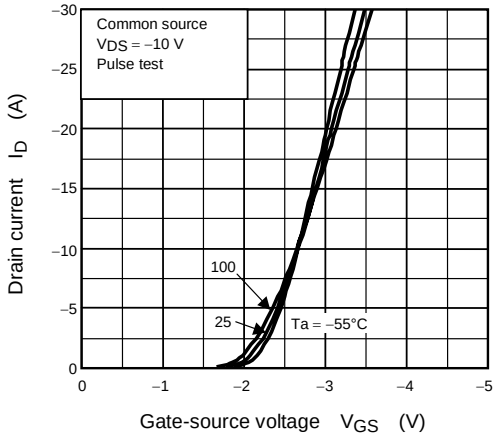
$I_D - V_{DS}$



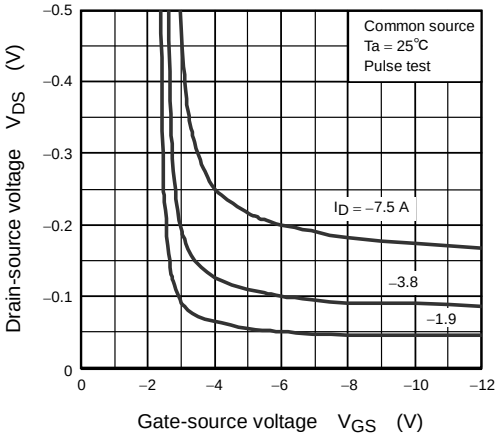
$I_D - V_{DS}$



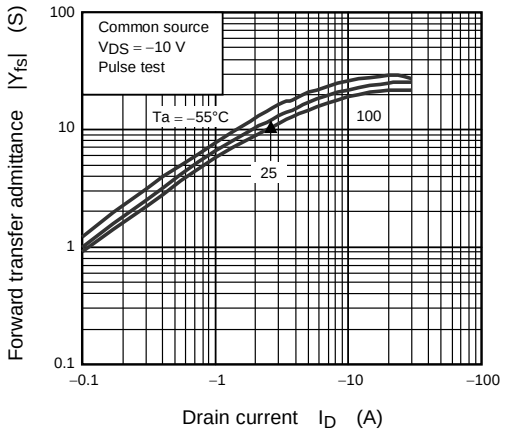
$I_D - V_{GS}$



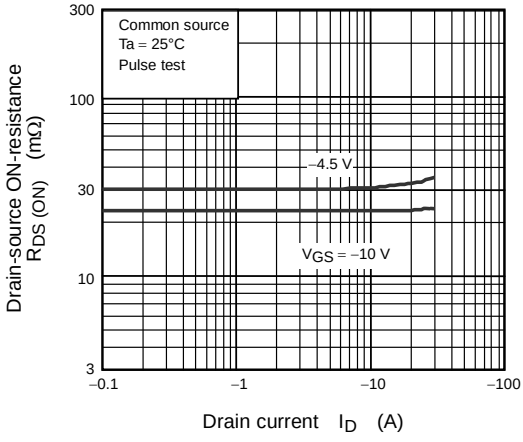
$V_{DS} - V_{GS}$



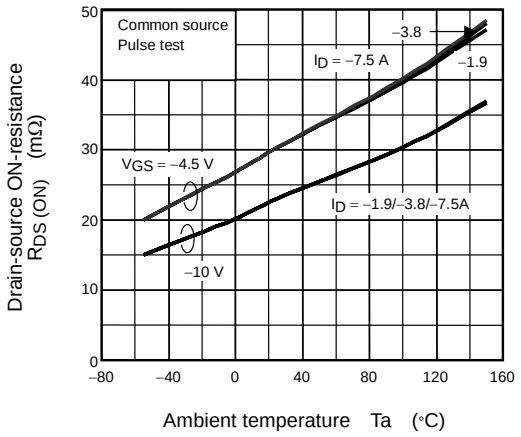
$|Y_{fs}| - I_D$



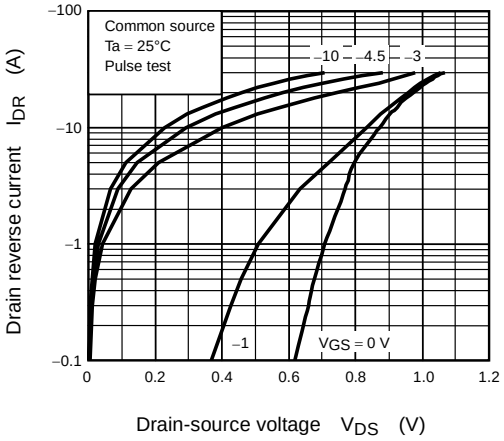
$R_{DS\ (ON)} - I_D$



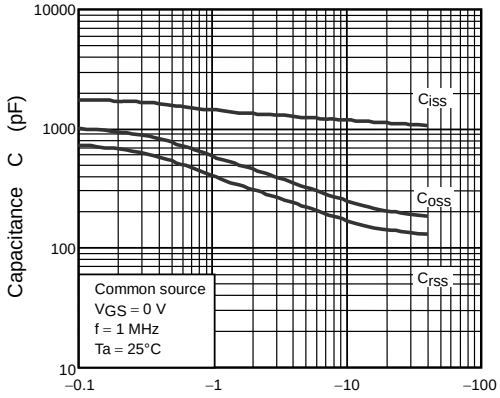
$R_{DS\ (ON)}$ – Ta



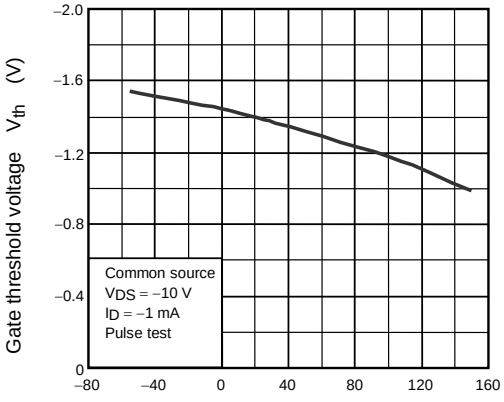
I_{DR} – V_{DS}



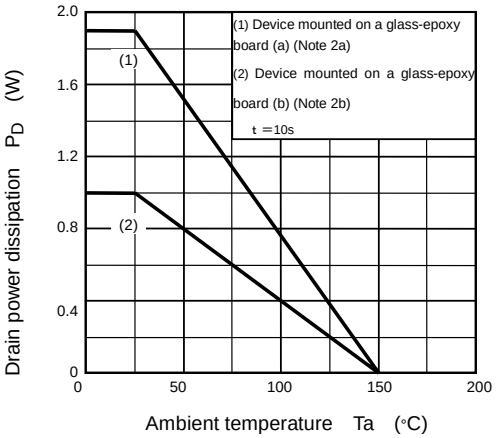
Capacitance – V_{DS}



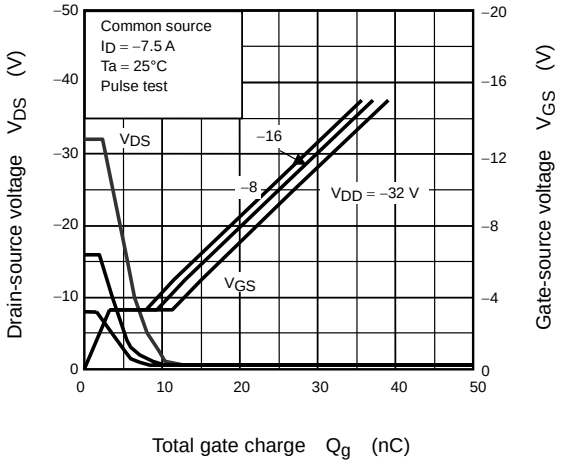
V_{th} – Ta



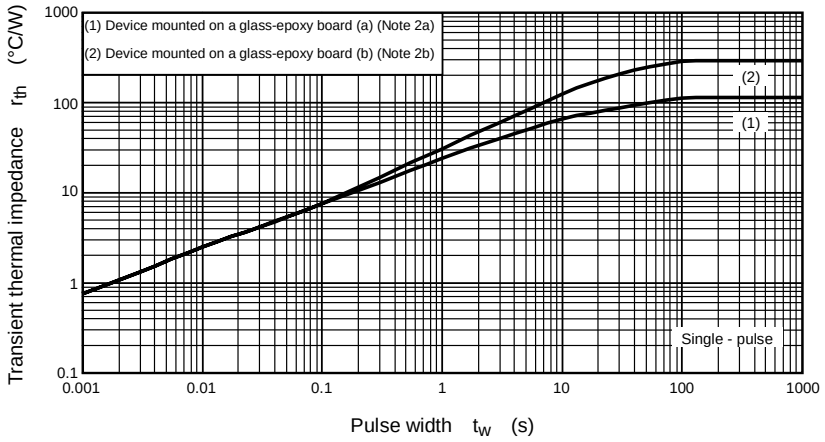
P_D – Ta



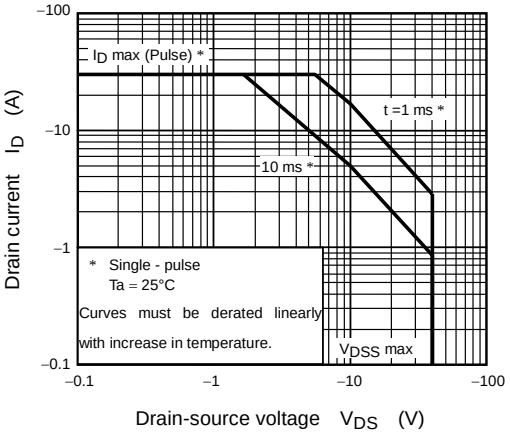
Dynamic input/output characteristics



$r_{th} - t_w$



Safe operating area



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