BUK7L11-34ARC

TrenchPLUS standard level FET

Rev. 03 — 3 December 2003 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance, integral gate resistor, ESD protection diodes and clamping diodes to protect the MOSFET from avalanching.

1.2 Features

- ESD and overvoltage protection
- Internal gate resistor
- Q101 compliant
- On-state resistance 8 mΩ (typ).

1.3 Applications

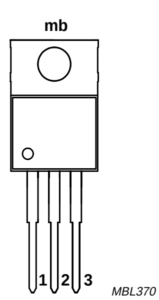
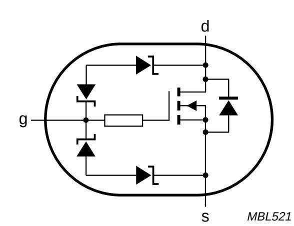
- 12 V loads
- Motors, lamps and solenoids.

1.4 Quick reference data

- $V_{DSR(CL)}$ = 41 V (typ)
- $I_D \leq 89$ A
- R_{DSon} = 8 mΩ (typ)
- $P_{tot} \leq 172$ W.

2. Pinning information

Table 1: Pinning - SOT78C, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 SOT78C (TO-220)	
2	drain (d)		
3	source (s)		
mb	mounting base, connected to drain (d)		

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BUK7L11-34ARC	TO-220	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads.	SOT78C

4. Limiting values

Table 3: Limiting values

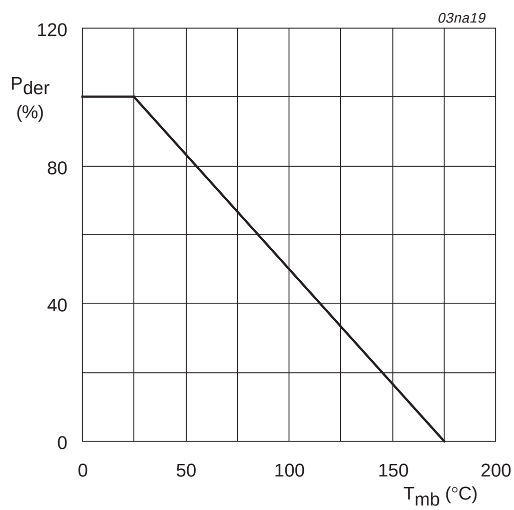
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)		[1]	-	34	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ	[1]	-	34	V
V_{GS}	gate-source voltage (DC)		[1]	-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	[2]	-	89	A
			[3]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	[2]	-	63	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs; Figure 3		-	358	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	172	W
$I_{DG(CL)}$	drain-gate clamping current	t_p = 5 ms; δ = 0.01		-	50	mA
$I_{GS(CL)}$	gate-source clamping current	continuous		-	10	mA
		t_p = 5 ms; δ = 0.01		-	50	mA
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	[2]	-	89	A
			[3]	-	75	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs		-	358	A
Avalanche ruggedness						
$E_{DS(CL)S}$	non-repetitive drain-source clamped energy	clamped inductive load; I_D = 60 A; $V_{DS} \leq$ 34 V; V_{GS} = 10 V; starting T_j = 25 °C		-	465	mJ
Electrostatic discharge						
V_{esd}	electrostatic discharge voltage; all pins	human body model; C = 100 pF; R = 1.5 kΩ		-	8	kV
		human body model; C = 250 pF; R = 1.5 kΩ		-	6	kV

[1] Voltage is limited by clamping.

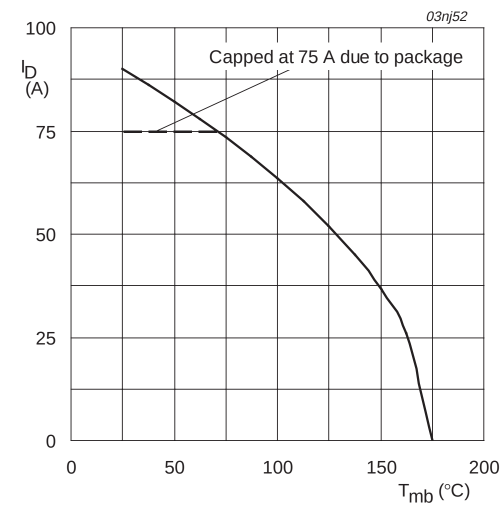
[2] Current is limited by power dissipation chip rating.

[3] Continuous current is limited by package.



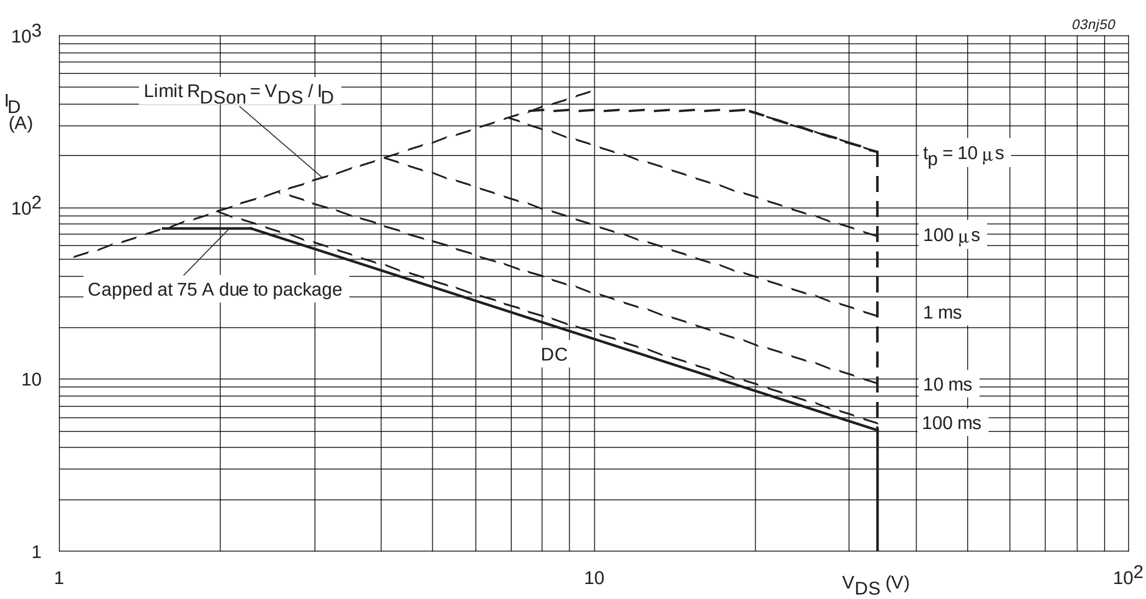
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25$ °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	0.55	0.87	K/W

5.1 Transient thermal impedance

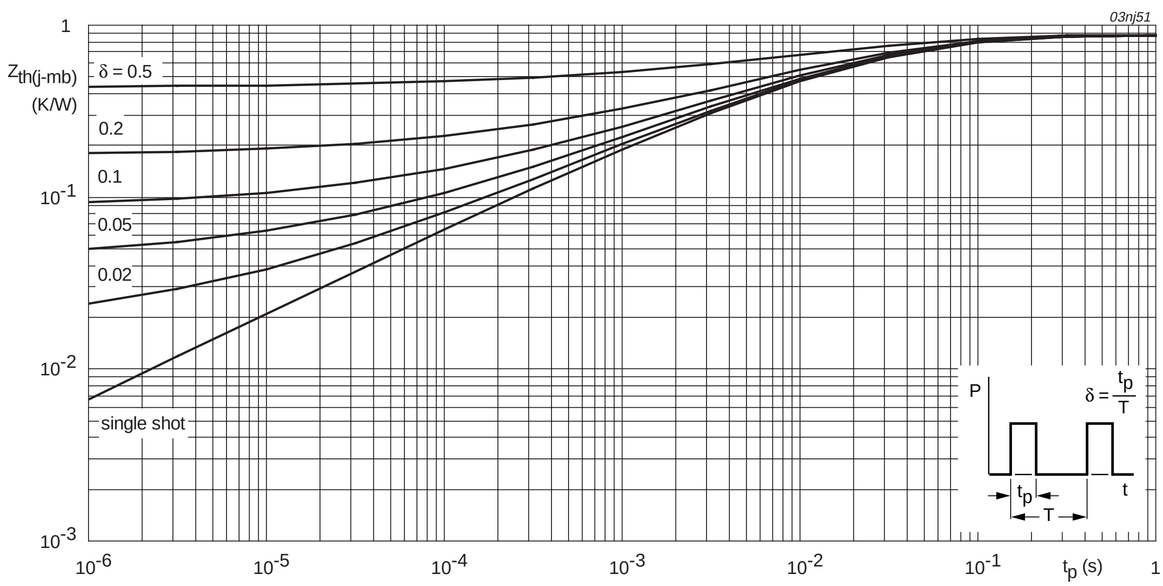


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

T_j = 25 °C unless otherwise specified.

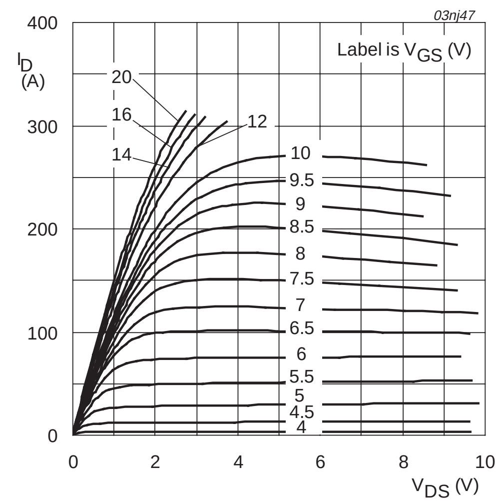
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DG}$	drain-gate zener breakdown voltage	I_D = 2 mA; V_{GS} = 0 V					
		T_j = 25 °C		34	-	45	V
		T_j = –55 °C		34	-	45	V
$V_{DSR(CL)}$	drain-source clamping voltage (DC)	$I_{GS(CL)}$ = –2 mA; I_D = 1 A Figure 16 and 17	[1]	-	41	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9					
		T_j = 25 °C		2.2	3	3.8	V
		T_j = 175 °C		1.2	-	-	V
		T_j = 150 °C		1.5	-	-	V
		T_j = –55 °C		-	-	4.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 16 V; V_{GS} = 0 V					
		T_j = 25 °C		-	0.1	2	µA
		T_j = 150 °C		-	3	50	µA
		T_j = 175 °C		-	18	250	µA
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = ±1 mA; –55 °C < T_j < +175 °C		20	22	-	V
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V					
		T_j = 25 °C		-	5	1000	nA
		T_j = 175 °C		-	-	50	µA
		V_{GS} = 16 V; V_{DS} = 0 V					
		T_j = 175 °C		-	-	150	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 30 A; Figure 7 and 8					
		T_j = 25 °C		-	8	11	mΩ
		T_j = 175 °C		-	-	20.9	mΩ
		V_{GS} = 16 V; I_D = 30 A			7	9.7	mΩ
R_G	Internal gate resistor			-	11	-	Ω
Dynamic characteristics							
$Q_{g(tot)}$	total gate charge	V_{GS} = 10 V; V_{DS} = 27 V; I_D = 25 A; Figure 14		-	53	-	nC
Q_{gs}	gate-source charge			-	11	-	nC
Q_{gd}	gate-drain (Miller) charge			-	20	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12		-	1880	2506	pF
C_{oss}	output capacitance			-	640	768	pF
C_{rss}	reverse transfer capacitance			-	400	548	pF

Table 5: Characteristics...*continued*

T_j = 25 °C unless otherwise specified.

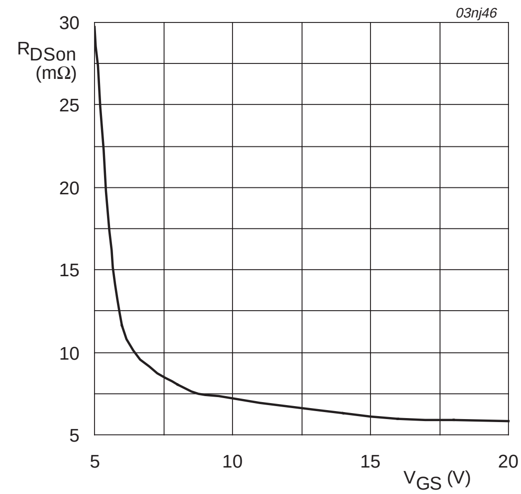
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	20	-	nS
t_r	rise time		-	92	-	nS
$t_{d(off)}$	turn-off delay time		-	127	-	nS
t_f	fall time		-	118	-	nS
L_d	internal drain inductance	measured from drain lead 6 mm from package to center of die	-	4.5	-	nH
		measured from contact screw on mounting base to center of die SOT78C	-	3.5	-	nH
L_s	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs V_{GS} = –10 V; V_{DS} = 30 V	-	52	-	ns
Q_r	recovered charge		-	28	-	nC

[1] Independent testing of MOSFET and clamping diodes safeguards against avalanching.



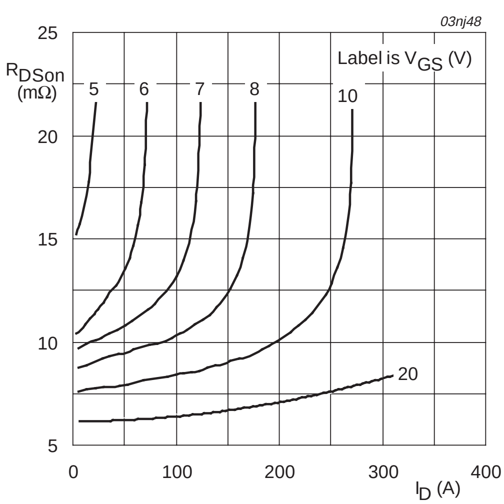
T_j = 25 °C; t_p = 300 µs

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



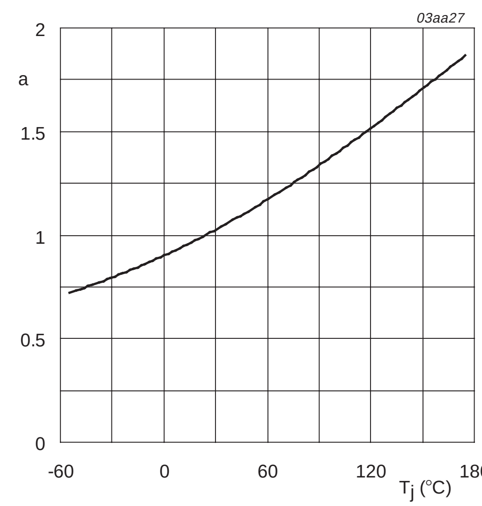
T_j = 25 °C; I_D = 30 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



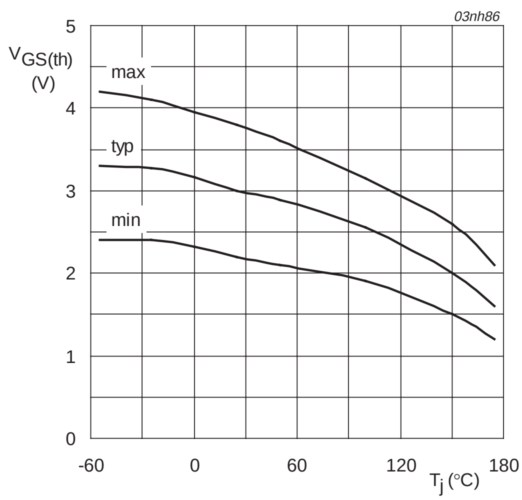
T_j = 25 °C; t_p = 300 µs

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



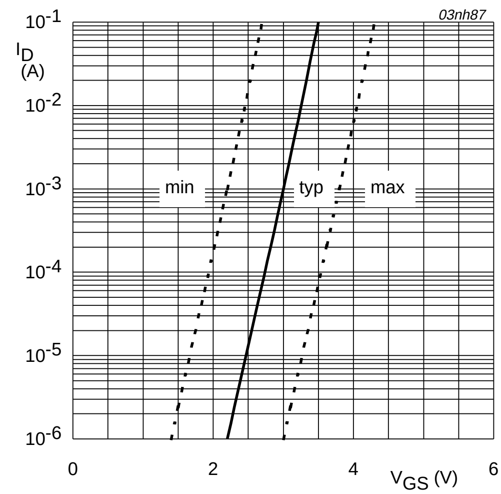
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



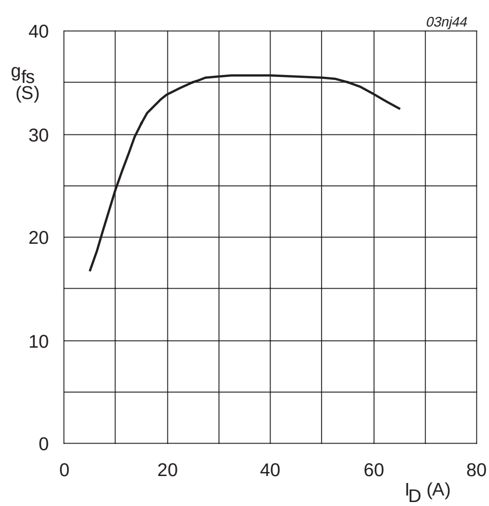
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



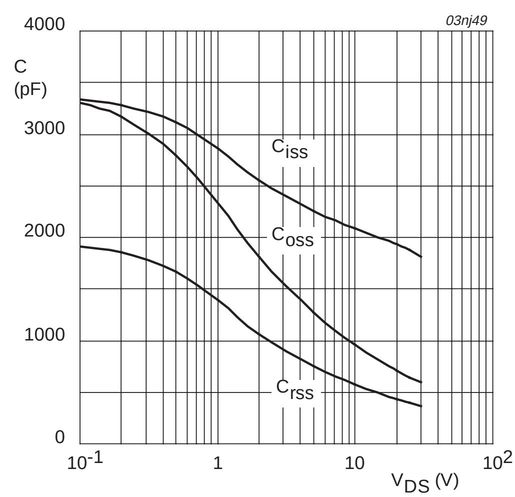
T_j = 25 °C; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



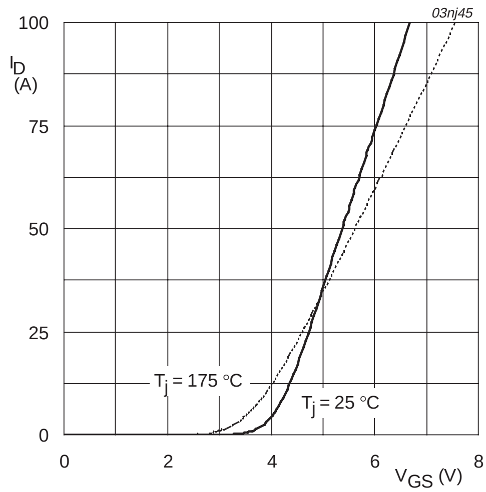
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values.



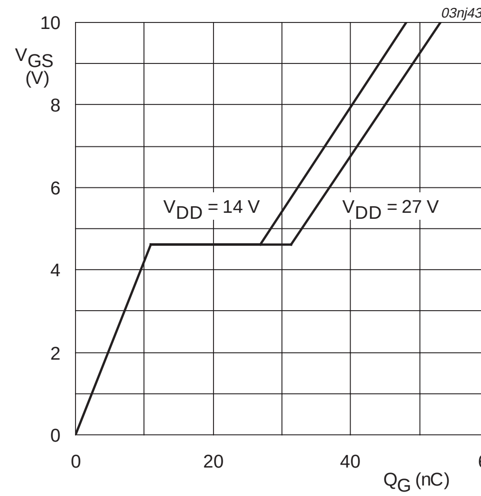
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



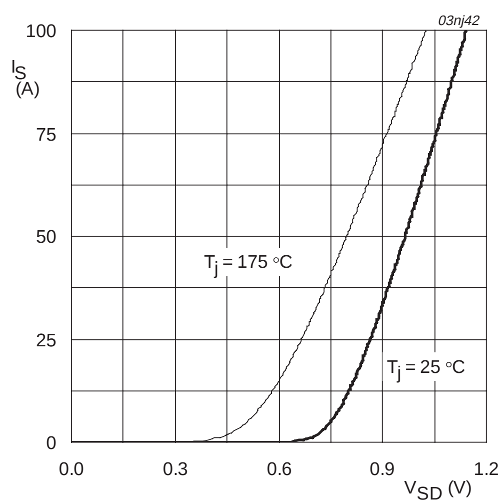
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



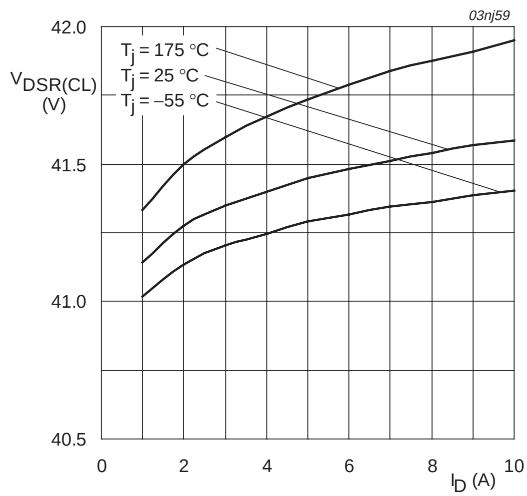
T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of gate charge; typical values.



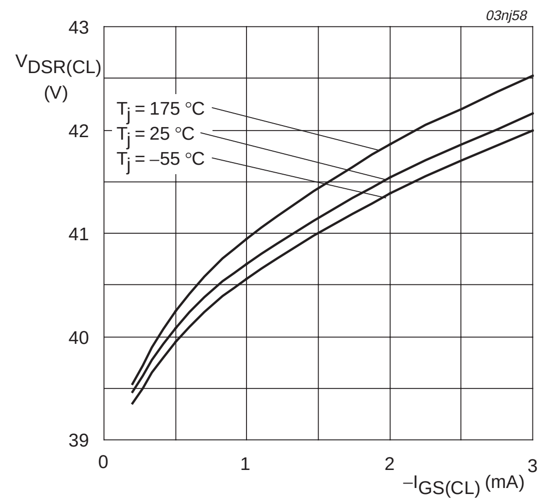
V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



I_{GD} = –2 mA

Fig 16. Drain-source clamping voltage as a function of drain current; typical values.

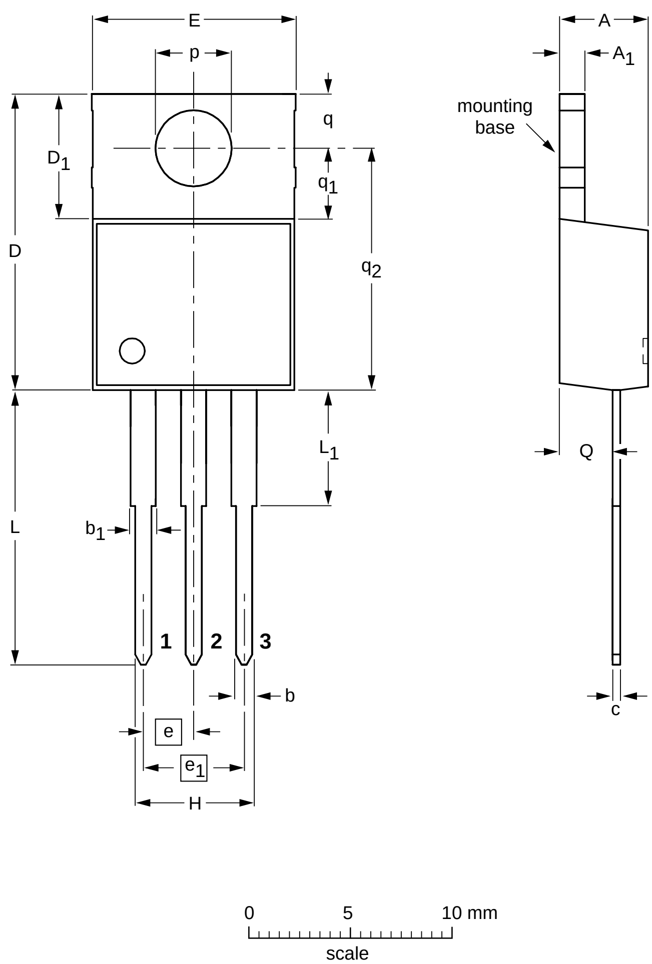


I_D = 10 A

Fig 17. Drain-source clamping voltage as a function of gate-source clamping current; typical values.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads **SOT78C**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1	b	b1	c	D	D1	E	e	e1	H	L	L1	p	Q	q	q1	q2
mm	4.58 4.31	1.33 1.21	0.87 0.76	1.33 1.21	0.44 0.33	15.07 14.80	6.47 6.22	10.40 10.00	2.64 2.44	5.16 5.00	6.03 5.76	14.00 13.50	6.10 5.58	3.90 3.78	2.72 2.40	2.95 2.69	3.80 3.42	12.40 12.00

Notes

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78C		3-lead TO-220				~~01-12-11~~ 03-01-21

Fig 18. SOT78C (TO-220).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20031203	-	**Product data (9397 750 12163)** • Avalanche Ruggedness parameter description in Section 4 changed from: ‘non-repetitive drain-source avalanche energy’ to ‘non-repetitive drain-source clamp energy’.
02	20030522	-	**Product data (9397 750 11472)** • Typical values of I_{DSS} added to characteristics table, Section 6.
01	20030423	-	**Product data (9397 750 11178)**

9. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Fax: +31 40 27 24825

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