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SM5807

NIPPON PRECISION CIRCUITS LTD.

FOLD OVER SAMPLING DIGITAL FILTER FOR DIGITAL AUDIO

■GENERAL DESCRIPTION

SM5807 is a four fold over sampling digital filter for low end digital audio system, using the molybdenum gate C-MOS process developed solely by NPC.

This LSI has two channel FIR filters, and the pass-band ripple is less than ±0.05dB, stop band attenuation is more than 50dB. The input and output datas are 16-bit serial, so the circuit system can be small.

■FEATURES

- FILTER STRUCTURE
  - -Four fold over sampling
  - -Tow channel filter
  - -Cascaded linear phase FIR filter (61st+13th order)
  - -On chip overflow limitter
  - -On chip quartz oscillation circuit
  - -Buffer output for XT input clock
- FILTER CHARACTERISTICS

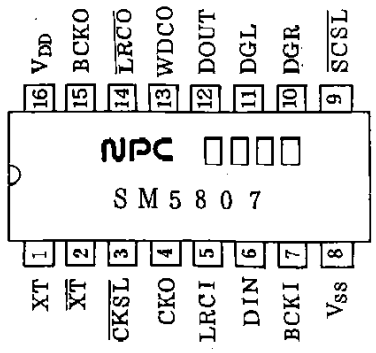
Filter chalacteristics	SM5807DP, DS	SM5807EP, ES, FP, FS
Pass band ripple(0~20kHz)	Within ±0.05dB	Within ±0.05dB
[Pass band attenuation]	[Within ±0.05dB]	[0~0.1dB]
Stop band attenuation(24.1kHz~)	More than 50dB	More than 45dB

  - -Linear Phase (There is no group delay distortion.)
- INPUT/OUTPUT
  - -16 bit serial input/output
    (2's complement code, MSB first)
  - -TTL compatible
  - -Interface for 2DACs(F type)
- Power supply voltage: 5V±0.5V
- 16 pin plastic DIP/SOP
- Molybdenum gate C-MOS process

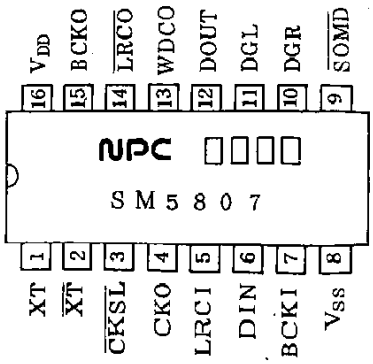
■PIN CONFIGURATION

TOP VIEW

•D, E Type



•F Type



■PACKAGE TYPE

TYPE	PACKAGE
SM5807DP, EP, FP	16 Pin plastic DIP
SM5807DS, ES, FS	16 Pin plastic SOP

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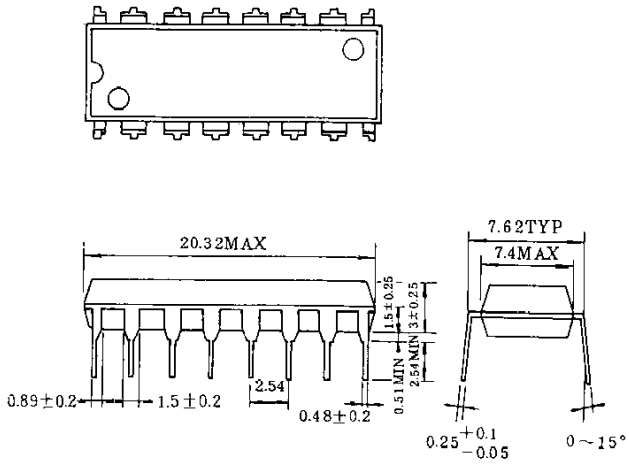
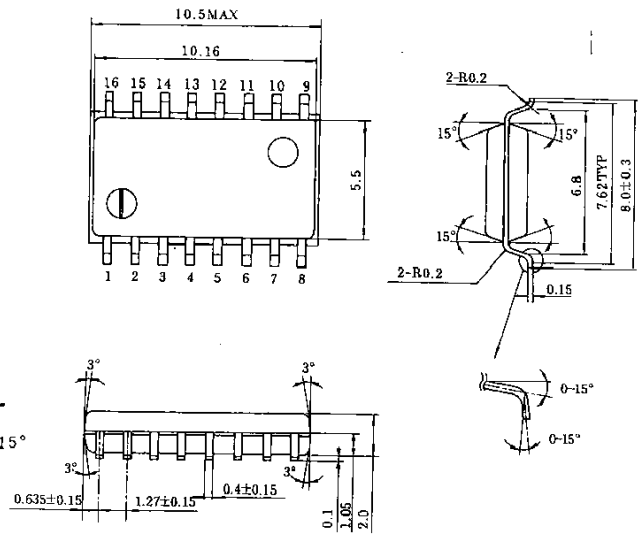
■PACKAGE DIMENSION(UNIT:mm)

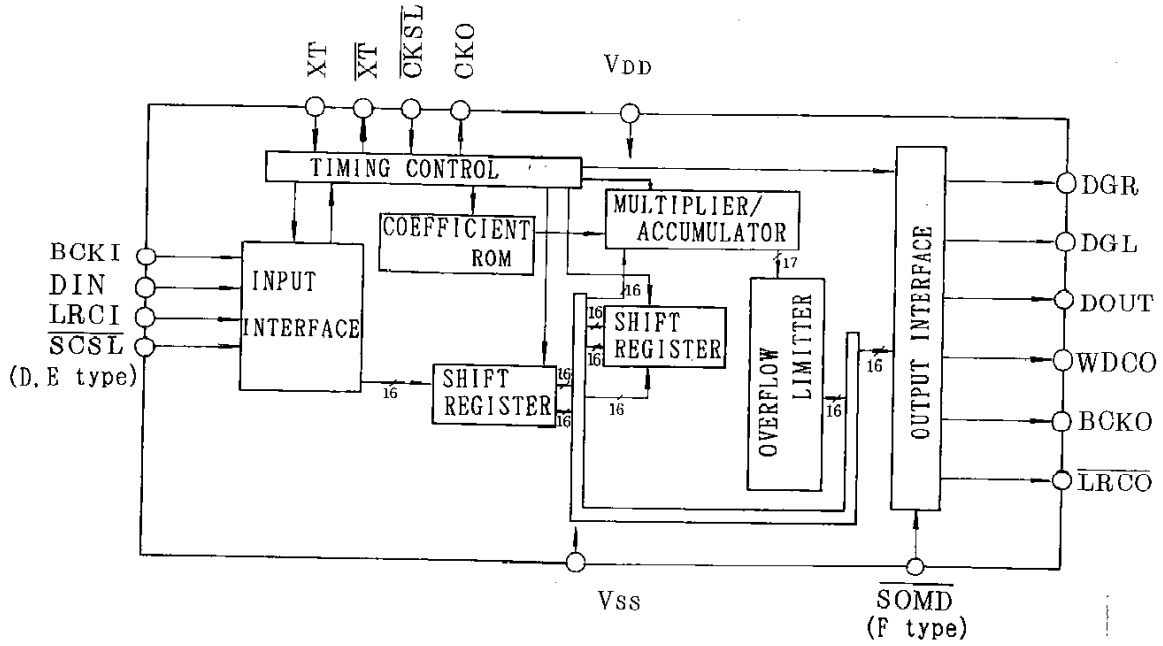
・DIP



・SOP



■BLOCK DIAGRAM



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■FILTER CHARACTERISTICS

(THEORITICAL VALUE)

1. SM5807 DP, DS

(frequency:0～88.2kHz)

ITEM	CHARACTERISTICS
PASS BAND	0～20kHz
STOP BAND	More than 24.1kHz
PASS BAND RIPPLE	Within ±0.05dB
STOP BAND ATTENUATION	More than 50dB

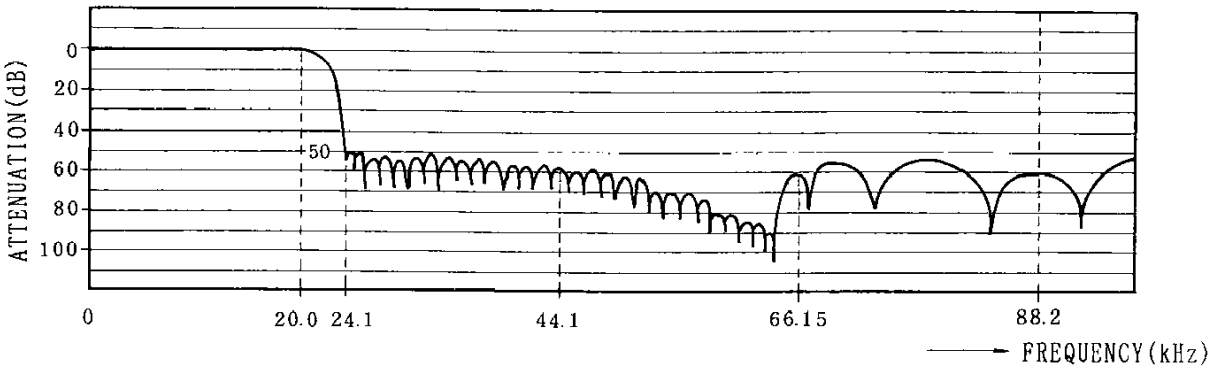

Fig. 1 Characteristics of frequency domain

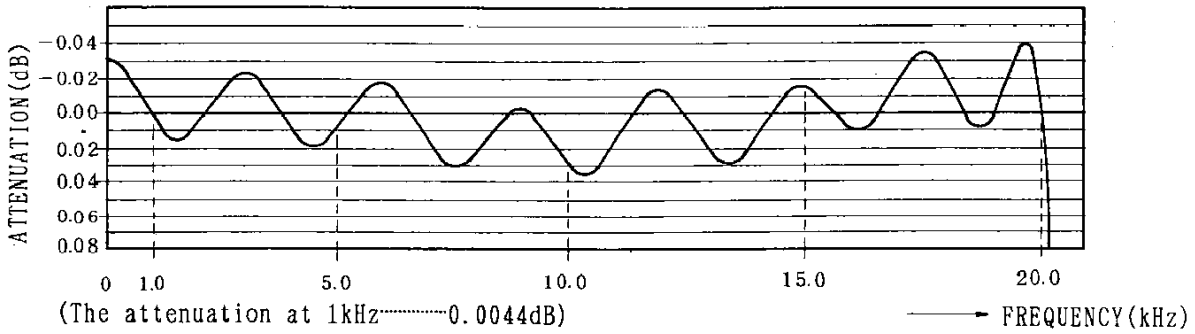

Fig. 2 Pass band

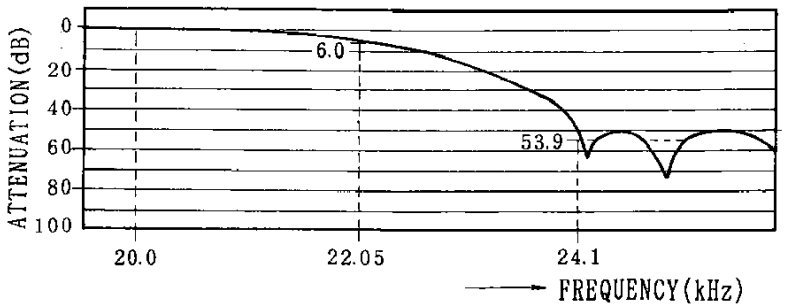

Fig. 3 The domain between pass band and stop band

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1. SM5807 EP, ES, FP, FS

(frequency:0～88.2kHz)

ITEM		CHARACTERISTICS
PASS BAND		0～20kHz
STOP BAND		More than 24.1kHz
PASS BAND RIPPLE		Within ±0.05dB
STOP BAND ATTENUATION	24.1~40kHz	More than 45dB
	40.0kHz～	More than 50dB

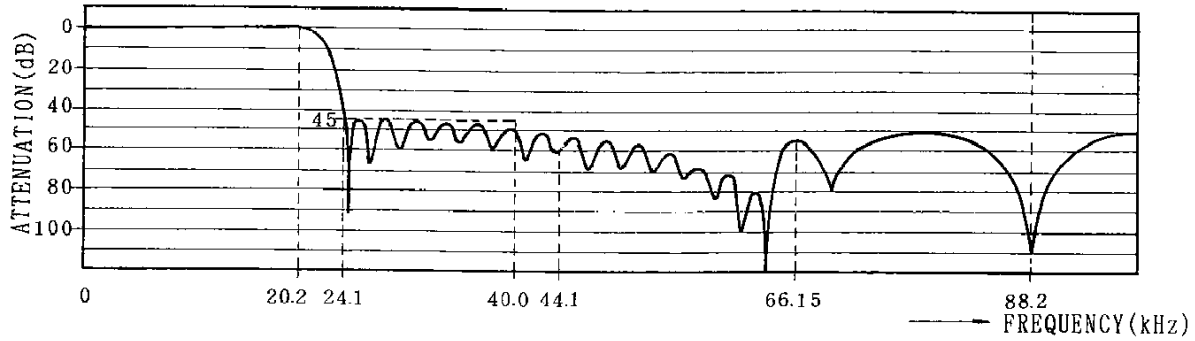
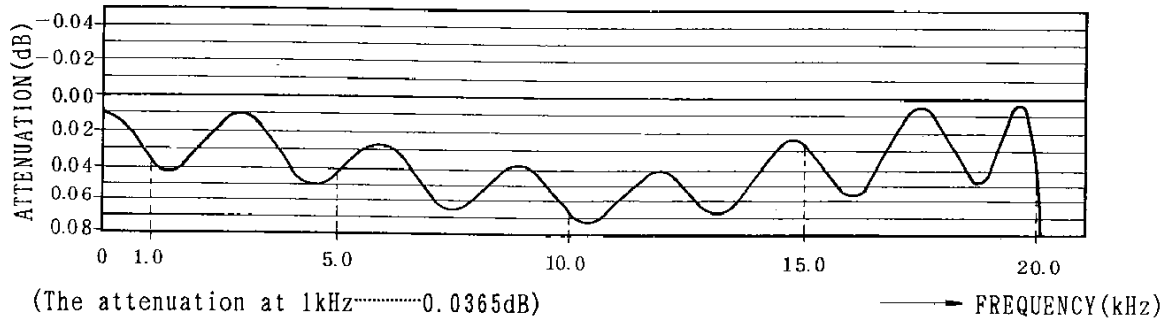


Fig. 4 Characteristics of frequency domain



(The attenuation at 1kHz·····0.0365dB)

Fig. 5 Pass Band

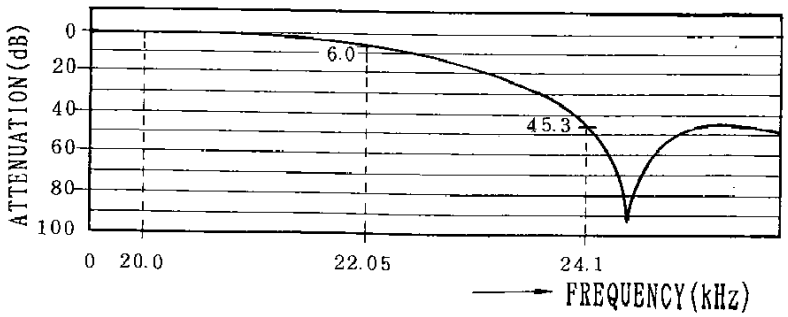


Fig. 6 The domain between pass band and stop band

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■PIN DESCRIPTION

No.	NAME	I/O	DESCRIPTION
1	XT	I	Input for oscillator or external clock input
2	$\overline{XT}$	O	Output for oscillator, No connect at using external clock
3	$\overline{CKSL}$	Ip	"H"……XT input clock is 16.9344MHz or 17.2872MHz(F type……only 16.9344MHz) "L"……XT input clock is 8.4672MHz or 8.6436MHz (F type……only 8.4672MHz)
4	CKO	O	Buffer out of XT clock
5	LRCI	Ip	Lch, Rch Synchronizing clock
6	DIN	Ip	Serial data input
7	BCKI	Ip	Timing clock for serial input data
8	Vss	—	Ground
9	$\overline{SCSL}$ (D, E)	Ip	"H"……System clock→192fs "L"……System clock→196fs (fs:Sampling frequency)
	$\overline{SOMD}$ (F)	Ip	"H"……Output interface for 1 DAC (Same as D, E type) "L"……Output interface for 2 DACs
10	DGR	O	Rch deglitch signal(176.4kHz)
11	DGL	O	Lch deglitch signal(176.4kHz)
12	DOUT	O	Serial data output
13	WDCO	O	Output timing control clock(352.8kHz)
14	$\overline{LRCO}$	O	Output timing control clock(176.4kHz)
15	BCKO	O	Timing clock for serial output data(8.4672kHz or 8.6436kHz) (F type……only8.4672MHz)
16	V_{DD}	—	Supply voltage(+5V)

NOTE) I :Input terminal
Ip:Input terminal with pull-up resistance
O :Output terminal

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■ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

ITEM	SYMBOL	LIMITS	UNIT
SUPPLY VOLTAGE	V_{DD}	-0.3～ 7.0	V
INPUT VOLTAGE	V_{IN}	-0.3～ V_{DD}+0.3	V
STORAGE TEMPERATURE	T_{STG}	-40～125	℃
POWER DISSIPATION	P_W	250	mW
SOLDERING TEMPERATURE	T_{SLD}	255	℃
SOLDERING TIME	t_{SLD}	10	Sec

■RECOMMENDATORY OPERATING CONDITION

(Vss=0V)

IETM	SYMBOL	CONDITION	UNIT
SUPPLY VOLTAGE	V_{DD}	4.5～ 5.5	V
OPERATING TEMPERATURE	T_{OPR}	-20～70	℃

■ELECTRIC CHARACTERISTICS

・DC CHARACTERISTICS (Ta=-20～70℃、V_{DD}=4.5～5.5V、V_{SS}=0V)

ITEM	TERMINAL	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION	V_{DD}	I_{DD}	V_{DD}=5V			20	mA
INPUT VOLTAGE(1)	XT	V_{IH1}		0.7V_{DD}			V
		V_{IL1}				0.3V_{DD}	V
INPUT VOLTAGE(2)	(*1)	V_{IH2}		2.4			V
		V_{IL2}				0.5	V
OUTPUT VOLTAGE	(*2)	V_{OH}	I_{OH}=-0.4mA	2.5			V
		V_{OL}	I_{OL}=1.6mA			0.4	V
INPUT LEAK CURRENT	XT	I_{LH}	V_{IN}=V_{DD}		5	15	μA
		I_{LL}	V_{IN}=0V		5	15	μA
	(*1)	I_{LH}	V_{IN}=V_{DD}			1.0	μA
INPUT CURRENT	(*1)	I_{IL}	V_{IN}=0V		10	20	μA

<TERMINAL>

*1	$\overline{CKSL}$, LRCI, DIN, BCKI, $\overline{SCSL}$(D, E Type), $\overline{SOMD}$(F Type)
*2	CKO, $\overline{LRCO}$, BCKO, WDCO, DOUT, DGL, DGR

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・AC CHARACTERISTICS

1. XT TERMINAL

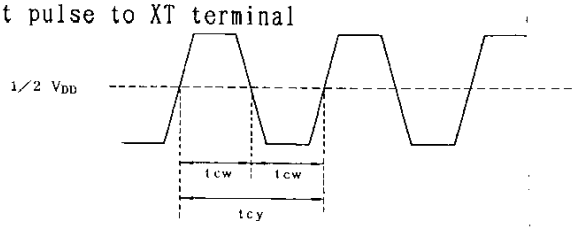
a. In case of crystal oscillation (Ta=-20～70℃, VDD=4.5～5.5V, VSS=0V)n

ITEM	SYMBOL	MIN	TYP	MAX	UINT	CONDITION
Oscillating frequency	f_{OSC}			20	MHz	$\overline{CKSL}$=H
				10	MHz	$\overline{CKSL}$=L

b. In case of clock input to XT terminal (Ta=-20～70℃, VDD=4.5～5.5V, VSS=0V)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Width of clock pulse	tcw	50		1000	nSec	$\overline{CKSL}$=L
		25		500	nSec	$\overline{CKSL}$=H
Cycle time of clock pulse	tcy	100		2000	nSec	$\overline{CKSL}$=L
		50		1000	nSec	$\overline{CKSL}$=H

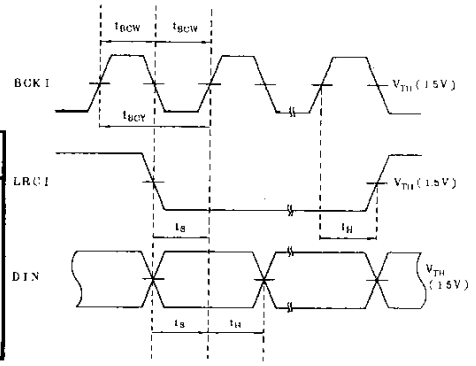
Input pulse to XT terminal



2. INPUT TIMING (DIN, BCKI, LRCI)

(Ta=-20～70℃, V_{DD}=4.5～5.5V, V_{SS}=0V)

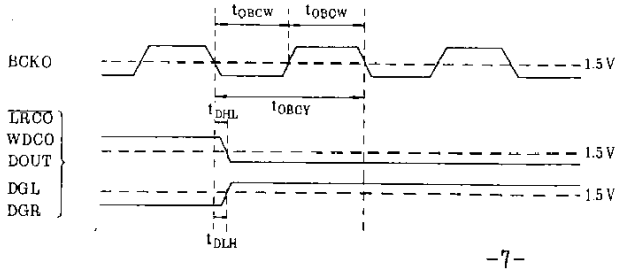
ITEM	SYMBOL	MIN	TYP	MAX	UNIT
BCKI, Pulse width	t_{BCW}	100			nSec
BCKI, Cycle time	t_{BCY}	200			nSec
DIN, LRCI, Set up time	ts	75			nSec
DIN, LRCI, Hold time	t_H	75			nSec



3. OUTPUT TIMING

(Ta=-20～70℃, V_{DD}=4.5～5.5V, V_{SS}=0V)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
BCKO, Pulse width	t_{OBCW}	40			nSec	
BCKO, Cycle time	t_{OBCY}	100			nSec	
Output delay time	t_{DHL}	0		25	nSec	$\overline{LRCO}$, WDCO, DOUT, DGL, DGR
	t_{DLH}			25	nSec	



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■FUNCTION

(1)SYSTEM CLOCK

D,E type $\overline{SCSL}$=H or OPEN·····192fs(8.4672MHz)
$\overline{SCSL}$=L·····196fs(8.6436MHz)
F type ·····only 192fs(8.4672MHz)
} fs:Sampling frequency(44.1kHz)

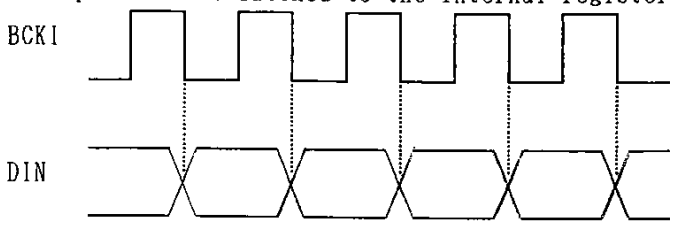
* Generating clock·····Crystal oscillation or external clock

	D,E Type($\overline{SCSL}$=H or OPEN) F Type		D,E Type($\overline{SCSL}$=L)	
$\overline{CKSL}$	H or open	L	H or open	L
XT/XT input frequency	384fs= 16.9344MHz	192fs= 8.4672MHz	392fs= 17.2872MHz	196fs= 8.6436MHz
CKO output	↑	↑	↑	↑
Internal system clock	192fs= 8.4672MHz	↑	196fs= 8.6436MHz	↑

(2)SERIAL INPUT(DATA & TIMING CLOCK)

The seial data input timing is raising edge of BCKI. So the input serial data must be changed at falling edge of BCKI.

And the input data is latched to the internal register by LRCI.



(3)INPUT DATA FORMAT

The input data format is 2's complement and MSB first.

(4)INTERNAL CALCULATION

The internal calculation starts at raising edge of LRCI.

(5)SERIAL OUTPUT(DATA & TIMING CLOCK)

The Lch/Rch datas are out from DOUT terminal alternately. So the 1 DAC interface system can be available.(D,E type & $\overline{SOMD}$=H of F type)

And using F type($\overline{SOMD}$=L) and 2DACs, the in-phase conversion is posible.

(Refer to 12 page.)

The output timing clock is out from BCKO terminal and the output data changes at falling edge of BCKO clock, so the data input timing to DAC is raising edge of BCKO.

BCKO=8.4672MHz(At $\overline{SCSL}$=H or open of D,E type/F type)

BCKO=8.6436MHz(At $\overline{SCSL}$=L of D,E type)

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(6)OUTPUT DATA FORMAT

The output data format is 2's complement and MSB first.

(7)DEGLITCH SIGNAL

DGL……Lch deglitch signal 176.4kHz(Duty 25%)

DGR……Rch deglitch signal 176.4kHz(Duty 25%)

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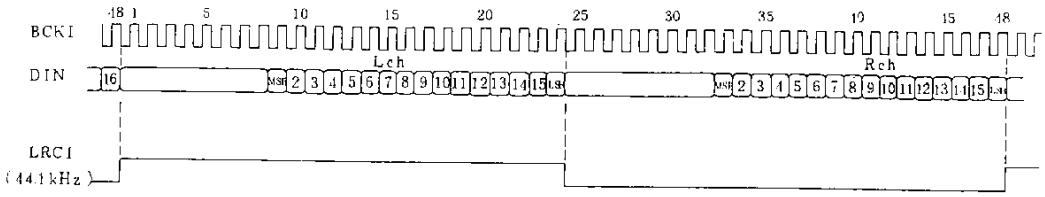
■TIMING CHART

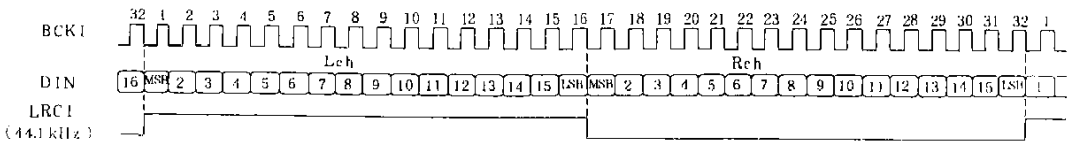
1. INPUT

(1) INPUT TIMING 1 (D, E Type; $\overline{SCSL}$=H or OPEN & F Type)

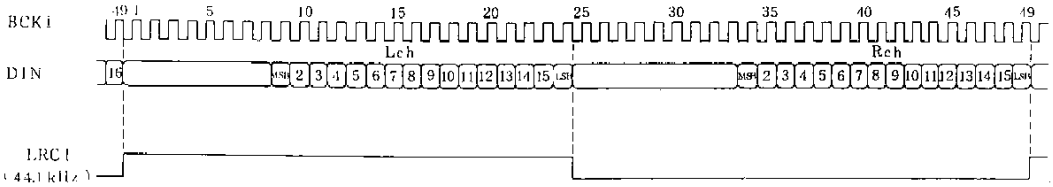
(a)



(b)

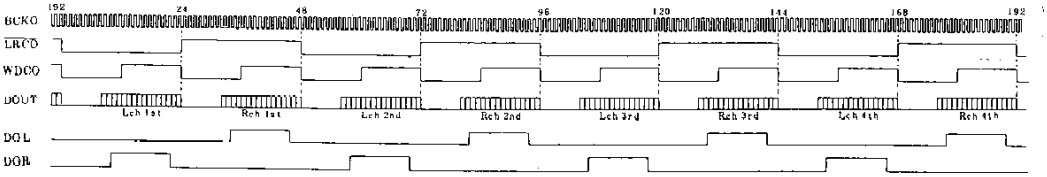


(2) INPUT TIMING 2 (D, E Type; $\overline{SCSL}$=L)

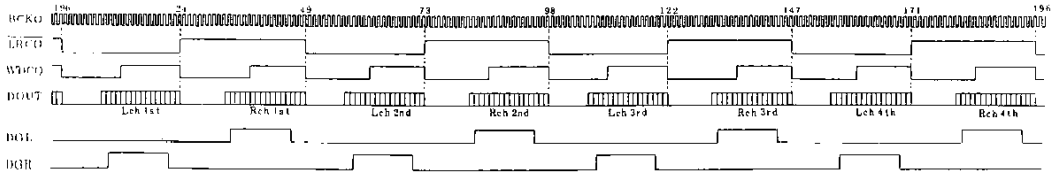


2. OUTPUT

(1) OUTPUT TIMING 1 (D, E Type; $\overline{SCSL}$=H or OPEN & F Type $\overline{SOMD}$=H or OPEN)



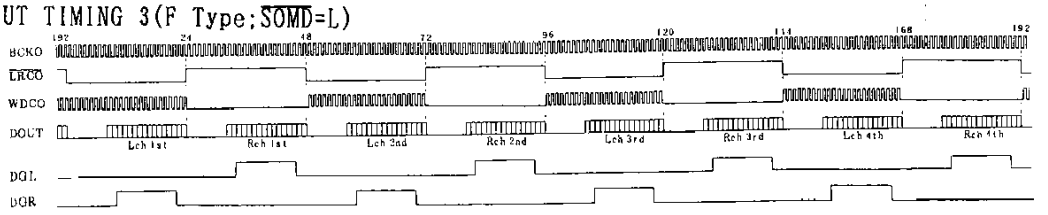
(2) OUTPUT TIMING 2 (D, E Type; $\overline{SCSL}$=L)



The output cycle of WDCO is not constant.

But the DGL, DGR cycles are constant. (176.4kHz, Duty 25%)

(3) OUTPUT TIMING 3 (F Type; $\overline{SOMD}$=L)



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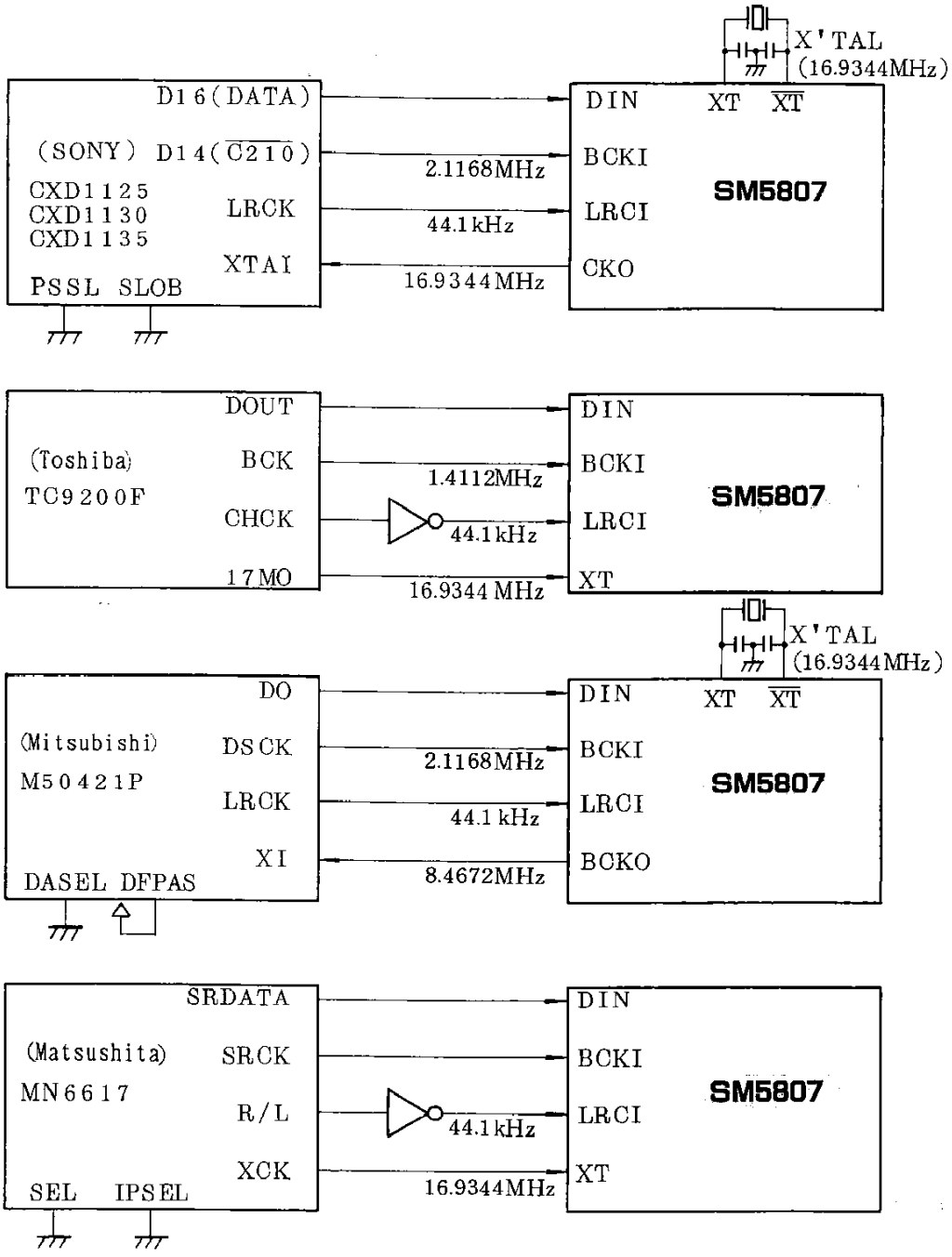
■TYPICAL APPLICATION

1. INPUT



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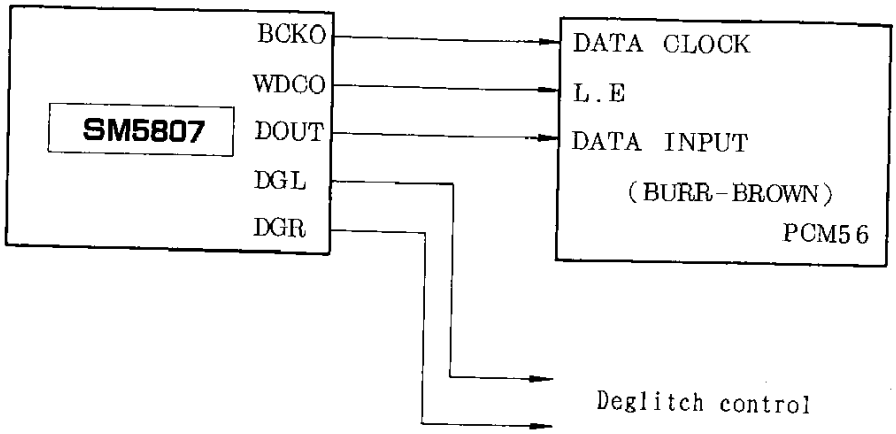
2. OUTPUT

(1)1DAC(D, E Type & F Type;SOMD=H or OPEN)



(2)2DACs(F Type;SOMD=L)