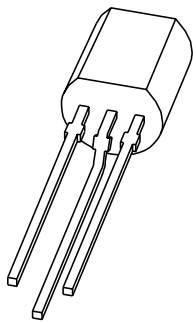


DATA SHEET



BSN304

**N-channel enhancement mode
vertical D-MOS transistor**

Product specification
Supersedes data of 1997 Jun 17

2001 Dec 11

N-channel enhancement mode vertical D-MOS transistor

BSN304

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

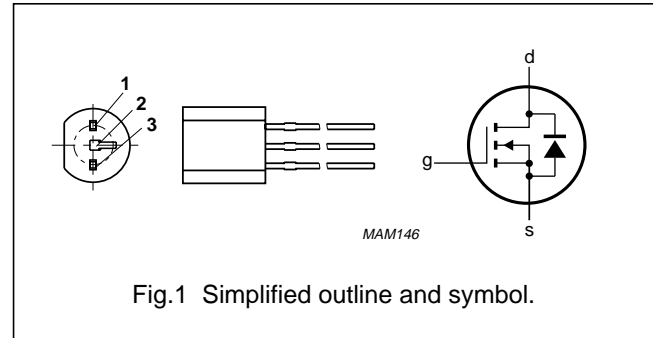
- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	gate
2	drain
3	source



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	300	V
I_D	drain current (DC)		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	1	W
V_{GSO}	gate-source voltage	open drain	–	± 20	V
R_{DSon}	drain-source on-state resistance	$I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	–	6	Ω
V_{GSoff}	gate-source cut-off voltage	$I_D = 1\text{ mA}; V_{GS} = V_{DS}$	0.8	2	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)		–	300	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}; \text{note 1}$	–	1	W
T_{stg}	storage temperature		–55	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–	150	$^{\circ}\text{C}$

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

N-channel enhancement mode vertical D-MOS transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient; note 1	125	K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

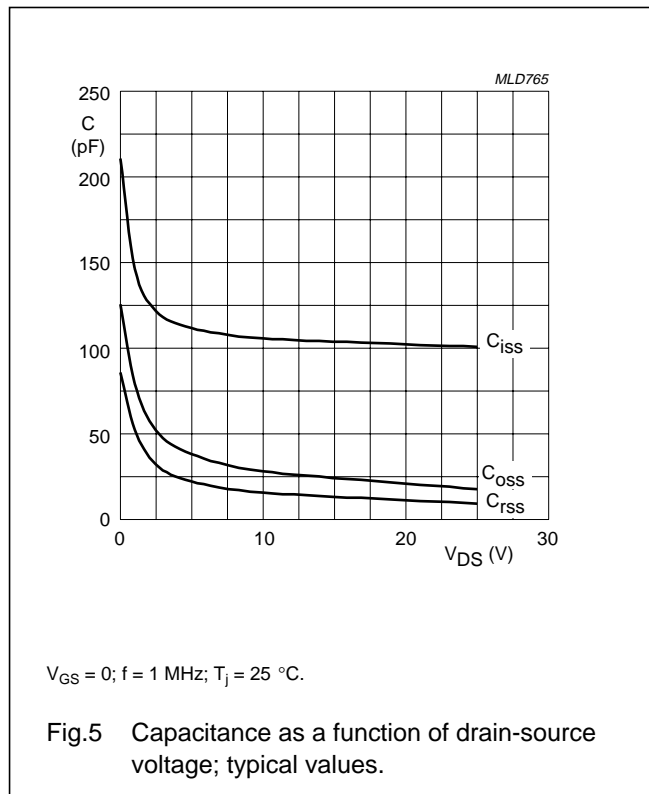
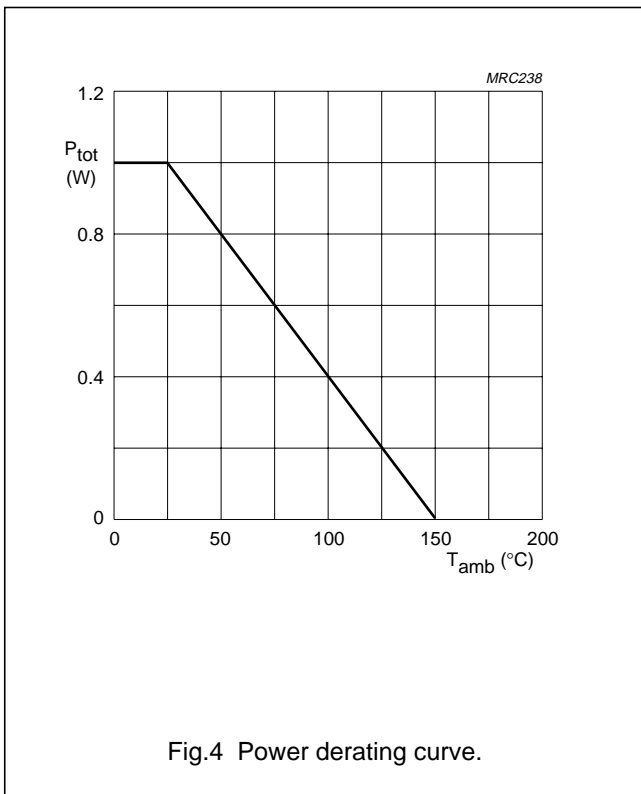
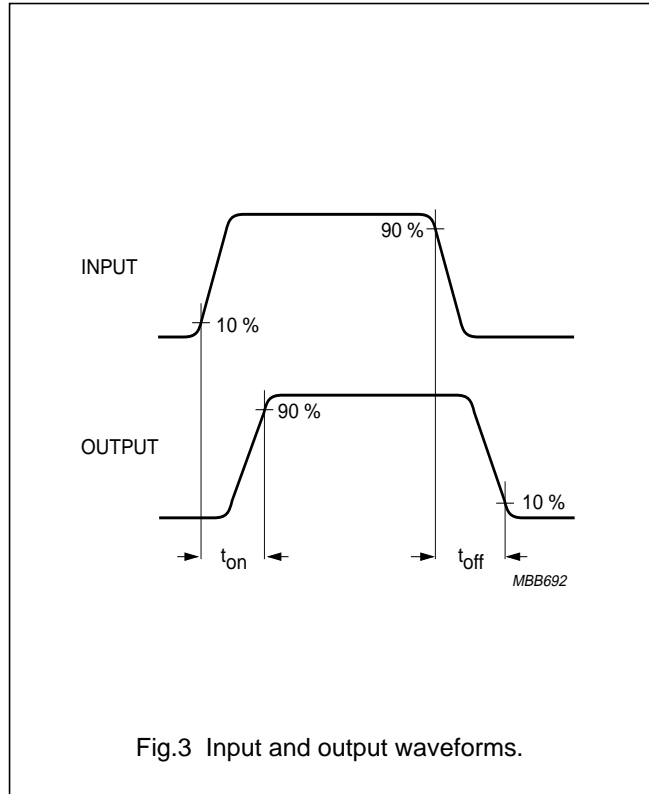
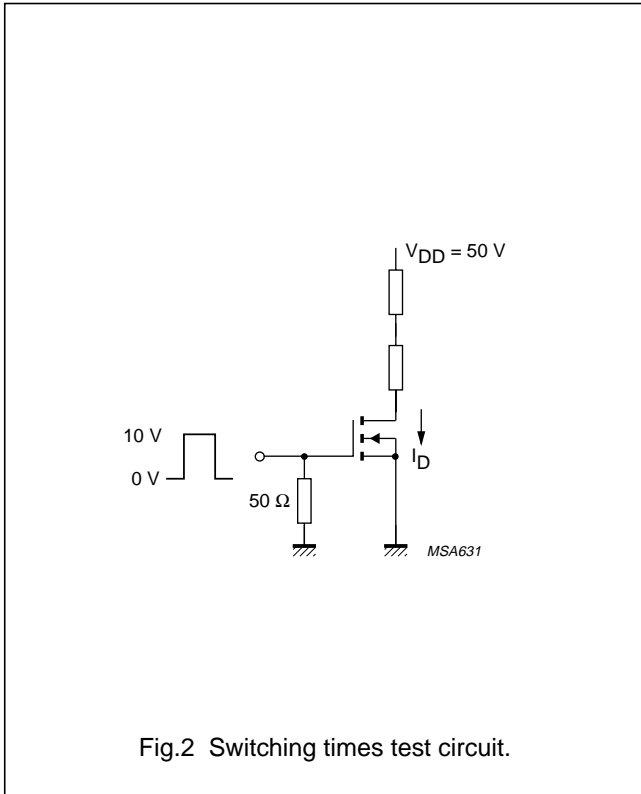
STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}; V_{GS} = 0$	300	–	–	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	± 100	nA
V_{GSth}	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$	0.8	–	2	V
R_{DSon}	drain-source on-state resistance	$I_D = 250\ \text{mA}; V_{GS} = 10\ \text{V}$	–	3.7	6	Ω
		$I_D = 20\ \text{mA}; V_{GS} = 2.4\ \text{V}$	–	4.8	10	Ω
I_{DSS}	drain-source leakage current	$V_{DS} = 240\ \text{V}; V_{GS} = 0$	–	–	100	nA
$ Y_{fs} $	transfer admittance	$I_D = 250\ \text{mA}; V_{DS} = 25\ \text{V}$	200	690	–	mS
C_{iss}	input capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	100	120	pF
C_{oss}	output capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	21	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0;$ $f = 1\ \text{MHz}$	–	10	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V};$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	6	10	ns
t_{off}	turn-off time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V};$ $V_{GS} = 10\ \text{to}\ 0\ \text{V}$	–	46	60	ns

N-channel enhancement mode vertical D-MOS transistor

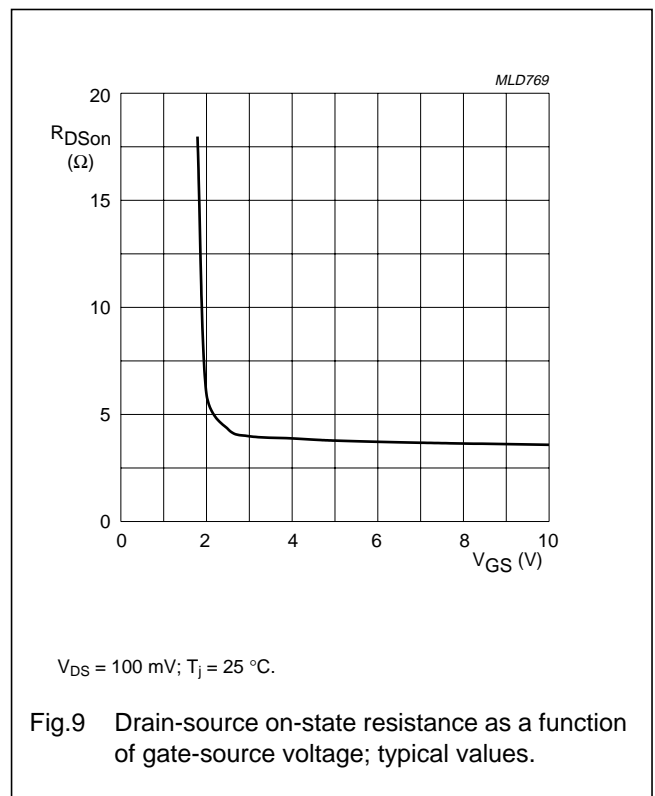
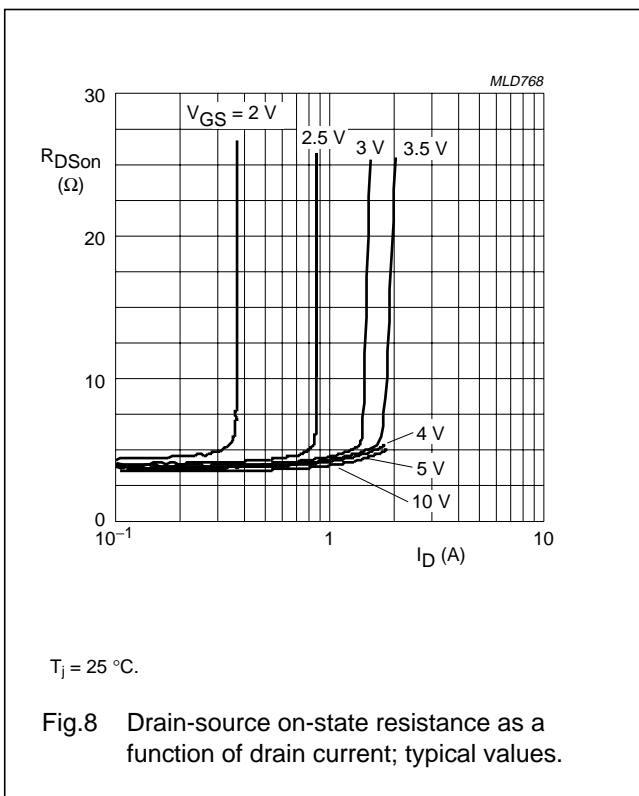
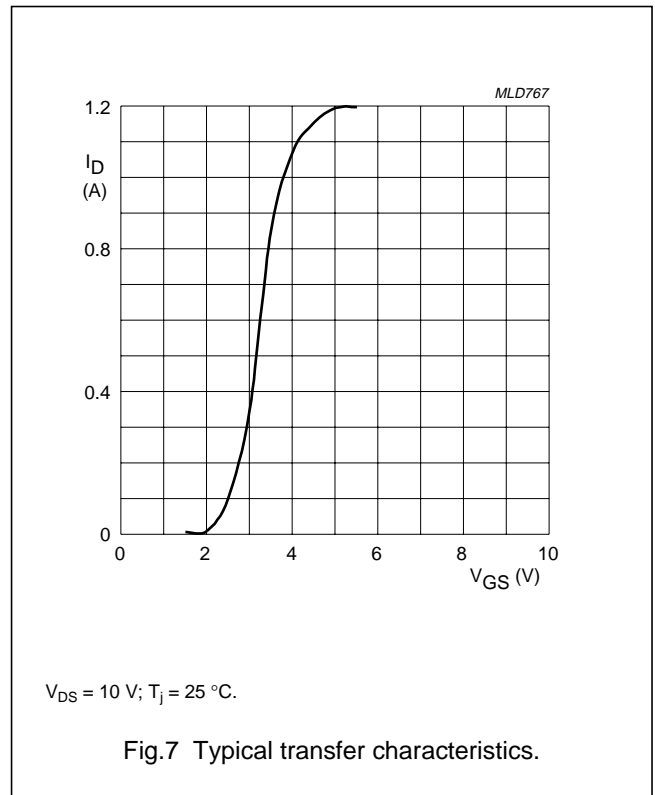
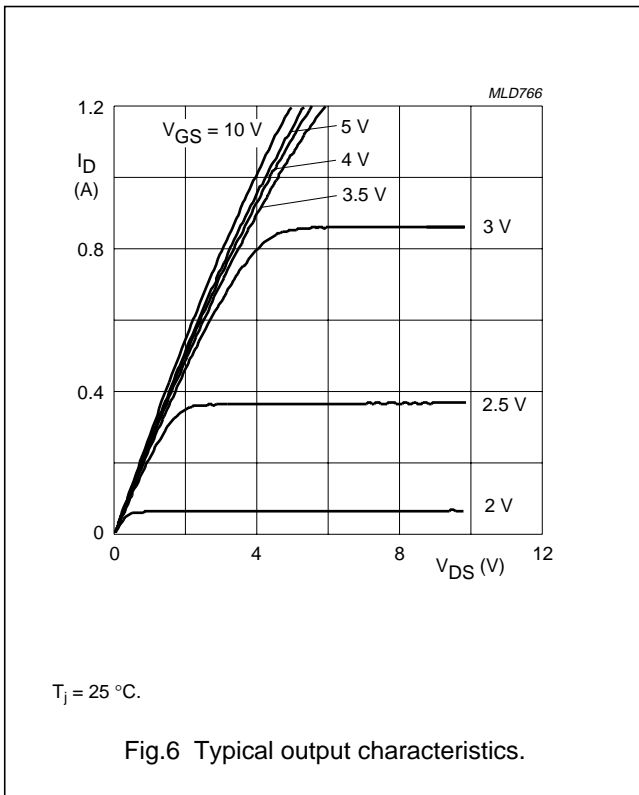
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$V_{GS} = 0$; $f = 1$ MHz; $T_j = 25$ °C.

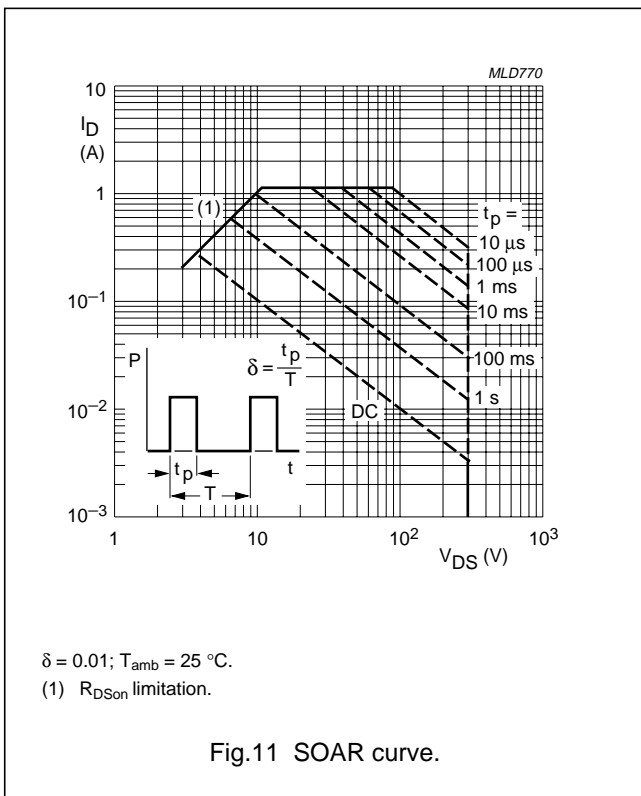
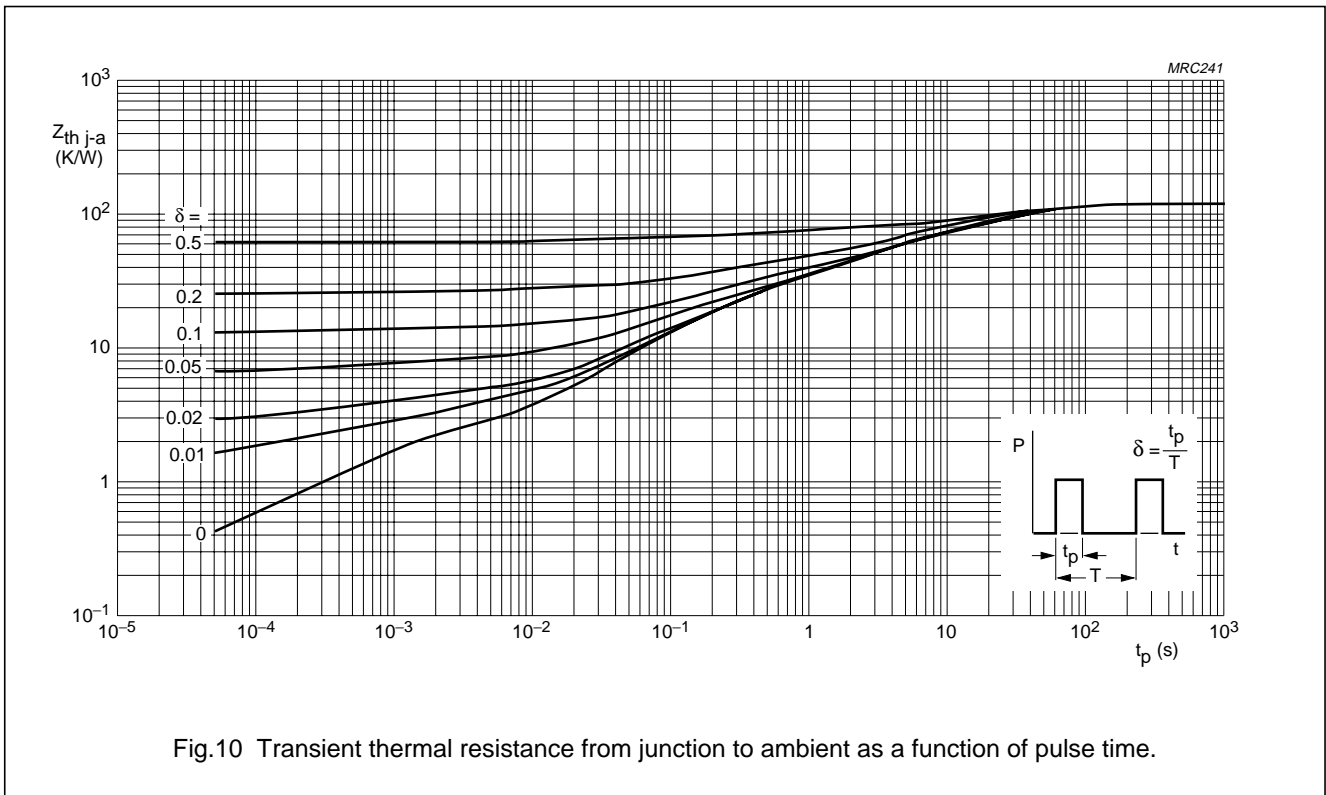
N-channel enhancement mode vertical D-MOS transistor

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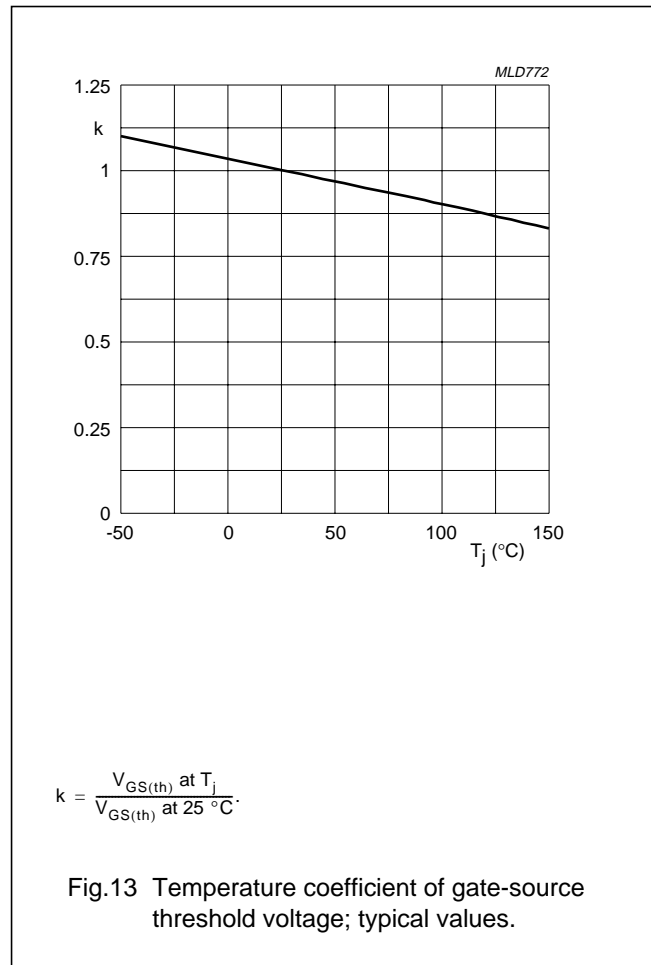
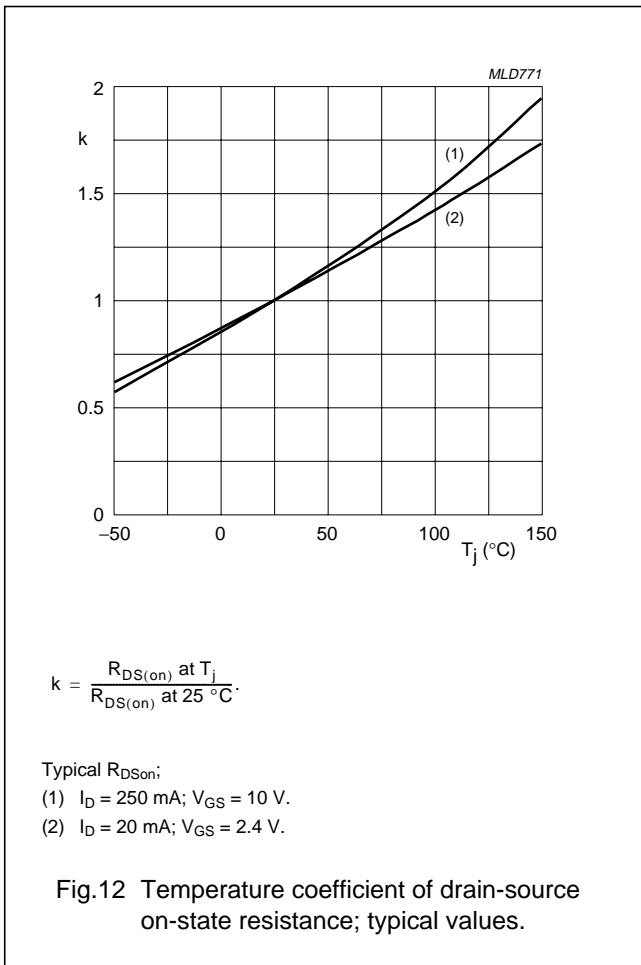
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N-channel enhancement mode vertical D-MOS transistor

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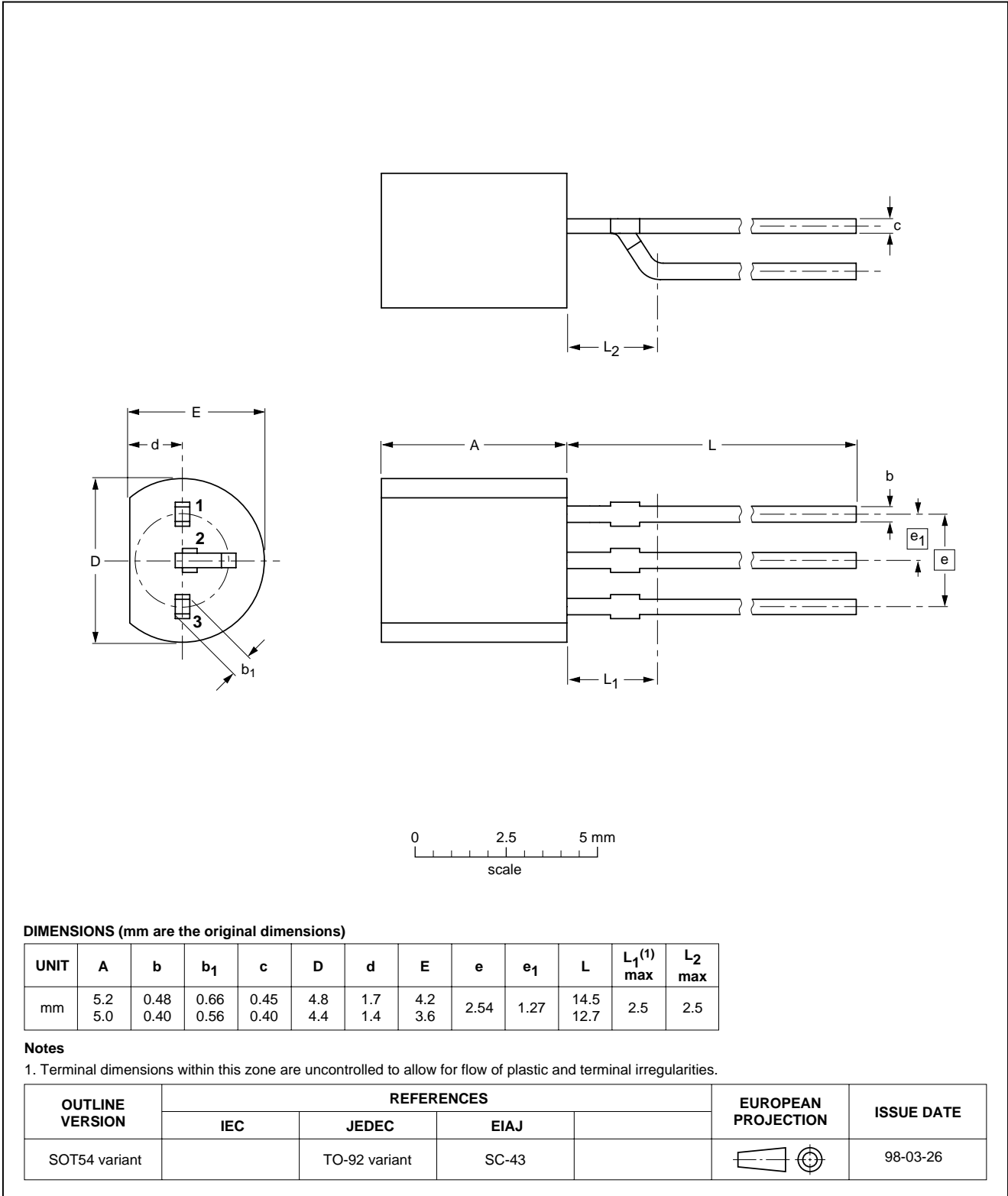
N-channel enhancement mode
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PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



N-channel enhancement mode vertical D-MOS transistor

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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NOTES

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NOTES

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