STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９８９３Ｆ**

FUNCTION
1. 1ch control with Push-Pull
2. Lamp current and voltage sense feed back control
3. Sequencing easily achieved with Soft Start Control
4. Short circuit protection with Timer Latch
5. Under Voltage Lock Out
6. Short circuit protection with over voltage
7. Mode-selectable the operating or stand-by mode by stand-by pin
8. BURST mode controlled by PWM and DC input

○Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	15	V
Operating Temperature Range	Topr	-35～+95	℃
Storage Temperature Range	Tstg	-55～+125	℃
Power Dissipation	Pd	562*	mW
Maximum Junction Temperature	Tjmax	+150	℃

*Pd derated at 4.5mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Recommended operating condition

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	4.5～14.0	V
Drive output frequency	f_{OUT}	20～150	KHz
BCT oscillation frequency	f_{BCT}	0.10～0.50	KHz

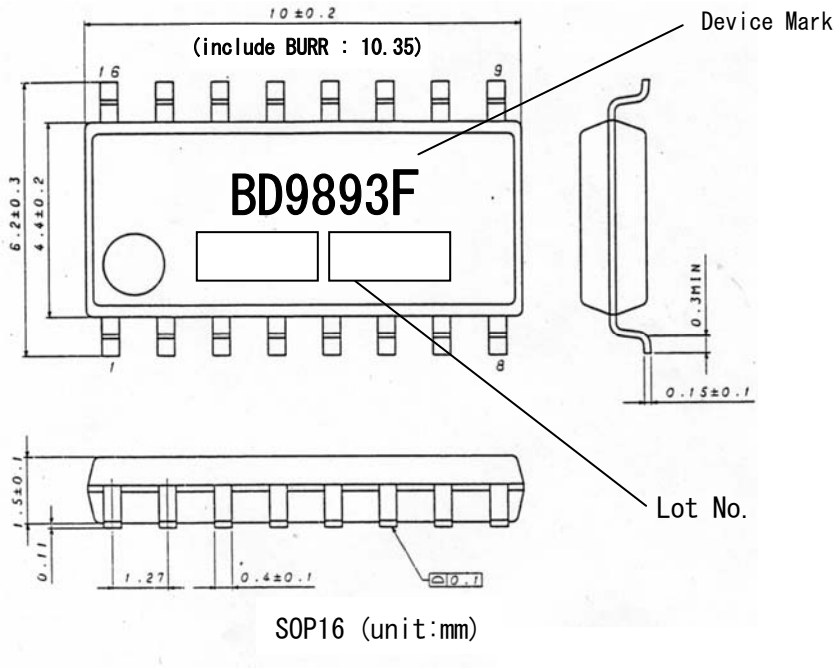
Status of this document
The Japanese version of this document is the official specification.
Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

○Electric Characteristics (Ta=25℃, VCC=7V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOLE DEVICE))						
Operating current	ICC1	—	8	16	mA	
Stand-by current	ICC2	—	2	10	μA	
((OVER VOLTAGE DETECT))						
FB over voltage detect voltage	Vovf	2.20	2.40	2.60	V	
((STAND-BY CONTROL))						
Stand-by voltage H1 (High Active)	VstH1	2.3	—	VCC	V	System ON DUTY pin : 0.5V→2.0V BURST Dimming : 100%→0%
Stand-by voltage H2 (Low Active)	VstH2	1.4	—	2.1	V	System ON DUTY pin : 0.5V→2.0V BURST Dimming : 0%→100%
Stand-by voltage L	VstL	-0.3	—	0.8	V	System OFF
((TIMER LATCH))						
Timer Latch voltage	VSCP	1.9	2.0	2.1	V	
Timer Latch current	ISCP	0.5	1.0	1.5	μA	
((OSC BLOCK))						
Active edge Current	Iact	1.25/RT	1.5/RT	1.75/RT	A	
MAX DUTY	MAXDUTY	44	46.4	49	%	fOUT=60kHz
Soft start current	Iss	1.0	2.0	3.0	μA	
IS COMP detect Voltage	Visc	0.45	0.50	0.55	V	
SS COMP detect voltage	Vss	2.0	2.2	2.4	V	
SRT ON resistance	RSRT	—	200	400	Ω	
((UVLO BLOCK))						
Operating voltage	VuvloH	4.13	4.30	4.47	V	
Shut down voltage	VuvloL	3.94	4.10	4.26	V	
((FEED BACK BLOCK))						
IS threshold voltage	Vis	1.225	1.250	1.275	V	
VS threshold voltage	Vvs	1.220	1.250	1.280	V	
IS source current 1	Iis1	—	—	1.5	μA	DUTY=2.0V
IS source current 2	Iis2	13.0	20.0	27.0	μA	DUTY=0V、IS=0.5V
VS source current	Ivs	—	—	1.0	μA	
((Output BLOCK))						
N1ch output voltage H	VoutN1H	VCC-0.3	VCC-0.1		V	
N2ch output voltage H	VoutN2H	VCC-0.3	VCC-0.1	—	V	
N1ch output voltage L	VoutN1L	—	0.1	0.3	V	
N2ch output voltage L	VoutN2L	—	0.1	0.3	V	
N1ch sink resistance	RsinkN1	—	4	8	Ω	Isink = 10mA
N1ch source resistance	RsourceN1	—	7	14	Ω	Isource = 10mA
N2ch sink resistance	RsinkN2	—	4	8	Ω	Isink = 10mA
N2ch source resistance	RsourceN2	—	7	14	Ω	Isource = 10mA
Drive output frequency	FOUT	58.5	60.0	61.5	kHz	RT=29.2kΩ
((BURST MODE))						
BOSC Max voltage	VburH	1.94	2.0	2.06	V	fBCT=0.2kHz
BOSC Min Voltage	VburL	0.4	0.5	0.6	V	fBCT=0.2kHz
BOSC frequency	FBOSC	252.2	260	267.8	Hz	BCT=4642OpF
((COMP BLOCK))						
Over voltage detect	VCOMPH	1.92	2.00	2.08	V	
Under voltage detect	VCOMPL	0.96	1.00	1.04	V	
Hysteresis width	⊿VCOMP	—	0.1	0.15	V	

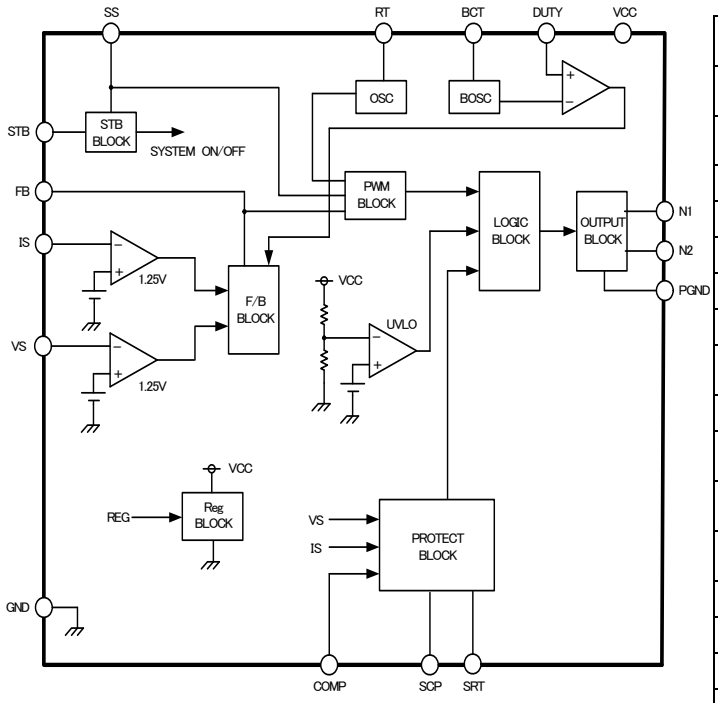
(This product is not designed for normal operation with in a radio active environment.)

○Package Dimensions



SOP16 (unit:mm)

○Block Diagram



○Pin Description

Pin No.	Pin Name	Function
1	RT	External resistor from RT to GND for adjusting the internal triangle oscillator
2	SRT	External resistor from SRT to RT for adjusting the internal triangle oscillator
3	FB	Error amplifier output
4	IS	Error amplifier input①
5	VS	Error amplifier input②
6	GND	GROUND
7	DUTY	Control PWM mode and BURST mode
8	BCT	External capacitor from BCT to GND for adjusting the BURST triangle oscillator
9	COMP	Under, over voltage detect
10	SCP	External capacitor from SCP to GND for Timer Latch
11	SS	External capacitor from SS to GND for Soft Start Control
12	STB	Stand-by switch Select the BURST dimming direction
13	N2	FET driver
14	PGND	Ground for FET drivers
15	N1	FET driver
16	VCC	Supply voltage input

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and the IC.Use adequate margins for steady state and transient characteristics.
2. Recommended Operating Range
   The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin
6. The BD9893F incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9893F are changed to 3 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～1.4V, 2.1～2.3V).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig-1)has P^+ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,
    ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
    ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

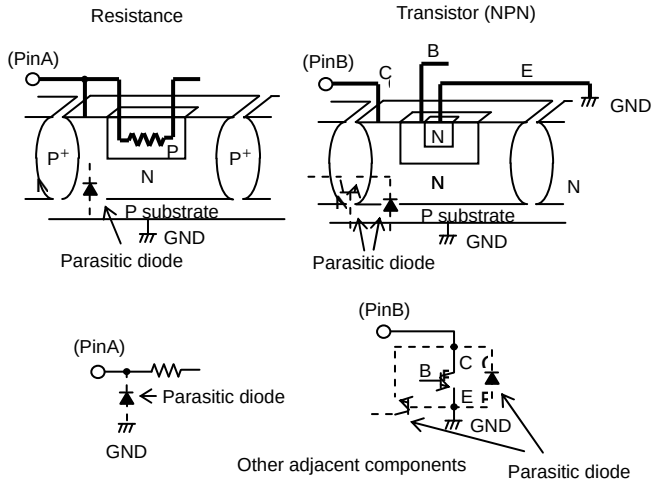


Fig-1 Simplified structure of a Bipolar IC

Notes

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