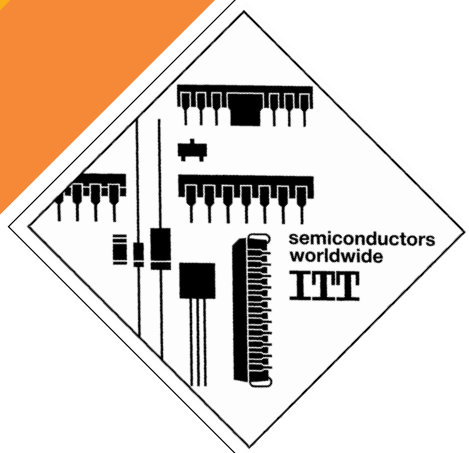

DPU 2553, DPU 2554
Deflection Processors

Edition May 8, 1992
6251-329-2E

ITT Semiconductors

Contents

Deflection Processors

Note: If not otherwise designated, the pin numbers mentioned refer to the 40–pin Dil package.

1. Introduction

These programmable VLSI circuits in N–channel MOS technology carry out the deflection functions in digital color TV receivers based on the DIGIT 2000 system and are also suitable for text and D2–MAC application. The three types are basically identical, but are modified according to the intended application:

DPU 2553

normal–scan horizontal deflection, standard CTV receivers, also equipped with Teletext and D2–MAC facility

DPU 2554

double–scan horizontal deflection, for CTV receivers equipped with double–frequency horizontal deflection and double–frequency vertical deflection for improved picture quality. At power–up, this version starts with double horizontal frequency.

1.1. General Description

The DPU 2553/54 Deflection Processors contain the following circuit functions on one single silicon chip:

- video clamping
- horizontal and vertical sync separation
- horizontal synchronization
- normal horizontal deflection
- east–west correction, also for flat–screen picture tubes
- vertical synchronization
- normal vertical deflection
- sawtooth generation
- text display mode with increased deflection frequencies (18.7 kHz horizontal and 60 Hz vertical)
- D2–MAC operation mode

and for DPU 2554 only:

- double–scan horizontal deflection
- normal and double–scan vertical deflection

In this data sheet, all information given for double–scan mode is available with the DPU 2554 only. Type DPU 2553 starts the horizontal deflection with 15.5 kHz according to the normal TV standard, whereas type DPU 2554 starts with 31 kHz according to the double–scan system.

The following characteristics are programmable:

- selection of the TV standard (PAL, D2–MAC or NTSC)
- selection of the deflection standard (Teletext, horizontal and vertical double–scan, and normal scan)
- filter time–constant for horizontal synchronization
- vertical amplitude, S correction, and vertical position for in–line, flat–screen and Trinitron picture tubes
- east–west parabola, horizontal width, and trapezoidal correction for in–line, flat–screen and Trinitron picture tubes
- switchover characteristics between the different synchronization modes
- characteristic of the synchronism detector for PLL switching and muting

1.2. Environment

Fig. 1–1 shows the simplified block diagram of the video and deflection section of a digital TV receiver based on the DIGIT 2000 system. The analog video signal derived from the video detector is digitized in the VCU 2133, VCU 2134 or VCU 2136 Video Codec and supplied in a parallel 7 bit Gray code. This digital video signal is fed to the video section (PVPU, CVPU, SPU and DMA) and to the DPU 2553/54 Deflection Processor which carries out all functions required in conjunction with deflection, from sync separation to the control of the deflection power stages, as described in this data sheet.

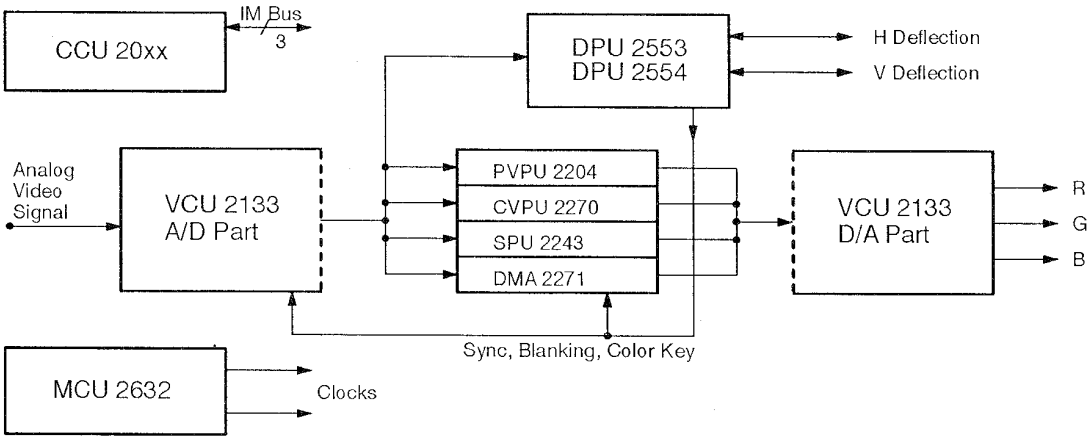

Fig. 1–1: Block diagram of the video and deflection section of a digital TV receiver according to the DIGIT 2000 concept

2. Specifications

2.1. Outline Dimensions

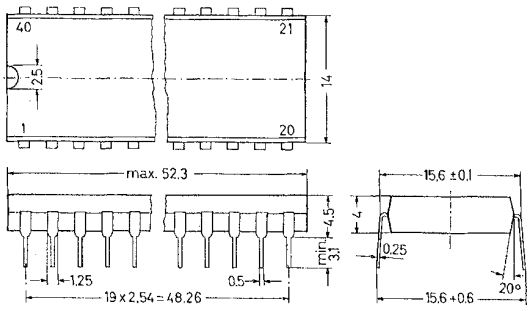

Fig. 2–1: DPU 2553 and DPU 2554 in 40–pin Dil plastic package, 20 B 40 according to DIN 41 870

Weight approx. 6 g, Dimensions in mm

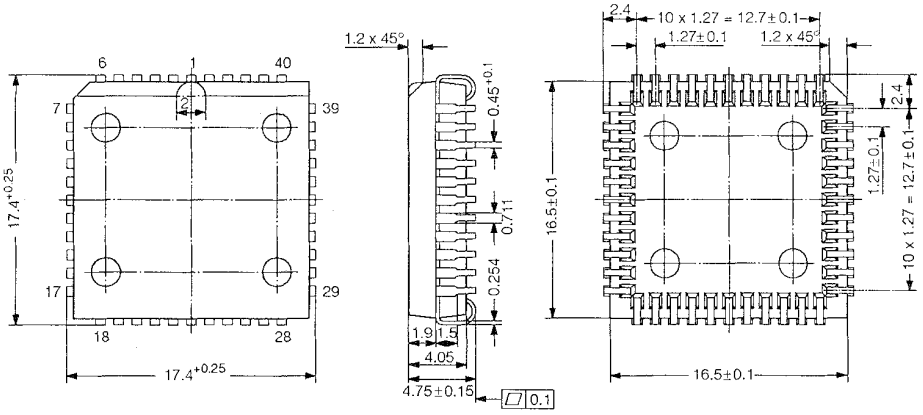

Fig. 2–2: DPU 2553 and DPU 2554 in 44–pin PLCC Package,

Weight approx. 2.2 g, Dimensions in mm

2.2. Pin Connections

2.2.1. 40–Pin Dil Package

1	Leave Vacant
2	ΦM Main Clock Input
3	Output for Single–Scan Vertical Blanking Pulse
4	Clamping Output 2
5	$\overline{\text{Reset}}$ Input
6	Input for the D2–MAC Composite Sync Signal and Output for the Separated Composite Sync Signal
7	1H and 2H Skew Data Output
8	Leave Vacant
9	V6 Video Input (MSB)
10	V5 Video Input
11	V4 Video Input
12	V3 Video Input
13	V2 Video Input
14	V1 Video Input
15	V0 Video Input (LSB)

16 IM Bus Clock Input

17 IM Bus Ident Input

18 IM Bus Data Input/Output

19 Combined Output for the Color Key Pulse and the Undelayed Horizontal Blanking Pulse

20 HSP Status Output

21 Clamping Output 1

22 Combined Output for the Delayed Horizontal Blanking Pulse and the Vertical Blanking Pulse

23 Horizontal Flyback Input

24 Undelayed Horizontal Blanking Output

25 Vertical Flyback Safety Input

26 Vertical Flyback Output

27 Vertical Sawtooth Output

28 East–West Parabola Output

29 Horizontal Output Polarity Select Input and Start Oscillator Pulsewidth Select Input

30 Ground

31 Horizontal Output

32 V_{SUP} Supply Voltage

33 External Standard Selection Input

34 Start Oscillator Clock Input

35 Start Oscillator Supply Voltage

36 Start Oscillator Select Input

37 Control Switch Output for the Horizontal Power Stage

38 Test Pin, leave vacant

39 Interlace Control Output

40 Leave Vacant

2.2.2. 44–Pin PLCC Package

1 Leave Vacant

2 Clamping Output 1

3 Vertical Blanking & Delayed Horizontal Blanking Pulse Output

4 Horizontal Flyback Input

5 Undelayed Horizontal Blanking Pulse Output

6 Vertical Flyback Safety Input

7 Vertical Flyback Output

8 Vertical Sawtooth Output

9 East/West Parabola Output

10 Horizontal Output Polarity & Pulsewidth Select Input

11 Ground

12 Ground

13 Horizontal Output

14 V_{SUP}

15 External Standard Selection Input

16 Start Oscillator Clock Input

17 V_{SUP} (Start Oscillator)

18 Start Oscillator Select Input

19 Horizontal Power Stage Control Switch Output

20 Leave Vacant (Test Pin)

21 Interlace Control Output

22 Leave Vacant

23 Leave Vacant

24 Leave Vacant

25 ΦM Main Clock Input

26 Single–Scan Vertical Blanking Pulse Output

27 Clamping Output 2

28 $\overline{\text{Reset}}$ Input

29 Input for the D2–MAC Composite Sync Signal and Output for the Separated Composite Sync Signal

30 1H and 2H Skew data Output

31 Leave Vacant

32 V6 Video Input (MSB)

33 V5 Video Input

34 V4 Video Input

35 V3 Video Input

36 V2 Video Input

37 V1 Video Input

38 V0 Video Input (LSB)

39 IM Bus Clock Input

40 Substrate

41 IM Bus Ident input

42 IM Bus Data Input/Output

43 Undelayed Horizontal Blanking & Color Key Pulse Output

44 HSP Status Output

2.3. Pin Descriptions (pin numbers for 40–pin DIL package)

Pin 30 – Ground
This pin must be connected to the negative of the supply.

Pin 2 – ΦM Main Clock Input (Fig. 2–5)
By means of this input, the DPU receives the required main clock signal from the MCU 2600 or MCU 2632 Clock Generator IC.

Pin 3 – Single–Scan Vertical Blanking Output (Fig. 2–12)
In vertical double–scan mode, this pulse is also required by the CVPU 2270 Comb Filter Video Processor.

Pins 4 and 21 – Clamping Outputs 2 and 1 (Fig. 2–11)
These pins supply pulses for clamping the video signal at the VCU 2133, VCU 2134 or VCU 2136 during the back porch.

Pin 5 – $\overline{\text{Reset}}$ Input (Fig. 2–3)
This pin is used for hardware reset. At low level, reset is actuated, and at high level the DPU is ready for communication with the CCU via the IM bus.

Pin 6 – Input for the D2–MAC composite Sync Signal and Output for the Separated Composite Sync Signal
This pin (Fig. 2–10) is the input for the D2–MAC composite sync signal and the output for the separated composite sync signal.

Pin 7 – Skew Data Output (Fig. 2–12)
This pin delivers the 1H and 2H skew data stream required by the PSP 2210 Progressive Scan Processor and the TPU 2735 or TPU 2740 Teletext Processor or others for adjusting the phase of the double–scan video signal and for information about vertical sync.

Pin 32 – V_{SUP} Supply Voltage
This pin must be connected to the positive of the supply.

Pins 9 to 15 – V6 to V0 Video Inputs (Fig. 2–4)
Via these pins, the DPU receives the digitized composite video signal from the VCU 2133, VCU 2134 or VCU 2136 Video Codec in a parallel 7–bit Gray code. With a standard signal, the sync pulse resolution is 6 bits.

Pins 16 to 18 – IM Bus Connections
These pins connect the DPU to the IM bus. It is via the IM bus that the DPU communicates with the CCU. Pins 16 (IM Bus Clock Input) and 17 (IM Bus Ident Input) have the configuration shown in Fig. 2–3. Pin 18 (IM Bus Data Input/Output) is shown in Fig. 2–10.

Pin 19 – Combined Output for the Color Key Pulse and the Undelayed Horizontal Blanking Pulse (Fig. 2–12)
This output is tristate–controlled. In conjunction with the input load represented by the VCU, the three–level key and blanking pulse is produced which is also needed by the other DIGIT 2000 processors.

Pin 20 – HSP Status Output (Fig. 2–13)
This output supplies a HSP status signal. If this pin is low, a malfunction of the internal HSP–processor is indicated, which may be caused by power or clock problems. This output will stay low until two hardware or software resets of the DPU occur.

Pin 22 – Combined Output for the Delayed Horizontal Blanking Pulse and the Vertical Blanking Pulse (Fig. 2–12)
This pin is a tristate–controlled output. In conjunction with the input load represented by the VCU, the three–level combined blanking pulse is produced which is also needed by the other DIGIT 2000 processors.

Pin 23 – Horizontal Flyback Input (Fig. 2–6)
Pin 23 requires horizontal flyback pulses which must be clamped by a diode to the +5 V supply.

Pin 24 – Undelayed Horizontal Blanking Output (Fig. 2–12)
This output supplies undelayed horizontal blanking pulses. These pulses are for keying of the IF amplifier and are keying pulses for the VCU.

Pin 25 – Vertical Flyback Safety Input (Fig. 2–6)
To protect the picture tube from damage by burn–in in the event of a malfunction of the vertical deflection, an acknowledge pulse derived from the vertical deflection yoke is fed to pin 25. If this pulse exceeds the 2.5 V threshold during vertical blanking, the blanking pulse will be terminated. If it is planned to operate without this picture tube protection, pin 25 must be connected to +5 V.

Pin 26 – Vertical Flyback Output (Fig. 2–14)
This pin supplies the same pulsewidth–modulated sawtooth signal as pin 27, but only for 350 µs from the start of the vertical flyback. During the remaining time, pin 26 is used for fast charge–reversal of the integration capacitor.

Pin 27 – Vertical Sawtooth Output (Fig. 2–14)
This pin supplies the signal, in pulsewidth–modulated form, for driving the vertical output stage. To produce the analog sawtooth signal, this signal must be integrated externally, e.g. by an RC network. By way of the IM bus interface and the HSP processor, it is possible for this sawtooth to be varied by the CCU.

Pin 28 – East–West Parabola Output (Fig. 2–14)
This pin supplies the vertical–frequency parabola signal for the east–west correction in pulsewidth–modulated form. Via the IM bus and the HSP processor, the east–west parabola can be adjusted by the CCU.

Pin 29 – Horizontal Output Polarity and Pulsewidth Select Input (Fig. 2–7)
This pin serves for selecting the polarity and the pulsewidth of the output pulses of pin 31 as described in section 3.4. This pin must be connected to ground or to +5 V.

Pin 31 – Horizontal Output (Fig. 2–11)
This output supplies the driving pulses for the horizontal output stage. The output pulse polarity can be selected by means of pin 29.

Pin 33 – External Standard Selection Input (Fig. 2–8)
This input is used for selecting the horizontal frequency standard, as shown in Table 3–3. If pin 33 is +5 V, the DPU operates only with the NTSC standard. If it is connected to ground, however, the DPU is set for the PAL or SECAM standard, and the horizontal standard can only be changed by the CCU command between PAL/SECAM and text display mode. If pin 33 is unconnected, all standards can be selected by the CCU via the IM bus. Furthermore, when pin 33 is unconnected, the horizontal protection circuit6 is in effect, and for this a 4 MHz signal is required at pin 34. In this case, the output pulse at pin 31 is limited to a maximum duration of 30 µs for all standards. The phase resolution of the trailing edge of this pulse is reduced to 250 ns, if the output pulse is set to more than 30 µs pulsewidth.

Pin 34 – Protection Circuit Clock Input (Fig. 2–9)
When pin 33 is left unconnected, a 4 MHz clock signal is required at pin 34 for the horizontal protection circuit. The 4 MHz clock can be fed to pin 34 via a capacitor, and is available, e.g., at pin 1 of the CCU at no added cost. If the 4 MHz signal is not present and pin 33 is not connected, the horizontal output pin 31 is undefined.

Pin 35 – Start Oscillator Supply
Via this pin it is possible with minimum current consumption to operate the horizontal protection circuit as a starting oscillator. For this purpose only the 4 MHz signal at pin 34 is required. Pin 36 must be connected to pin 35.

Pin 36 – Start Oscillator Select Input (Fig. 2–7)
If the start oscillator function is required (see Table 3–3), pin 36 must be connected to pin 35. If the start oscillator function is not used, pin 36 has to be connected to ground. In this mode, the horizontal output pin 31 is switched off (at high level) as long as the $\overline{\text{Reset}}$ input pin 5 is Low.

Pin 37 – Control Switch Output for the Horizontal Power Stage (Fig. 2–12)
This pin serves for switching over the horizontal output stage to another frequency.

Pin 38 – Test pin
This pin is an input/output of the type shown in Fig. 2–10. It i used for testing the DPU during production and should be left unconnected in normal operation.

Pin 39 – Interlace Control Output (Fig. 2–11)
This pin is for controlling an AC coupled vertical power stage for interlace–free mode (with DPU 2553) and for AC and DC coupled vertical power stage for the three interlace modes with the VMC–Processor

2.4. Pin Circuits (pin numbers for 40–pin DIL package)

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter " E " means enhancement, the letter " D " depletion, and " S " stands for signal.

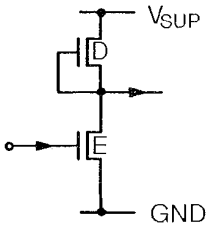

Fig. 2–3:
Input Pins 5, 16 and 17

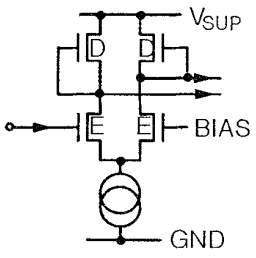

Fig. 2–4:
Input Pins 9 to 15

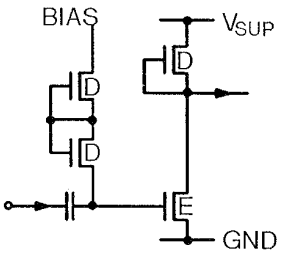

Fig. 2–5:
Input Pin 2

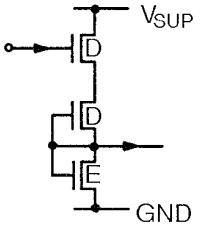

Fig. 2–6:
Input Pins 23 and 25

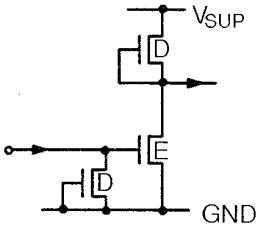

Fig. 2–7:
Input Pins 29 and 36

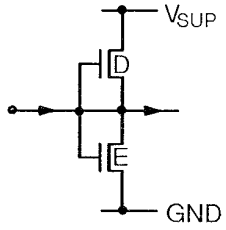

Fig. 2–8:
Input Pin 33

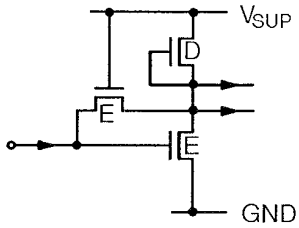

Fig. 2–9:
Input Pin 34

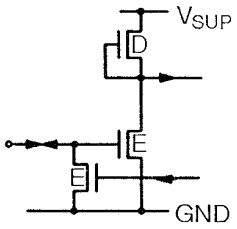

Fig. 2–10:
Input/Output Pins 6, 18 and 38

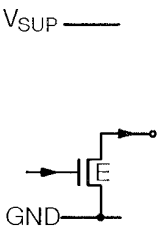

Fig. 2–11:
Output Pins 4, 21, 31 and 39

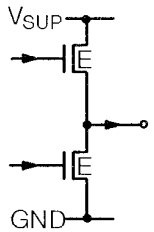

Fig. 2–12:
Output Pins 3, 7, 19, 22, 24 and 37

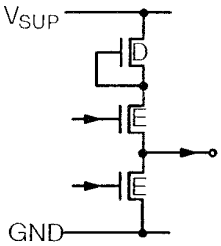

Fig. 2–13:
Output Pin 20

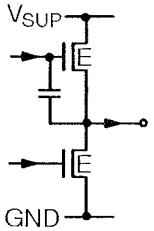

Fig. 2–14:
Output Pins 26 to 28

2.5. Electrical Characteristics (pin numbers for 40–pin DIL package)

All voltages are referred to ground.

2.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	32	–	6	V
V_I	Input Voltage, all Inputs	–	–0.3 V	V_{SUP} + 0.3 V	–
V_O	Output Voltage	3, 6, 7, 18, 19, 22, 24, 26 to 28, 37, 38	–0.3 V	V_{SUP} + 0.3 V	–
V_O	Output Voltage	4, 21	–0.3	+9	V
V_O	Output Voltage	31, 39	–0.3	+11	V
I_O	Output Current	4, 18, 21, 39	–	10	mA
I_O	Output Current	20	–	1	mA
I_O	Output Current	31	–	50	mA
I_O	Output Current	3, 6, 7, 19, 22, 24, 26 to 28, 37, 38	–	*)	–

*) These outputs are short,circuit proof with respect to supply and ground

2.5.2. Recommended Operating Conditions at T_A = 0 to 65 °C, $f_{\Phi M}$ = 14.3 to 20.5 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	32	4.75	5.0	5.25	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage	2	1.5	–	3.5	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage (p–p)		0.8	–	2.5	V
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	ΦM Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi MIHL}$	ΦM Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi D}}$	–
$t_{\Phi MILH}$	ΦM Clock Input Low to High Transition Time		–	–	$\frac{0.15}{f_{\Phi D}}$	–
V_{VIL}	Video Input Low Voltage	9 to 15	–	–	$0.5 \cdot V_{SUP}$ + 0.3 V	–
V_{VIH}	Video Input High Voltage		$0.5 \cdot V_{SUP}$ + 0.3 V	–	–	–
$t_{\Phi VIH}$	Video Input Setup Time after ΦM Clock Input	9 to 15, 2	8	–	–	ns
$t_{VIS\Phi}$	Video Input Setup Time before ΦM Clock Input		8	–	–	ns
V_{REIL}	Reset Input Low Voltage	5	–	–	1.2	V
V_{REIH}	Reset Input High Voltage		2.4	–	–	V
V_{D2IL}	D2–MAC Sync Input Low Voltage	6	–	–	0.8	V
V_{D2IH}	D2–MAC Sync Input High Voltage		2.4	–	–	V
V_{IMIL}	IM Bus Input Low Voltage	16 to 18	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	170	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM6}	ΦI Clock Input Hold Time before Ident End–Pulse Input	16 to 18	6.0	–	–	µs
t_{IM7}	IM Bus Data Input Delay Time after ΦI Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End–Pulse Low Time		3.0	–	–	µs
V_{HFIL}	Horizontal Flyback Input Low Voltage	23	–	–	0.8	V
V_{HFIH}	Horizontal Flyback Input High Voltage		3.2*)	–	–	V
V_{VFSIL}	Vertical Flyback Safety Input Low Voltage	25	–	–	1.5	V
V_{VFSIH}	Vertical Flyback Safety Input High Voltage		3.5	–	–	V
V_{SIL}	Select Input Low Voltage	29, 33, 36	–	–	0.8	V
V_{SIH}	Select Input High Voltage		2.4	–	–	V
V_{SOCI}	Start Oscillator Clock Input Voltage (p–p), A.C. Coupled	34	0.5	–	–	V
f_{SOC}	Start Oscillator Clock Frequency		–	–	–	MHz

*) Pin 23 must be clamped to the +5 V supply by means of a diode (anode of the diode to pin 23).

2.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, $f_{\Phi M}$ = 14.3 to 20.5 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	32	–	160	205	mA	
I_{SUP}	Supply Current	35	–	2.5	5	mA	
V_{IMOL}	IM Bus Output Low Voltage	18	–	–	0.4	V	I_{IMO} = 3 mA
I_{IMOH}	IM Bus Output High Current		–	–	10	µA	V_{IMO} = 5 V
Clamping Circuit and Pulse Separation Values referred to an analog composite video signal of 2 V (p–p), whose potential is between 5 and 7 V at pin 37 of the VCU 2133, VCU 2134 or VCU 2136 Video Codec (see Fig. 3–2)							
V_{CL}	Clamping Level of the Sync Pulse Top	–	–	5.125	–	V	non–synchronized horizontal deflection
V_{BPC}	Back Porch Clamping Level	–	–	5.5	–	V	synchronized horizontal deflection

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{SPSNS}	Sync Pulse Separation Level	–	–	5.25	–	V	non–synchronized horizontal deflection
V_{SPSS}	Sync Pulse Separation Level	–	50 % of the sync pulse amplit.			–	synchronized horizontal deflection
t_{CPD}	Clamping Pulse Duration	4, 21	–	0.86	–	µs	
R_{CLON}	Clamping Pulse Output ON Resistance		–	–	150	Ω	I_{CLO} = 5 mA
I_{CLOFF}	Clamping Pulse Output OFF Current		–	–	10	µA	V_{CLO} = 8 V
t_{CPPH}	Clamping Pulse Phase Position	4, 21 9 to 15	–	6.49	–	µs	referred to the center of the sync pulse in the input video signal
f_{cor}	Corner Frequency of the Digital Lowpass Filter Following the Video Inputs V0 to V6	9 to 15	–	1	–	MHz	
Horizontal Synchronization							
t_{HO}	Horizontal Output Pulse Duration	31	1	–	63	µs	variable in steps of 1 µs
R_{HOON}	Horizontal Output ON Resistance		–	–	40	Ω	I_{HO} = 10 mA
I_{HOOF}	Horizontal Output OFF Current		–	–	10	µA	V_{HO} = 10 V
V_{CSOL}	Control Switch Output Low Voltage	37	–	–	0.4	V	I_{CSO} = 5 mA
V_{CSOH}	Control Switch Output High Voltage		4.0	–	–	V	$-I_{CSO}$ = 1.5 mA
V_{CSOHI}	Control Switch Output High Impedance Current		–10	–	+10	µA	V_O = 0 to +5 V
f_{CR}	Capture Range and Frequency Borders of the Horizontal PLL	–	15625 Hz ± 800 Hz			–	**DPU 2553** for PAL, SECAM and D2–MAC
			31250 Hz ± 1600 Hz			–	**DPU 2554** for PAL, SECAM and D2–MAC
			15734 Hz ± 750 Hz			–	**DPU 2553** for NTSC
			31 468 Hz ± 1500 Hz			–	**DPU 2554** for NTSC
			18746, 802 Hz ± 400 Hz			–	for Text Display Mode
$DR_{CL/HO}$	Divider Ratio between ΦM Clock Frequency and 1 Horizontal Output Frequency f_{HO}	2, 31	–	946	–	–	for Text Display Mode with $f_{ΦM}$ = 17.734475 MHz
			–	1296	–	–	for D2–MAC Mode with $f_{ΦM}$ = 20.25 MHz
			–	1135.0064	–	–	for PAL and SECAM with $f_{ΦM}$ = 17.734475 MHz
			–	910	–	–	for NTSC with $f_{ΦM}$ = 14. 31818 MHz

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
D_{SON}	Switch–On Delay for Horizontal Color–Locking	–	–	10	–	s	for PAL and SECAM
			–	8.5	–	s	for NTSC
D_{SOF}	Switch–Off Delay for Horizontal Color–Locking	–	–	80	–	ms	for PAL and SECAM
			–	66	–	ms	for NTSC
$D_{HO/FL}$	Admissible Delay between Hor. Output Pulse (Pin 31) and Hor. Flyback Pulse (Pin 23)	31, 23	0	–	15	µs	**DPU 2553**
			0	–	10	µs	**DPU 2554**
Phase Position Between Center of the Horizontal Sync Pulse in the Digital Video Signal at Pins 9 to 15 and the Leading Edge of the Horizontal Flyback Pulse at Pin 23 assuming that the Digital Composite Video Signal is delayed in the PVPU/CVPU,PSP and/or DTI for 65 Clock Periods of 17.7 or 14.3 MHz:							
t_{SZ}	Phase Position	9 to 15, 23	–	–0.22	–	µs	**DPU 2553** for PAL and SECAM, t_{HFL} = 12 µs
t_{SZ}	Phase Position		–	–0.22	–	µs	**DPU 2554** for PAL and SECAM, t_{HFL} = 6.2 µs
t_{SZ}	Phase Position		–	–0.98	–	µs	**DPU 2553** for NTSC, t_{HFL} = 11 µs
t_{SZ}	Phase Position		–	–0.54	–	µs	**DPU 2554** for NTSC, t_{HFL} = 5.75 µs
Δt_{SZ}	Phase Setting Range		–	±3.5	–	µs	**DPU 2553** for PAL and SECAM
Δt_{SZ}	Phase Setting Range		–	±1.75	–	µs	**DPU 2554** for PAL and SECAM
Δt_{SZ}	Phase Setting Range		–	±4.5	–	µs	**DPU 2553** for NTSC
Δt_{SZ}	Phase Setting Range		–	±2.25	–	µs	**DPU 2554** for NTSC
dt_{SZ}	Phase Setting Step Width	9 to 15, 23	–	0.225	–	µs	**DPU 2553** for PAL and SECAM
dt_{SZ}	Phase Setting Step Width		–	0.11	–	µs	**DPU 2554** for PAL and SECAM
dt_{SZ}	Phase Setting Step Width		–	0.28	–	µs	**DPU 2553** for NTSC
dt_{SZ}	Phase Setting Step Width		–	0.14	–	µs	**DPU 2554** for NTSC
V_{SKOL}	Skew Data Output Low Voltage	7	–	–	0.4	V	I_{SKO} = 12 mA
V_{SKOH}	Skew Data Output High Voltage		3.5	–	–	V	$-I_{SKO}$ = 0.1 mA

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
Vertical Synchronization							
R_{HSON}	HSP Status Output ON Resistance	20	–	–	10	kΩ	I_{HSO} = 0.1 mA
I_{HSOOF}	HSP Status Output OFF Resistance	20	–	–	10	µA	V_{HSO} = 5 V
R_{ON}	Output ON Resistance	26 to 28	–	100	–	Ω	$\pm I_O$ = 0.5 mA
V_{ICL}	Interlace Control Output Low Voltage	39	–	–	0.4	V	I_{IC} = 6 mA
I_{ICH}	Interlace Control Output High Current		–	–	10	µA	V_{IC} = 5 V
t_{dB}	Delay of the Vertical Blanking Pulse	22	–	35	–	µs	for PAL and SECAM, not locked
			–	4.5	–	µs	for PAL and SECAM, locked
			–	35	–	µs	for NTSC, not locked
			–	36.5	–	µs	for NTSC, locked
CRVS	Capture Range of the Vertical Synchronization Output	–	50 Hz ± 5 Hz			–	**DPU 2553** for PAL, SECAM and D2–MAC
			100 Hz ± 10 Hz			–	**DPU 2554** for PAL, SECAM and D2–MAC
			60 Hz ± 6 Hz			–	**DPU 2553** for NTSC
			120 Hz ± 12 Hz			–	**DPU 2554** for NTSC
$DR_{2H/V}$	Divider Ratio between Double the Horizontal Frequency and the Vertical Frequency in the Locked Operation Mode Switch–On–Delay for the Vertical Locking (adjustable)	–	–	625	–	–	for PAL and SECAM
			–	525	–	–	for NTSC
			–	624	–	–	for Text Display Mode (ZN = 0)
D_{SON}	Switch–On–Delay for the Vertical Locking (adjustable)	–	1.3	–	2.5	s	for PAL and SECAM
			1.7	–	3.3	s	for NTSC
D_{SOF}	Switch–Off–Delay for the Vertical Locking (adjustable)		80/160/240/320			ms	for PAL and SECAM
			67/134/200/270			ms	for NTSC

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
Key and Blanking Pulses							
V_{BOL}	1 V Vertical Blanking Output Low Voltage	3	–	–	0.4	V	I_{VBO} = 1.6 mA
V_{BOH}	1 V Vertical Blanking Output High Voltage		3.5	–	–	V	$-I_{VBO}$ = 0.1 mA
	1 V Vertical Blanking Output Timing		Same Timing as Pin 22 Vertical but Single–Scan Pulses only				
Undelayed Horizontal Blanking and Color Key Pulse Output		19					
I_{UHBOL}	Undelayed Horizontal Blanking Pulse Output Low Level (High Impedance)		–10	–	+10	µA	V_{UHBO} = 0 to +5 V
V_{UHBOH}	Undelayed Horizontal Blanking Pulse Output High Voltage		4.0	–	–	V	$-I_{UHBO}$ = 0.1 mA
t_{AZ1}	Undelayed Horizontal Blanking Pulse Phase Position		–	3.85	–	µs	
V_{CKOL}	Color Key Pulse Output Low Voltage		–	–	0.4	V	I_{CKO} = 6 mA
V_{CKOH}	Color Key Pulse Output High Voltage		4.0	–	–	V	$-I_{CKO}$ = 0.1 mA
t_{VB1}	Color Key Pulse Phase Position		–	2.82	–	µs	
Delayed Horizontal Blanking and Vertical Blanking Pulse Output		22					
I_{DHBOL}	Delayed Horizontal Blanking Pulse Output Low Level (High Impedance)		–10	–	+10	µA	V_{DHBO} = 0 to +5 V
V_{DHBOH}	Delayed Horizontal Blanking Pulse Output High Voltage		4.0	–	–	V	$-I_{DHBO}$ = 0.1 mA
t_{AZ2}	Delayed Horizontal Blanking Pulse Phase Position		–	–1.26	–	µs	with BP = 19
V_{VBOL}	Vertical Blanking Pulse Output Low Voltage		–	–	0.4	V	I_{VBO} = 6 mA
V_{VBOH}	Vertical Blanking Pulse Output High Voltage		4.0	–	–	V	$-I_{VBO}$ = 0.1 mA
	Vertical Blanking Pulse Phase Position	22	see t_{DB} at Vertical Synchronization				
t_{AB}	Vertical Blanking Pulse Duration		–	0.83	–	ms	for PAL and SECAM with VBL=4
			that is 18.5 lines				
			–	0.83	–	ms	for NTSC with VBL = 0
			that is 13 lines				
V_{UHBOL}	Undelayed Horizontal Blanking Pulse Output Low Voltage	24	–	–	0.4	V	I_{UHBO} = 1.6 mA
V_{UHBOH}	Undelayed Horizontal Blanking Pulse Output High Voltage		3..5	–	–	V	$-I_{HBO}$ = 0.1 mA
	Undel. Hor. Blank. Pulse Timing		Same Timing as Pin 19				

Table 2–1: Adjustment range and step width for the various adjustments for vertical single–scan mode

Adjustable Quantity	Step Width	Adjustment Range
Vertical Amplitude*)	1 %	±20 %
Vertical Linearity (S Curve)	0.1 %	0 to 20 %
Point of Inflection of the S curve**)	0.5 %	100 %
Vertical Position	0.1 %	±10 %
Horizontal Amplitude	0.4 %	±30 %
Cushion Correction	0.3 %	Curvature 10 to 90 %
Trapezoidal Correction	0.1 %	±10 %

*) 1 % = 2 mm with a 26–inch picture tube
**) at 10 % linearity correction

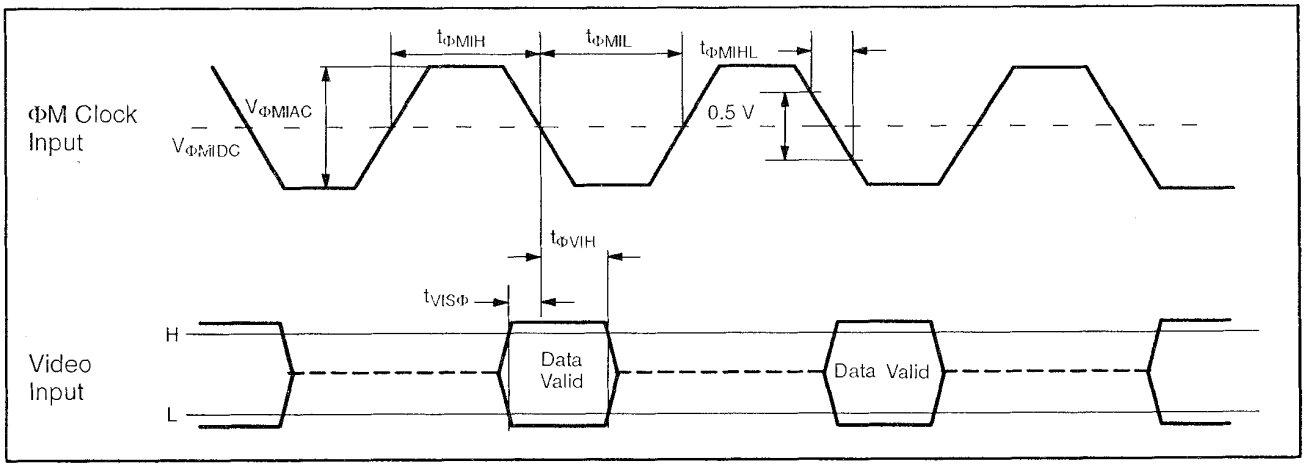

Fig. 2–15: Digital video input signals (pins 9 to 15)

3. Functional Description

3.1. Block Diagram

The DPU 2553 and DPU 2554 Deflection Processors perform all tasks associated with deflection in TV sets:

- sync separation
- generation and synchronization of the horizontal and the vertical deflection frequencies
- the various east–west corrections
- vertical sawtooth generation including S correction

as described hereafter. The DPU communicates, via the bidirectional serial IM bus, with the CCU 2050 or CCU 2070 Central Control Unit and, via this bus, is supplied with the picture–correction alignment information stored in the MDA 2062 EEPROM during set production, when the set is turned on. The DPU is normally clocked with a trapezoidal 17.734 MHz (PAL or SECAM), or 14.3 MHz (NTSC) or 20.25 MHz (D2–MAC) clock signal supplied by the MCU 2600 or MCU 2632 Clock Generator IC. The functional diagram of the DPU is shown in Fig. 3–1.

3.2. The Video Clamping Circuit and the Sync Pulse Separation Circuit

The digitized composite video signal delivered as a 7–bit parallel signal by the VCU 2133, VCU 2134 or VCU 2136 Video Codec is first noise–filtered by a 1 MHz digital low-pass filter and, to improve the noise immunity of the clamping circuit, is additionally filtered by a 0.2 MHz low-pass filter before being routed to the minimum and back porch level detectors (Fig. 3–3).

The DPU has two different clamping outputs, No. 1 and No. 2, one of which supplies the required clamping pulses to the video input of the VCU as shown in Fig. 3–1. The following values for the clamping circuit apply for Video Amp. I. since the gain of Video Amp. II is twice that of Video Amp I, all clamping and signal levels of Video Amp II are half those of Video Amp I referred to +5 V.

After the TV set is switched on, the video clamping circuit first of all ensures by means of horizontal–frequency current pulses from the clamping output of the DPU to the coupling capacitor of the analog composite video signal, that the video signal at the VCU's input is optimally biased for the operation range of the A/D converter of 5 to 7 V. For this, the sync top level is digitally measured and set to a constant level of 5.125 V by these current pulses. The horizontal and vertical sync pulses are now separated by a fixed separation level of 5.250 V so that the horizontal synchronization can lock to the correct phase (see section 3.3. and Figs. 3–2 and 3–3).

With the color key pulse which is now present in synchronism with the composite video signal, the video clamping circuit measures the DC voltage level of the porch and by means of the pulses from pin 21 (or pin4), sets the DC level of the porch at a constant 5.5 V (5.25 V for Video Amp II). This level is also the reference black

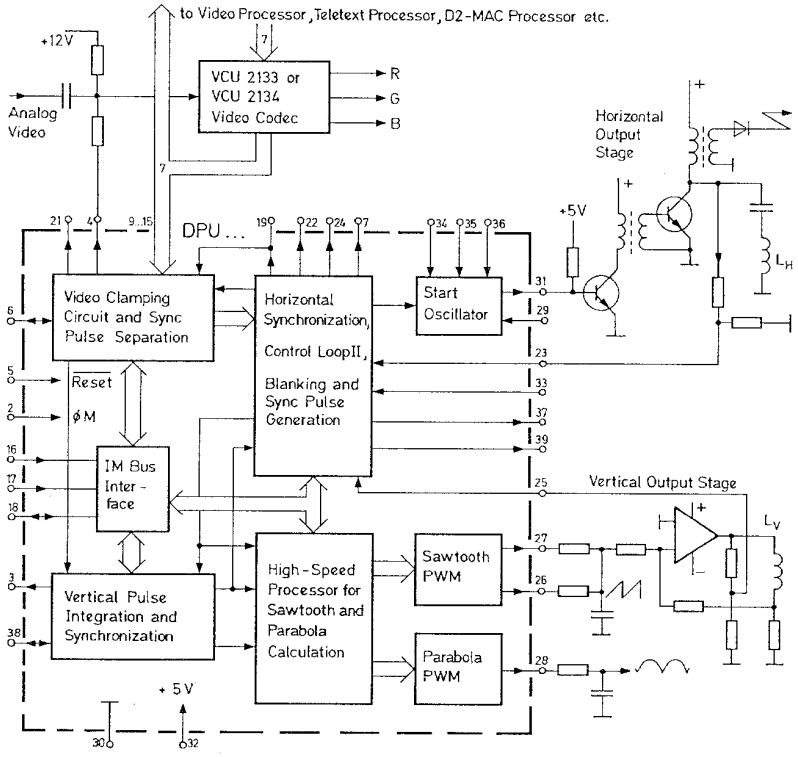

Fig. 3–1: Block diagram of the DPU 2553/54 Deflection Processors

level for the PVPU 2204 or CVPU 2270 Video Processors.

When horizontal synchronization is achieved, the slice level for the sync pulses is set to 50 % of the sync pulse amplitude by averaging sync top and black level. This ensures optimum pulse separation, even with small sync pulse amplitudes (see application notes, section 4.).

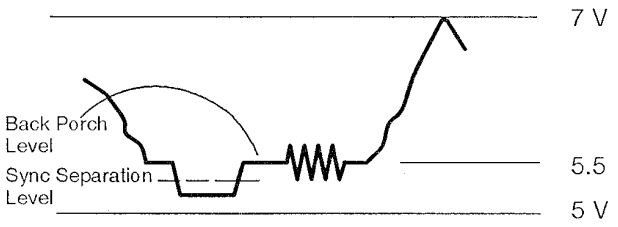

Fig. 3–2: Levels in the video clamping circuit

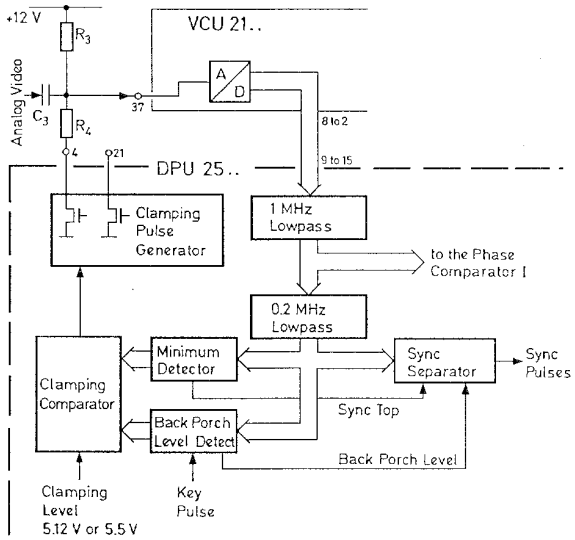

Fig. 3–3: Principle of video clamping and pulse separation

3.3. Horizontal Synchronization

Two operating modes are provided for in horizontal synchronization. The choice of mode depends on whether or not the TV station is transmitting a standard PAL or NTSC signal, in which there is a fixed ratio between color subcarrier frequency and horizontal frequency. In the first case we speak of "color–locked" operation and in the second case of "non–color–locked" operation (e.g. black–and–white programs). Switching between the two modes is performed automatically by the standard signal detector.

3.3.1. Non–Color–Locked Operation

In the non–locked mode, which is needed in the situation where there is no standard fixed ratio between the color subcarrier frequency and the horizontal frequency of the transmitter, the horizontal frequency is produced by subdividing the clock frequency (17.7 MHz for PAL and SECAM, 14.3 MHz for NTSC) in the programmable frequency divider (Fig. 3–4) until the correct horizontal frequency is obtained. The correct adjustment of frequency and phase is ensured by phase comparator I. This determines the frequency and phase deviation by means of a digital phase comparison between the separated horizontal sync pulses and the output signal of the programmable divider and corrects the divider accordingly. For optimum adjustment of phase jitter, capture behavior and transient response of the horizontal PLL circuit, the measured phase deviation is filtered in a digital lowpass filter (PLL phase filter). In the case of non–synchronized horizontal PLL, this filter is set to wideband PLL response with a pull–in range of ±800 Hz. If the PLL circuit is locked, the PLL filter is automatically switched to narrow–band response by an internal synchronism detector in order to limit the phase jitter to a minimum, even in the case of weak and noisy signals.

A calculator circuit in phase comparator I, which analyzes the edges of the horizontal sync pulses, increases the resolution of the phase measurement from 56 ns at 17.7 MHz clock frequency to approx. 6 ns, or from 70 ns at 14.3 MHz clock frequency to approx. 2.2 ns.

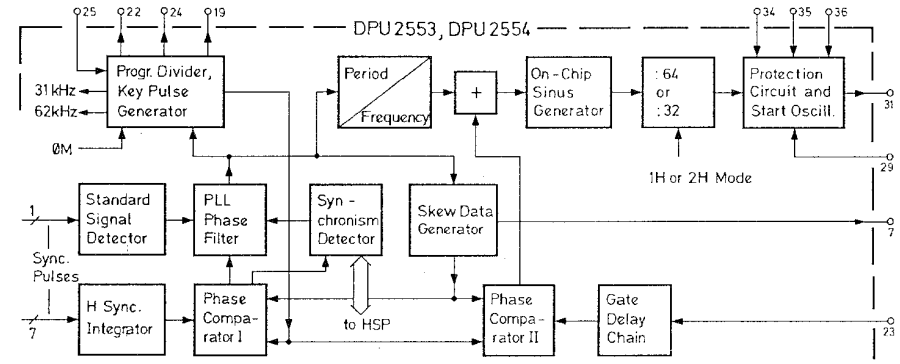

Fig. 3–4: Principle of the horizontal synchronization

The various key and gating pulses such as the color key pulse (t_{Key}), the normal–scan (1H) and double–scan (2H) horizontal blanking pulse (t_{AZV}) and the 1 H horizontal undelayed gating pulse (t_{AZ}) are derived from the output signals of the programmable divider and an additional counter for the 2H signals and the 1H and 2H skew data output. These pulses retain a fixed phase position with respect to the 1H input video signal and the double–scan output video signal from the CVPU 2270 Video Processor.

For the purpose of equalizing phase changes in the horizontal output stage due to switching response tolerances or video influence, a second phase control loop is used which generates the horizontal output pulse at pin 31 to drive the horizontal output stage. In phase comparator II (Fig. 3–4), the phase difference between the output signal of the programmable divider and the leading edge (or the center) of the horizontal flyback pulse (pin 23) is measured by means of a balanced gate delay line. The deviation from the desired phase difference is used as an input to an adder. In this, the information on the horizontal frequency derived from phase comparator I is added to the phase deviation originating form phase comparator II. The result of this addition controls a digital on–chip sinewave generator (about 1 MHz) which acts as a phase shifter with a phase resolution of 1/128 of one main clock period ΦM.

By means of control loop II the horizontal output pulse (pin 31) is shifted such that the horizontal flyback pulse (pin 23) acquires the desired phase position with respect to the output signal of the programmable divider which, in turn, due to phase comparator I, retains a fixed phase position with respect to the video signal. The horizontal output pulse itself is generated by dividing the frequency of the 1 MHz sinewave oscillator by a fixed ratio of 64 in the case of normal scan and of 32 in the case of double–scan operation.

3.3.2. Color–Locked Operation

When in the color–locked operating mode, after the phase position has been set in the non–color–locked mode, the programmable divider is set to the standard division ratio (1135:1 for PAL, 910:1 for NTSC) and phase comparator I is disconnected so that interfering pulses and noise cannot influence the horizontal deflection. Because phase comparator II is still connected, phase errors of the horizontal output stage are also corrected in the color–locked operating mode. The standard signal detector is so designed that it only switches to color–locked operation when the ratio between color subcarrier frequency and horizontal frequency deviates no more than 10^{-7} from the standard division ratio. To ascertain this requires about 8 s (NTSC). Switching off color–locked operation takes place automatically, in the case of a change of program for example, within approximately 67 ms (e.g. two NTSC fields, 60 Hz).

Table 3–1: Times relating to Fig. 3–5. The times are given in µs, the values in brackets represent the corresponding numbers of ΦM clock periods with SP = 16 and ZM = 1

Standard	PAL or SECAM with "BP" = 18		NTSC with "BP" = 19		Text mode with "BP"=18
	DPU 2554	DPU 2553	DPU 2554	DPU 2553	DPU 2553
One clock period =	56.38 ns	56.38 ns	69.84 ns	69.84 ns	56. 38 ns
t_{F1} t_{F2} t_{F3} t_{F4} t_{F5}	12.0 1.5 4.7 0.9 2.25	– – – – –	10.95 1.75 4.77 min. 0.38 min. 2.23	– – – – –	10.0 0.25 3.25 – –
t_{VB1} t_{19L} t_{VB2} t_{21}	2.82 (50) 3.67 (65) 6.49 (115) 0.86 (15)	– – – –	2.80 (40) 3.22 (46) 6.02 (86) 0.84 (12)	– – – –	2.26 (40) 2.59 (46) 7.85 (86) 0.86 (15)
t_{AZ1} t_{24}	3.85 (68) 10.4 (184)	– –	4.05 (58) 10.36 (148)	– –	3.27 (58) 8.34 (148)
t_{AZ2} t_{22H}	–0.22 (–4) 6.2 (110)	–0.22 (–4) 12.0 (213)	–1.26 (–18) 5.75 (82)	–1.26 (–18) 10.9 (156)	–1.02 (–18) 10.04 (178)
t_{SZ}	–0.22 (–4)	–0.22 (–4)	–1.54 (–22)	–0.98 (–14)	–0.79 (–14)
$t_{HO\ min}$ $t_{HO\ max}$	1 63	1 31	1 63	1 31	1 63
t_{AS1} and t_{AS2}	0.79	–	0.98	–	0.79 (14)

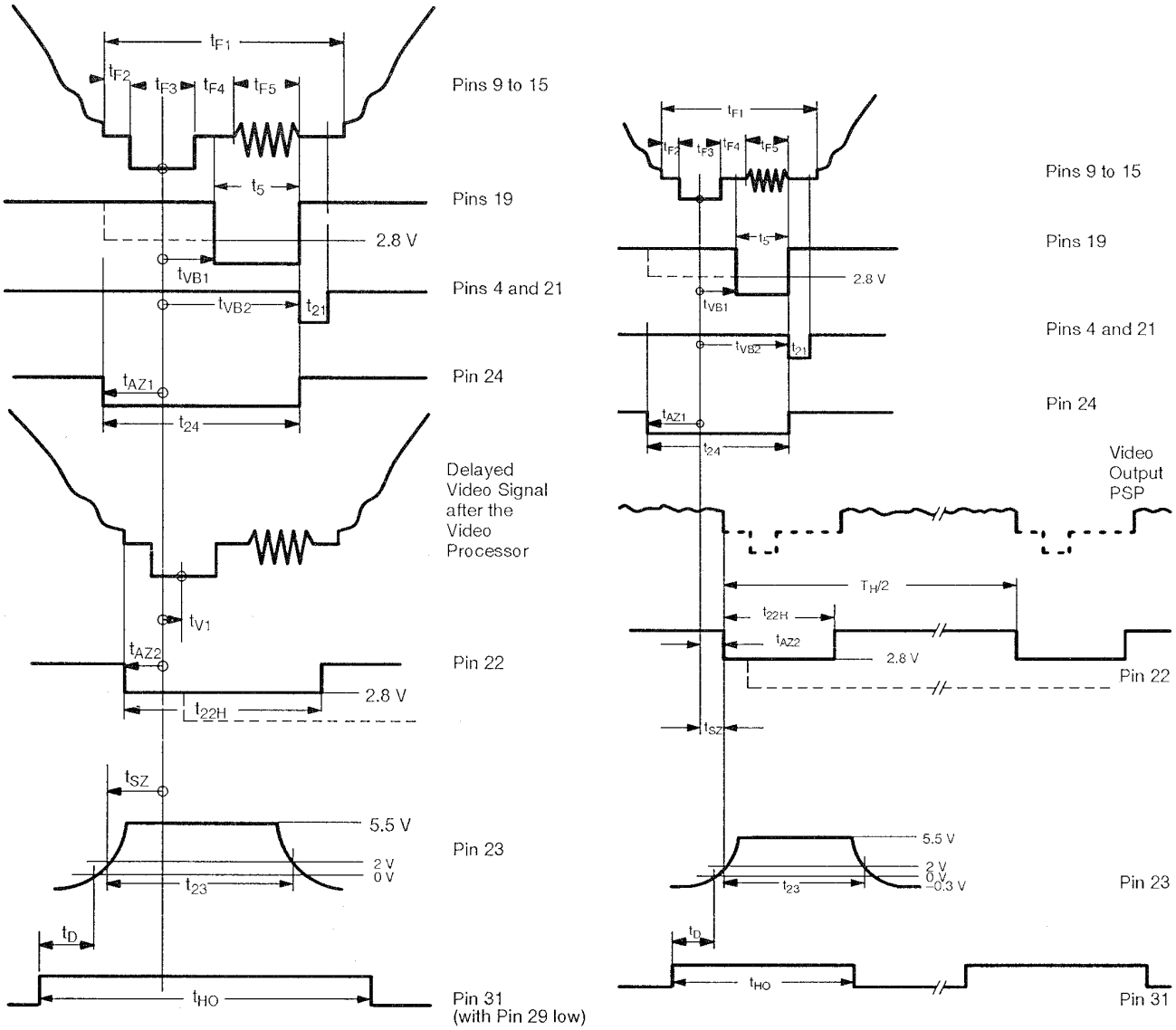

Fig. 3–5: Pulse diagram for the horizontal frequency
a) normal standard (**DPU 2553**)
b) double–scan mode (**DPU 2554**)

3.3.3. Skew Data Output and Field Number Information

With non–standard input signals, the TPU 2735 or TPU 2740 Teletext Processor produce a phase error with respect to the deflection phase.

The DPU generates a digital data stream (skew data, pin 7 of the DPU), which informs the PSP and TPU on the amount of phase delay (given in 2.2 ns increments) used in the DPU for the 1H and 2H output pulse compared with the FM main clock signal of 17.7 MHz (PAL or SECAM) or 14.3 MHz (NTSC), see also Figs. 3–6 to 3–8. The skew data is used by the PSP and by the TPU to adjust the double–scan video signal to the 1H and 2H phase of the horizontal deflection to correct these phase errors.

For the VMC processor the skew data contains three additional bits for information about frame number, 1 V sync and 2 V sync start.

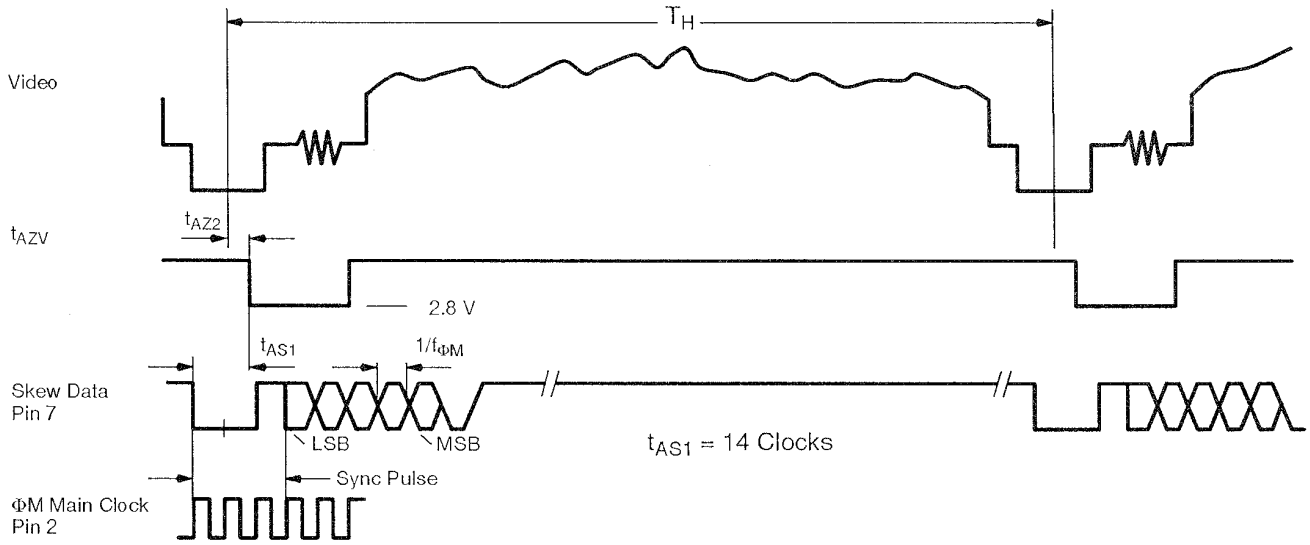

Fig. 3–6: Skew data timing at pin 7 of **DPU 2553** with ASK = 1

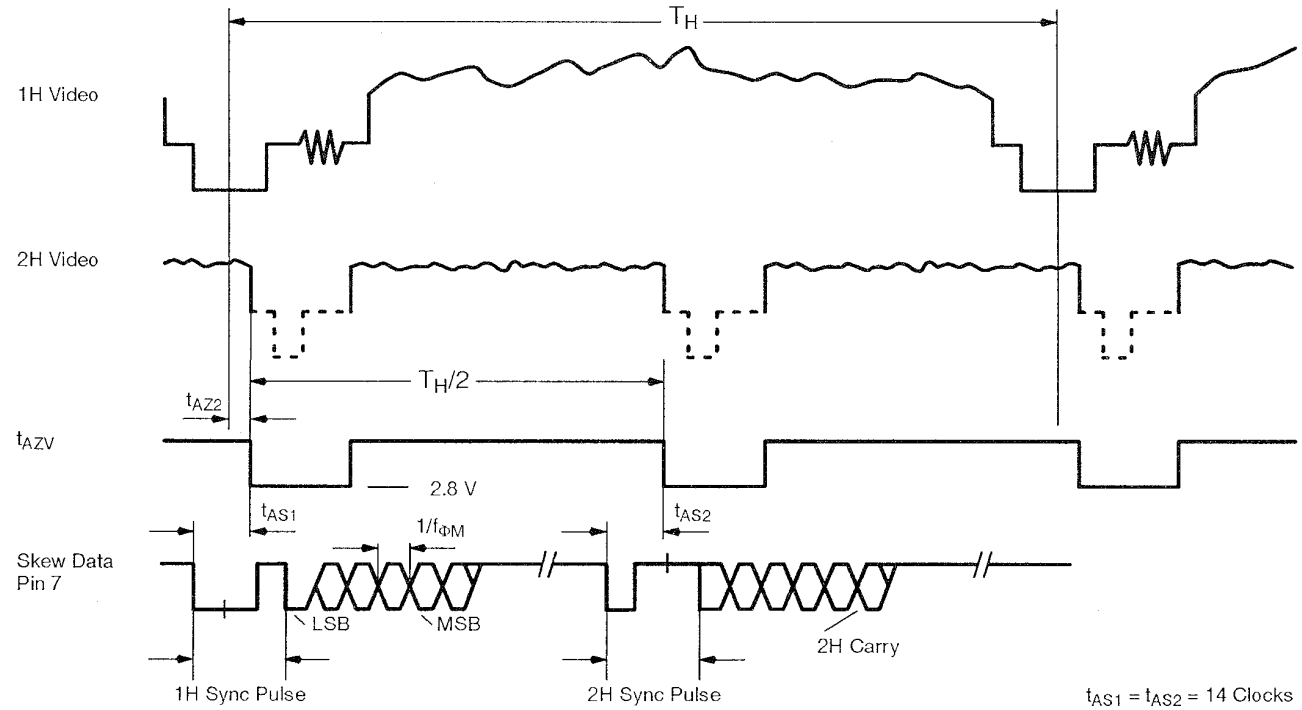

Fig. 3–7: Skew data timing at pin 7 of **DPU 2554** with ASK = 1

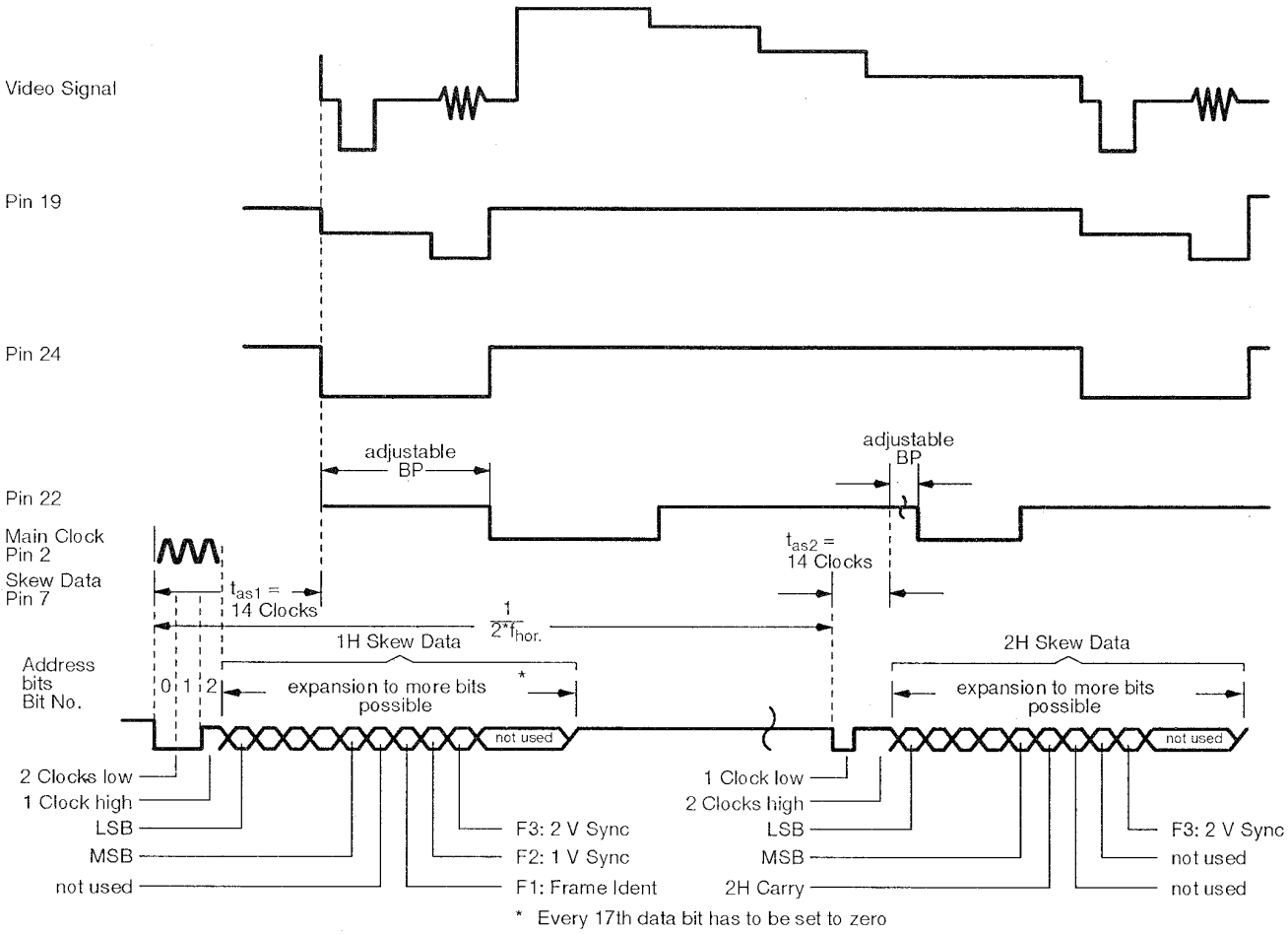

Fig. 3–8: Skew data timing for **DPU 2554** with ASK = 0

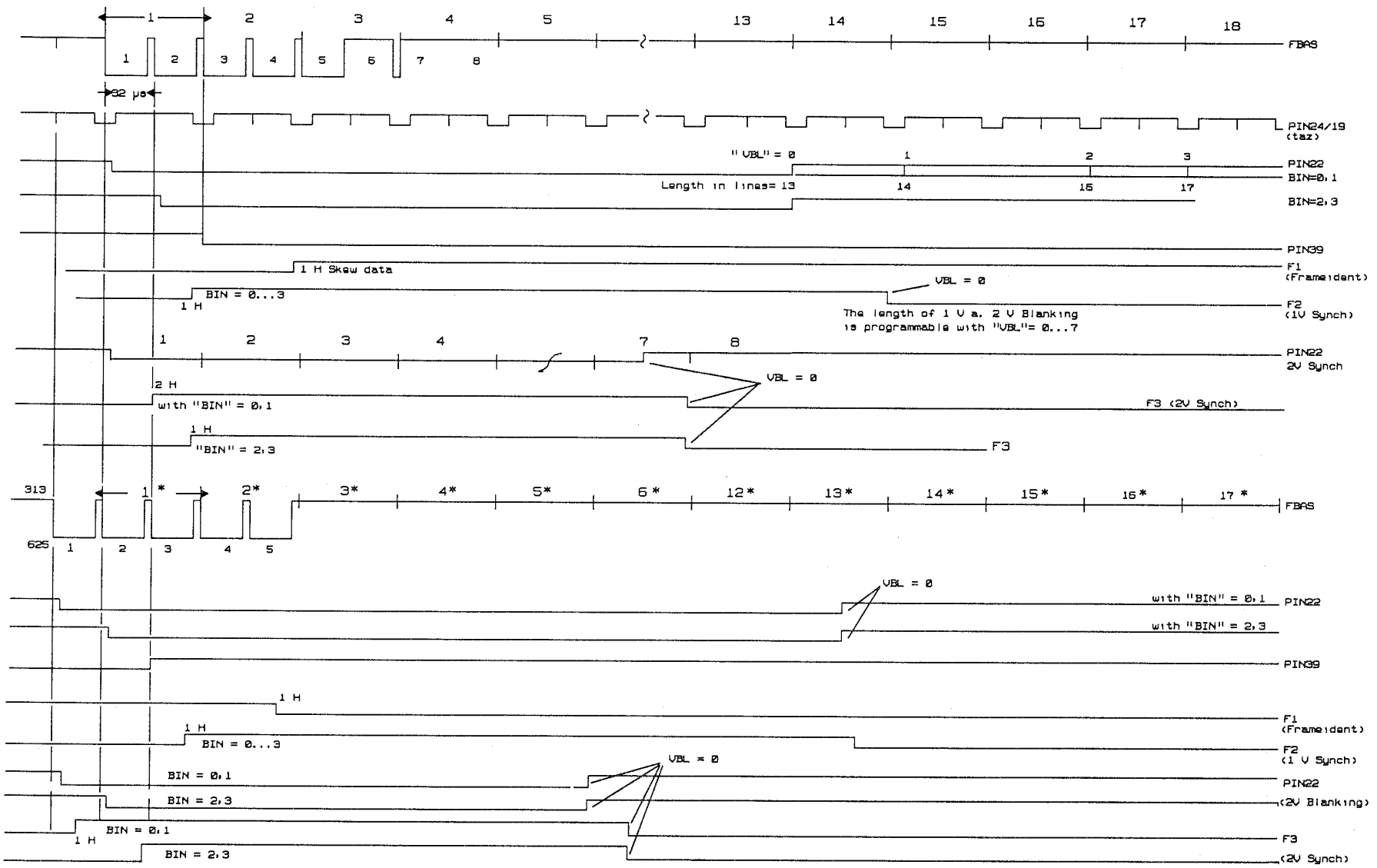

Fig. 3–9: Timing of pin 39 and of the frame–ident data bits

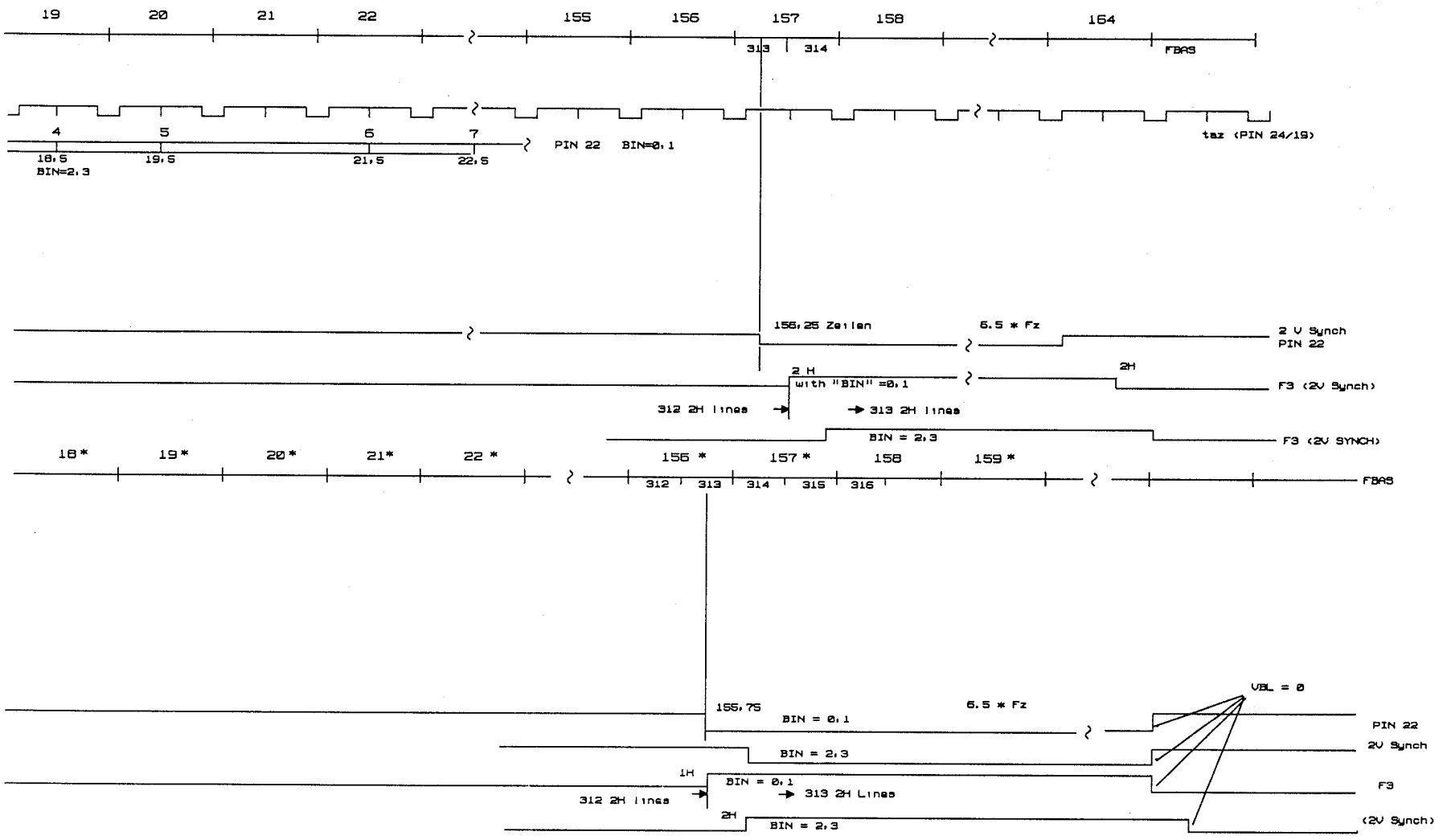

Fig. 3–10: Fig. 3–9 continued

3.3.4. Synchronism Detector for PLL and Muting Signal

To evaluate locking of the horizontal PLL and condition of the signal, the DPU's HSP high–speed processor (Fig. 3–1) receives two items of information from the horizontal PLL circuit (see Fig. 3–11).

a) the overall pulsewidth of the separated sync pulses during a 6.7 µs phase window centered to the horizontal sync pulse (value A in Fig. 3–11).

b) the overall pulsewidth of the separated sync pulse during one horizontal line but outside the phase window (value B in Fig. 3–11).

Based on a) and b) and using the selectable coefficients KS1 and KS2 and a digital lowpass filter, the HSP processor evaluates an 8–bit item of information "SD" (see Fig. 3–12). By means of a comparator and a selectable level SLP, the switching threshold for the PLL signal "UN" is generated. UN indicates whether the PLL is in the synchronous or in the asynchronous state.

To produce a muting signal in the CCU, the data SD can be read by the CCU. The range of SD extends from 0 (asynchronous) to +127 (synchronous). Typical values for the comparator levels and their hysteresis R1 = 30/20 and for muting 40/30 (see also HSP RAM address Table 5–6).

The corner frequency for the digital lowpass filter in Fig. 3–12 can be selected as shown in Table 3–2.

Table 3–2: Corner frequency of the digital lowpass filter

fk	Corner Frequency
0	20 Hz
1	10 Hz
2	5 Hz
3	2.5 Hz

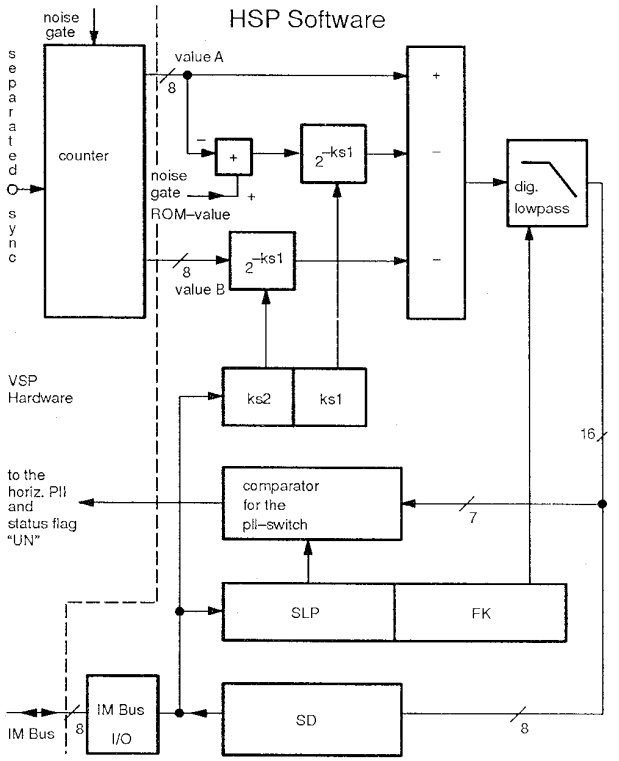

Fig. 3–12: Block diagram of the synchronism detector

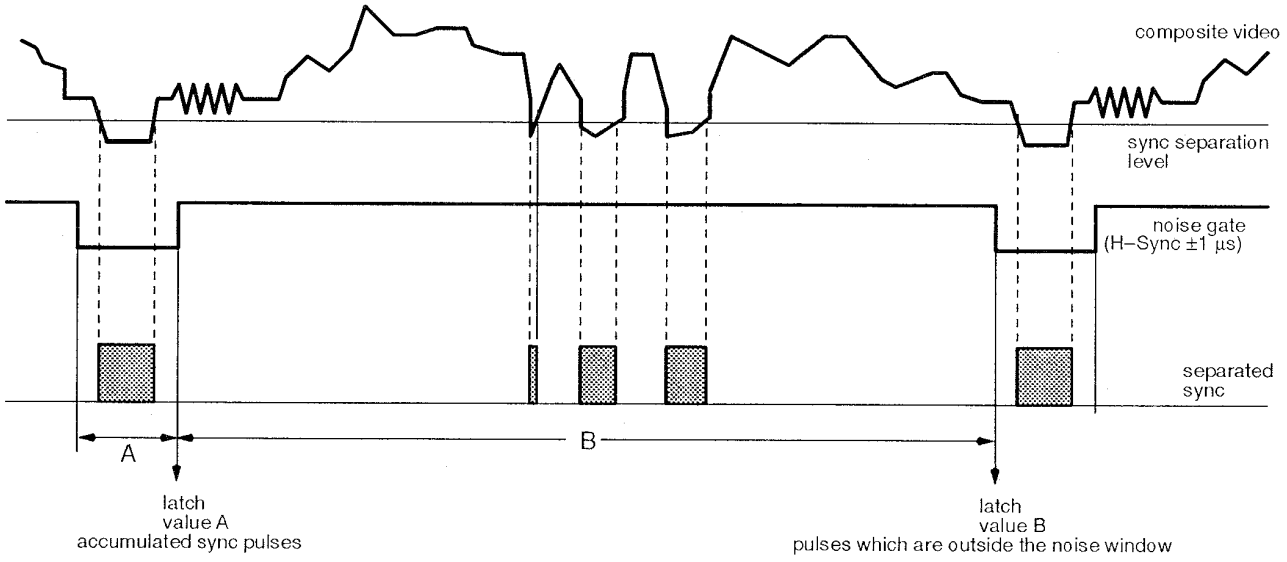

Fig. 3–11: Measurement of separated sync pulses for the synchronism detector

3.4. Start Oscillator and Protection Circuit

To protect the horizontal output stage of the TV set during changing the standard and for using the DPU as a low power start oscillator, an additional oscillator is provided on–chip (Fig. 3–4), with the output connected to pin 31. This oscillator is controlled by a 4 MHz signal independent from the FM main clock produced by the MCU 2600 or MCU 2632 Clock Generator IC and is powered by a separate supply connected to pin 35. The function of this circuitry depends on the external standard selection input pin 33 and on the start oscillator select input pin 36, as described in Table 3–3. Using the protection circuit as a start oscillator, the following operation modes are available (see Table 3–3).

With pin 33 open–circuit, pin 36 at high potential (connected to pin 35) and a 4 MHz clock applied to pin 34, the protection circuit acts as a start oscillator. This produces a constant–frequency horizontal output pulse of 15.5 kHz in the case of DPU 2553, and of 31 kHz in the case of DPU 2554 while the Reset input pin 5 is at low potential. The pulsewidth is 30 µs with DPU 2553, and 16 µs with DPU 2554. Main clock at pin 2 or main power supplies at pins 8, 32 and 40 are not required for this start oscillator After the main power supply is stabilized and the main clock generator has started, the Reset input pin 5 most be switched to the high state. As long as the start values from the CCU are invalid, the start oscillator will continuously supply the output pulses of constant frequency to pin 31. By means of the start values given by the CCU via the IM bus, the register FL must be set to zero to enable the start oscillator to be triggered by the horizontal PLL circuit. After that, the output frequency and phase are controlled by the horizontal PLL only.

If the external standard selection input pin 33 is connected to ground or to +5 V, the start oscillator is switched off as soon as it is in phase with PLL circuit. Pin 33 to ground selects PAL or SECAM standard (17.7 MHz main clock), and pin 33 to +5 V selects NTSC standard (14.3 MHz main clock). After the main power supplies to pins 8, 32 and 40 are stabilized, the start oscillator can be used as a separate horizontal oscillator with a constant frequency of 15.525 kHz. For this option, pin 33 must be unconnected. By means of the IM bus register SC the start oscillator can be switched on (SC = 0) or off (SC = 1). Setting SC = 1 is recommended.

By means of pin 29 (horizontal output polarity select input and start oscillator pulsewidth select input), the output pulsewidth and polarity of the start oscillator and protection circuit can be hardware–selected. Pin 29 at low potential gives 30 µs for DPU 2553 and 16 µs for DPU 2554, with positive output pulses. Pin 29 at high potential gives 36 µs for DPU 2553 and 18 µs for DPU 2554, with negative output pulses. Both apply for the time period in which no start values are valid from the CCU. If pin 29 is intended to be in the high state, it must be connected to pin 35 (standby power). Pin 29 must be connected to ground or to +5 V in both cases.

Table 3–3: Operation modes of the start oscillator and protection circuit

Operation Mode		Pins			
		33	34	35	36
Horizontal output stage protected during main clock frequency changing (for PAL and NTSC)		not connected	4 MHz Clock	at +5 V	at ground
Horizontal output stage protected and start oscillator function (for PAL and NTSC)		not connected	4 MHz Clock	+5 V with start oscillator supply	connected to pin 35
Only start oscillator function with NTSC standard after Reset		at +5 V	4 MHz Clock	+5 V with start oscillator supply	connected to pin 35
Only start oscillator function with PAL or SECAM standard after Reset		at ground	4 MHz Clock	+5 V with start oscillator supply	connected to pin 35
without protection and start oscillator function	with 17.7 MHz clock frequency only (PAL or SECAM)	at ground	at ground	at +5 V	at ground
	with 14.3 MHz clock frequency only (NTSC)	at +5 V	at ground	at +5 V	at ground

3.5. Blanking and Color Key Pulses

Pin 19 supplies a combination of the color key pulse and the undelayed horizontal blanking pulse in the form of a three–level pulse as shown in Fig. 3–13. The high level (4 V min.) and the low level (0.4 V max.) are controlled by the DPU. During the low time of the undelayed horizontal blanking pulse, pin 19 of the DPU i sin the high–impedance mode and the output level at pin 19 is set to 2.8 V by the VCU.

At pin 22, the delayed horizontal blanking pulse in combination with the vertical blanking pulse is available as a three–level pulse as shown in Fig. 3–13. Output pin 22 is in high–impedance mode during the delayed horizontal blanking pulse.

In double–scan operation mode (DPU 2554), pin 22 supplies the double–scan (2H) horizontal blanking pulse instead of the 1H blanking pulse (DPU 2553). In text display mode with increased deflection frequencies (see section 1.), pin 22 of the respective DPU (DPU 2553, as defined by register ZN) delivers the horizontal blanking pulse with 18.7 kHz and the vertical blanking pulse with 60 Hz according to the display. At pin 24 the undelayed horizontal blanking pulse is output.

Normally, pin 3 supplies the same vertical blanking pulse as pin 22. However, with "DVS" = 1, pin 3 will be in the single–scan mode also with double–scan operation of the system. The pulsewidth of the single–scan vertical blanking pulse at pin 3 will be the same as that of the double–scan vertical blanking pulse at pin 22. The output pulse of pin 3 is only valid if the CCU register "VBE" is set to 1. The default value is set to 0 (high–impedance state of pin 3).

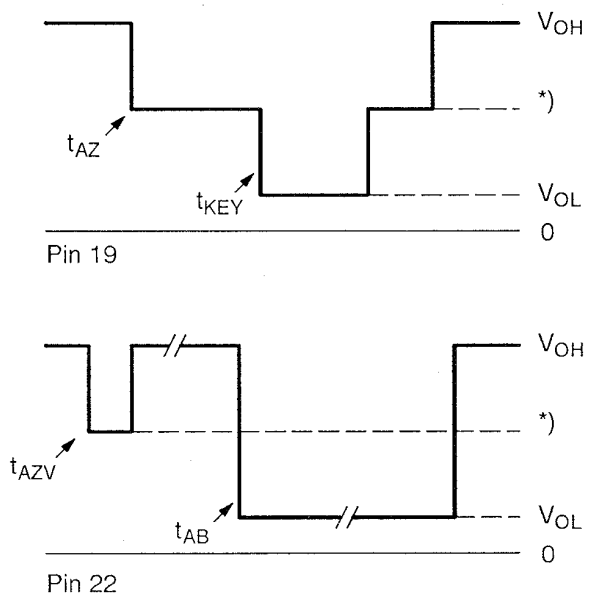

Fig. 3–13: Shape of the output pulses at pins 19 and 22
*) The output level is externally defined

3.6. Output for Switching the Horizontal Power Stage Between 15.6 kHz (PAL/NTSC) and 18 kHz (Text Display)

This output (pin 37) is designed as a tristate output. High levels (4 V min.) and low levels (0.4 V max.) are controlled by the DPU. During high–impedance state an external resistor network defines the output level.

For changing the horizontal frequency from 15 kHz to 18 kHz, the following sequence of output levels is derived at pin 37 (see Fig. 3–14).

After register ZN is set from ZN = 2 (15 kHz) to ZN = 0 (18 kHz) by the CCU, pin 37 is switched from High level to high–impedance state synchronously with the frequency change at pin 31. Following a delay of 20ms, pin 37 is set to Low level and remains in this state for the time the horizontal frequency remains 18 kHz (with ZN = 0). This 20 ms delay is required for switching–over the horizontal power stage.

To change the horizontal frequency in the opposite direction, from 18 kHz to 15.6 kHz, the sequence described is reversed.

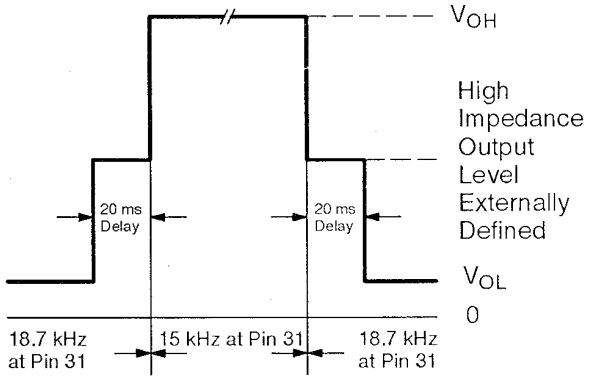

Fig. 3–14: Timing of the output signal at pin 37

3.7. Text Display Mode with Increased Deflection Frequencies

As already mentioned, the DPU 2553 provides the feature of increased deflection frequencies for text display for improved picture quality in this mode of operation. To achieve this, the processor acting as deflection processor has its register ZN set to 0. The horizontal output frequency at pin 31 is then switched to a frequency of 18746.802 Hz which is generated by dividing the FM main clock frequency by 946 ± 46. The horizontal PLL is then able to synchronize to an external composite sync signal of f_H = 18.746 kHz ± 46. The horizontal PLL is then able to synchronize to an external composite sync signal of f_H = 18.746 kHz ± 5 % and f_V = 60 Hz ± 10 % and can be set to an independent horizontal and vertical sync generator by setting register VE = 1 and register VB = 0. That means a constant divider of 946 for horizontal frequency and constant 312 lines per frame.

The DPU working in this mode supplies the TPU 2740 Teletext Processor or the respective Viewdata Processor with the 18.7 kHz horizontal blanking pulses form pin 24 and the 60 Hz vertical blanking pulses form pin 22 (see Fig. 3–8).

To be able to receive and store data from an IF video signal at the same time, the Teletext or Viewdata Processor requires horizontal and vertical sync pulses from this IF signal. Therefore, the second DPU provides video clamping and sync separation for the external signal and supplies the horizontal sync pulses (pin 24) and the vertical sync pulses (pin 22) to the Teletext or Viewdata Processor. For this, the second DPU is set to the PAL standard by register ZN = 2, and the clamping pulses of the other DPU are disabled by CLD = 1.

To change the output frequency of the DPU acting as deflection processor from 18.7 kHz to 15.6 kHz, the control switch output pin 37 prepares the horizontal output stage for 15.6 kHz operation (pin 37 is in the high–impedance state) before the DPU changes the horizontal output frequency to 15.6 kHz, after a minimum delay of one vertical period. Switching the horizontal deflection frequency from 15.6 kHz to 18.7 kHz is done in the reverse sequence. Firstly, the horizontal output frequency of pin 31 is switched to 18.7 kHz, and after a delay of one vertical period, pin 37 is set low.

3.8. D2–MAC Operation Mode

When receiving TV signals having the D2–MAC standard (direct satellite reception), register ZN is set to 3. The programmable divider is set to a division ratio of 1296 ±48 to generate a horizontal frequency of 15.625 kHz with the clock rate of 20.25 MHz used in the D2–MAC standard. In this operation mode, pin 6 acts as input for the composite sync signal supplied by the DMA 2271 D2–MAC Decoder. The DPU is synchronized to this sync signal, and after locking–in (status register UN = 0), the CCU switches the DPU to a clock–locked mode between clock signal and horizontal frequency ($f_{\Phi M}/f_H = 1296$).

In D2–MAC operation mode (ZN = 3), the clamping pulse outputs (pins 4 and 21) are set to the high–impedance state by the CCU (with CLD = 1) to enable the video clamping function of the DMA 2270 at the same pin of the VCU. Further, pin 24 must be set to the high–impedance state by means of register "UHD", because the DMA 2271 uses this pin.

3.8.1. Vertical Synchronization

The vertical sync pulse is derived by means of digital integration from the separated composite sync signal (Fig. 3–15). Then, the trigger pulse for the high–speed processor and the vertical deflection is produced in the working counter which divides the double horizontal frequency (31 kHz) by (625 ±64) for PAL and SECAM, and by (525 ±64) for NTSC.

The working counter can be set to three different operating modes (see Fig. 3–16):

1. Non–locked operation using a wide trigger window.
The working counter can be reset by the vertical sync pulse at a counter position of 561 to 689 (for PAL and SECAM) or of 461 to 589 (for NTSC), which means that it can be synchronized by vertical frequencies in the range from 45 to 55 Hz for PAL and SECAM or 54 to 66 Hz for NTSC.

2. Non–locked operation using a narrow trigger window
In this mode, the working counter reset range is restricted to between 618 to 632 for PAL and SECAM or 518 to 532 for NTSC. This ensures that improved noise immunity is also obtained with non–standard signals or in the case of video recorder operation.

3. Locked operation.
In this mode, the standard division ratio, e.g. 625 : 1 for PAL and SECAM or 525 : 1 for NTSC, is fixed. This ensures optimum noise immunity for all standard signals.

The three operating modes described are defined by the following test circuitry. A standard signal detector, comprising measuring counter, measuring window, coincidence detector and frequency detector, checks whether the ratio of the vertical frequency received to double the horizontal frequency is in accordance with the specified standard. For this purpose, the measuring counter which can be triggered first of all by the vertical sync pulses supplied by the transmitter in the counter range of 625 ±64 for NTSC, is used to produce a constant measuring window representing the counts 620 to 630 (PAL and SECAM) or 520 to 530 (NTSC). A subsequent up/down counter establishes whether five consecutive sync pulses appear in the measuring window. If this rough coincidence test has a positive result, the measuring counter is set to the standard divider ratio, and the frequency detector starts to count the vertical sync pulses lying inside the measuring window. When the count reaches 64 (in about 1.3 s for PAL and SECAM or about 1.7 s for NTSC), the frequency detector signals that locking is present between horizontal frequency and vertical frequency. Following this, the working counter is then also set to the standard division ratio.

The switch–on delay for the locked operation can be extended to 128 (corresponding to about 2.5 s for PAL and SECAM or 3.3 s for NTSC) by means of the CCU register "FF". The time needed for canceling the locked mode, in the case of a program change for example, is defined by the maximum counter reading of the up/down counter which can be selected. This counter counts down the sync pulses which do not appear in the measuring window. In the case of a reading of less than 2, the measuring counter is switched back to window operation and the frequency detector is reset to "0". The switch–off delay can be selected in four steps (from 80 to 320 ms for

PAL and SECAM or from 67 to 270 ms for NTSC) by means of the CCU register "GH".

With the aid of a further measuring window of 625 ±5 for PAL and SECAM or 525 ±5 for NTSC, which is derived from the working counter, a phase test circuit is used, synchronously with the frequency detector, to ascertain whether more than 128 consecutive sync pulses are found within the phase window of the synchronized working counter. If there have been, and the standard test has not yet resulted in locking of the vertical synchronization, the working counter is switched to the narrow window.

If the phase positions of the measuring counter and the working counter do not coincide, then the working counter is set to the phase position of the measuring counter if the sync pulse does not appear more than four times in succession in the measuring window of the working counter. This is done without directly influencing the other test circuitry.

To achieve additional noise suppression, the vertical sync pulse passes through a gating circuit derived from the measuring counter which corresponds to a count of 561 to 689 for PAL and SECAM or 461 to 589 for NTSC. In order to ensure vertical synchronization even when the vertical sync pulses in the composite sync signal are suppressed (in the case of reflections for example), all the test results remain unchanged if no vertical sync pulse from the transmitter is received during the entire vertical cycle, i.e. a locked operating mode, once switched on, is retained.

The vertical frequency fv is evaluated in the HSP high–speed processor by counting the cycles of the HSP calculation clock, which is derived by dividing the ΦM main clock by 1024, during the vertical sync signal separated from the received video signal. To use an 8–bit register, the result of the count is divided by 2 and given to the DPU status register. In the CCU, the vertical frequency can be evaluated using the following equation:

$$f_V = \frac{f_{\Phi M}}{1024 \cdot VP \cdot 2}$$

with

$f_{\Phi M}$ = 17.734475 MHz with PAL and SECAM

$f_{\Phi M}$ = 14.31818 MHz with NTSC

$f_{\Phi M}$ = 20.25 MHz with D2–MAC

VP = status value, read from DPU.

The interlace control output pin 39 supplies a 25 Hz (for PAL and SECAM) or 30 Hz (for NTSC) signal for controlling an external interlace–off switch, which is required with A.C.–coupled vertical output stages, because these are not able to handle the internal interlace–off procedure using register "ZS".

For operation with the VMC Processor the DPU 2554 has three interlace control modes in double vertical scan mode (DVS = 1). These options can be selected with the register "IOP" and can be used together with the control output pin 39 only. This output has to be connected to the vertical output stage, so that the vertical phase can be shifted by 16 µs (or 32 µs with DPU 2553).

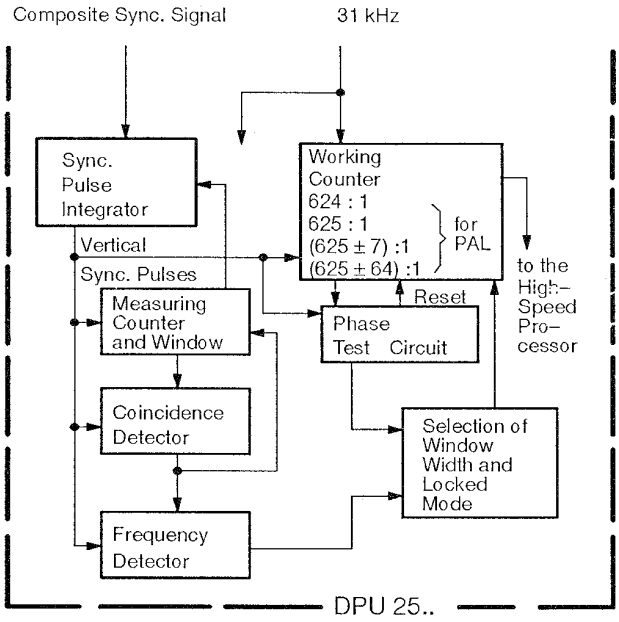

Fig. 3–15: Principle of the vertical synchronization

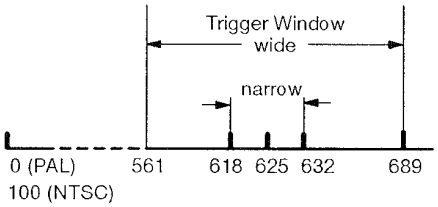

Fig. 3–16: Trigger window of the vertical synchroniza tion

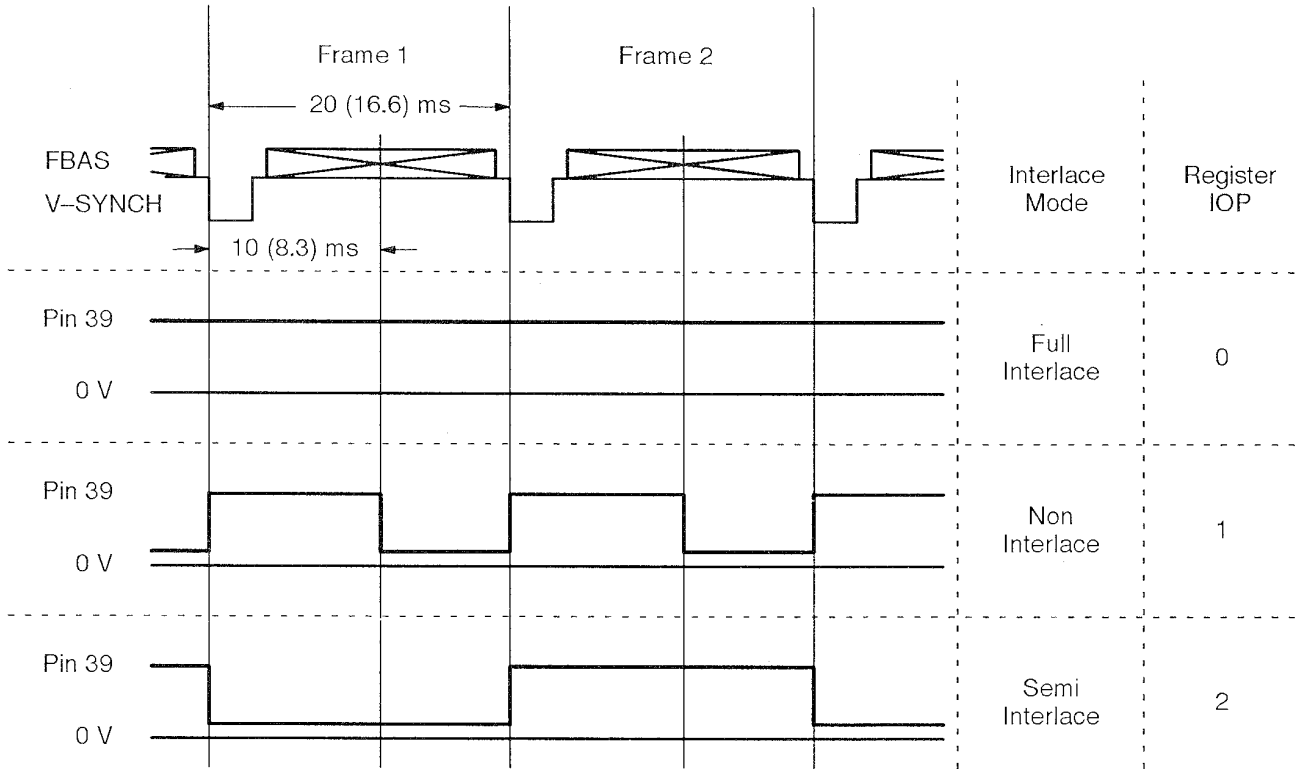

Fig. 3–17: Interlace options with register "IOP" in double vertical scan mode

Besides the skew data, pin 7 supplies three data bits which give the following vertical information:

F1 = field–ident data bit, which serves to identify the first and the second frame

F2 = single–scan vertical blanking (1 V sync)

F3 = double–scan vertical blanking (2 V sync)

The timing of the output signal of pin 39 can be seen in Figs. 3–9 and 3–10.

The type **DPU 2554** has the double–scan vertical mode, which is set by register "DVS" = 1. With this, the vertical deflection frequency is doubled, and the pulsewidth of the vertical blanking pulses at pins 3 and 22 is divided by two. To achieve the correct shape of the vertical sawtooth and parabola, the following geometry parameters must be doubled:

H_0, S_0, S_1, P_0, P_1, Z_0, Z_1

The values for k_1 and k_2 must be divided by two.

3.8.2. Calculation of S Correction and East–West Parabola and Pulsewidth Modulators

At pins 11 and 12 the DPU has two pulsewidth–modulated signals available for control of the vertical output stage and the east–west modulator circuit. After being smoothed by RC elements (Fig. 3–19) these signals serve as the voltage reference for the vertical deflection current and the east–west correction current. The DPU receives all adjustment values via the IM bus interface from the MDA 2062 EEPROM where they were stored when the TV set was manufactured. In the HSP high–speed processor and subsequently connected pulsewidth modulators, the adjustment values are converted into pulsewidth–modulated signals (Fig. 3–18).

To have more flexibility in calculation the east–west correction for different picture tubes (e.g. Trinitron tubes or flat–screen picture tubes), a newly–designed high–speed processor HSP is used (see Figs. 3–1 and 3–19 section 3.8.1.).

Using the vertical trigger pulse as a starting pulse, the HSP calculates a 12–bit value for the vertical sawtooth and the east–west parabola at a clock pulse rate of fΦM/1024 = 17.3 kHz for PAL and using the summation formulae given below. These values are quantized to 4–bit values and given to a pulsewidth modulator (Fig. 3–18) which, together with an external lowpass filter, acts as a 4–bit D/A converter with a conversion time of 16/fΦM. The quantizer's error is accumulated and fed back to the quantizer. In this way, the D.C. level of the externally–filtered output signal is controlled with a resolution of 5 V/1024. To generate the voltage step in the sawtooth during the vertical flyback, the same PSM signal as at pin 11 is output at pin 10 for five calculation periods,

in order to discharge the external filter capacitor to the start value of the sawtooth.

Fig. 3–19 shows the adjustment parameters, and Fig. 3–23 depicts their influence on the curve shapes of sawtooth and east–west parabola. The following equations describe the effect of the adjustment parameters on the summation formulae where Z is the number of 17 kHz computing–clock pulses. For the vertical sawtooth

$$Y_S = A_0 + \sum_{Z=1}^{Z=N} \left(\frac{H_0}{2^{10}} - \left| \frac{S_1}{2^8} - \frac{S_0}{2^{18}} \cdot \text{integer} \left[\frac{Z}{2} \right] \right| \right)$$

For a symmetrical curve, the values for S_0 and S_1 must be given in a certain ratio to one another:

$$S_1 = \frac{S_0}{2048} \cdot m$$

where:

$S_0 = 256 \cdot S_{0H} + S_{0L}$

$S_1 = 256 \cdot S_{1H} + S_{1L}$

The values of "m" are:

m = 144 for NTSC with 17.7 MHz
m = 173 for PAL, SECAM with 17.7 MHz
m = 116 for NTSC with 14.3 MHz

For the east–west parabola, two different parabolas are added to generate a combined parabola for Trinitron or flat–screen picture tubes (see Fig. 3–24).

$$Y_{P1} = 4 \cdot Y_0 + \sum_{Z=1}^{Z=N} \left(\frac{Z_0}{2^8} - \frac{P_0}{2^{18}} \cdot \text{integer} \left(\frac{Z+1}{2} \right) \right)$$

$$+ \sum_{Z=2k_1}^{Z=2k_2} \left(\frac{Z_1}{2^8} - \frac{P_1}{2^{18}} \cdot \left[\text{integer} \left(\frac{Z+1}{2} \right) - k_1 \right] \right)$$

For symmetrical curve, the values for P_0, P_1, Z_0 and Z_1 must be:

$$Z_0 = \frac{P_0 \cdot m}{2048}$$

$$Z_1 = \frac{P_1 \cdot (m - 2k_1)}{2048}$$

where:

$$P_0(Z_0, P_1, Z_1) = 256 \cdot P_{0H}(Z_{0H}, P_{1H}, Z_{1H}) + P_{0L}(Z_{0L}, P_{1L}, Z_{1L})$$

For adjusting the sawtooth and parabola parameter at the screen, it is recommended to increment the HSP RAM values in steps of:

H_0 : 16

S_0 : 8

S_1 : 4

P_0, P_1 : 64

Z_0, Z_1 : 16

For vertical double–scan, the steps must be divided by two.

For the parameters S_1, Z_0, Z_1 the HSP uses only 14 bits (LSB) of the RAM space of 16 bits.

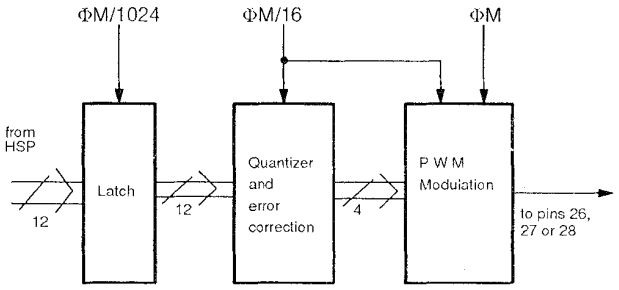

Fig. 3–18: Pulsewidth modulators for sawtooth and parabola

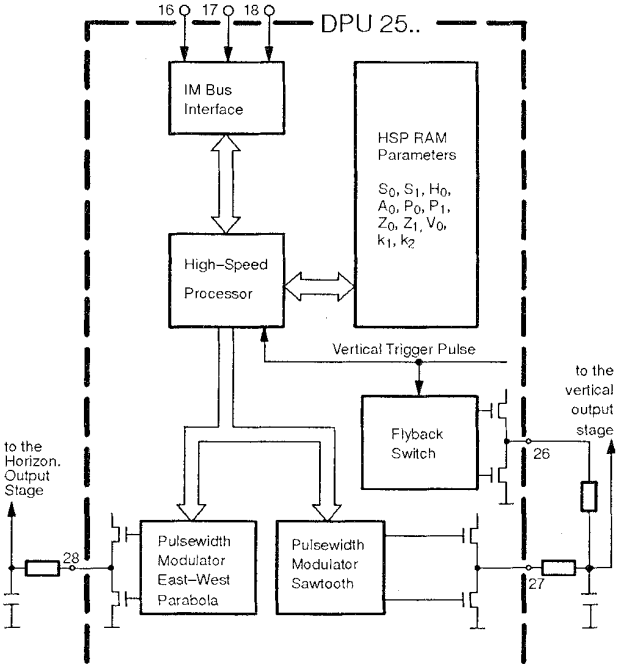

Fig. 3–19: Principle of the vertical PWM generation

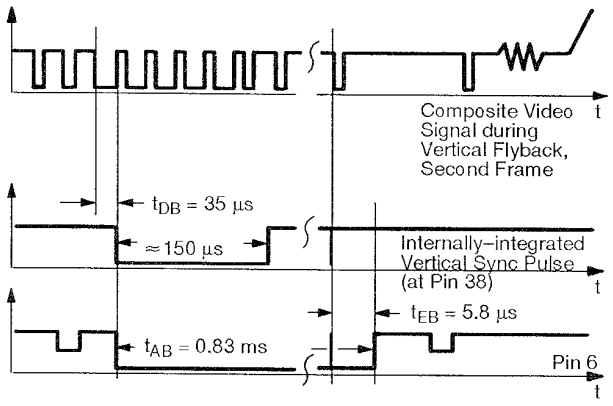

Fig. 3–20: Pulse diagram for the vertical frequency (for NTSC)

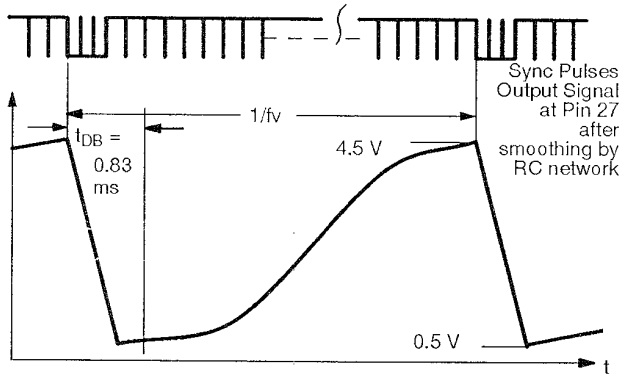

Fig. 3–21: Signals at the vertical sawtooth output pin 27 and at the vertical flyback output pin 26 (for PAL)

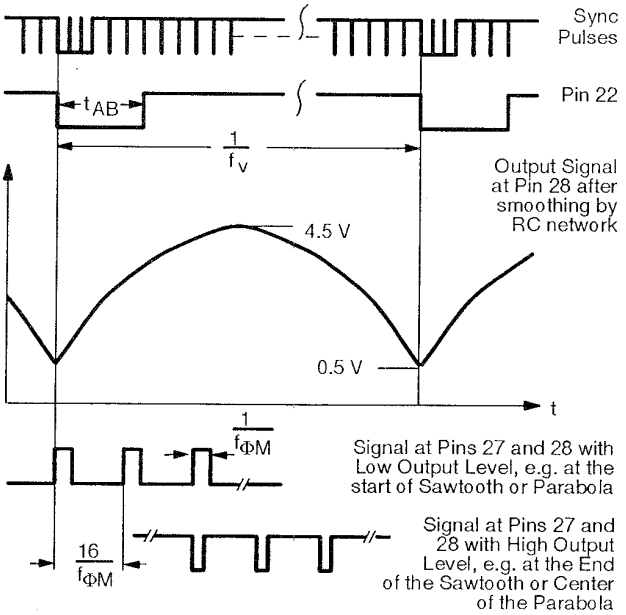

Fig. 3–22: Signals at the east–west parabola output pin 28

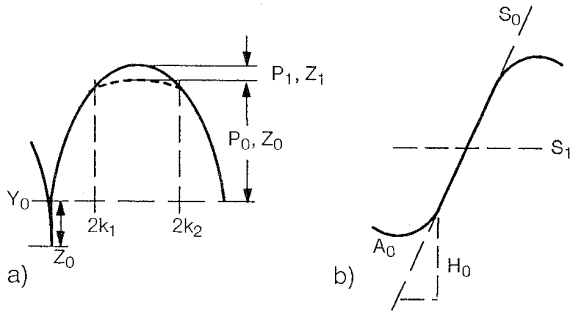

Fig. 3–23: Influence of the adjustment parameters on the curves
a) east–west parabola b) vertical sawtooth

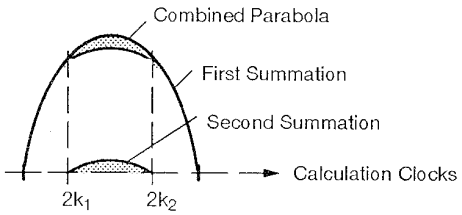

Fig. 3–24: Combined east–west parabola for Trinitron or flat–screen picture tubes

3.9. Subaddressing of the HSP Processor

The hardware of the high–speed processor is shown in Fig. 3–27 with respect to the input/output functions of the HSP. For communicating via the IM bus, the HSP has four IM bus addresses:

Address 34:
In this address, the CCU has to load the HSP RAM address to which the CCU wants to write.

Address 35:
In this address, the CCU has to load the HSP RAM address which the CCU wants to read from.

Address 36:
This address is used to send or to receive data to or from the HSP.

Address 37:

	2	1	0
	DTC	RR	WR

LSB

This status byte contains three status flags about the HSP transmission status:

Bit 0 (WR) Write Request
If this bit is set, an IM bus 34 Write has occurred.
If this bit is reset, HSP input of data is enabled.

Bit 1 (RR) Read Request
If this bit is set, an IM bus 35 Write has occurred.
If this bit is reset, an IM bus 36 read has occurred.

Bit 2 (DTC) Data Transmission Control
If this bit is set, an IM bus 36 Write has occurred, or the HSP has written data into IM bus 36. If this bit is reset, an IM bus 36 Read has occurred, or the HSP has read data from IM bus 36.

Figs. 3–25 and 3–26 give the normal data transfer sequence for reading or writing the HSP's RAM. Because the maximum time of the HSP to be ready for the next read or write instruction after end of CCU data transmission is 50 µs max., the check of HSP status can be omitted with slow CCU operations.

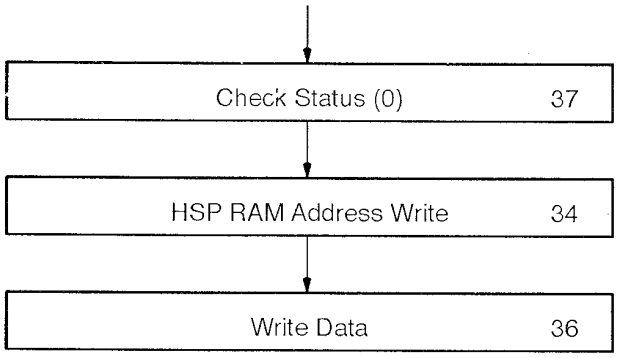

Fig. 3–25: Sequence for writing to the HSP RAM

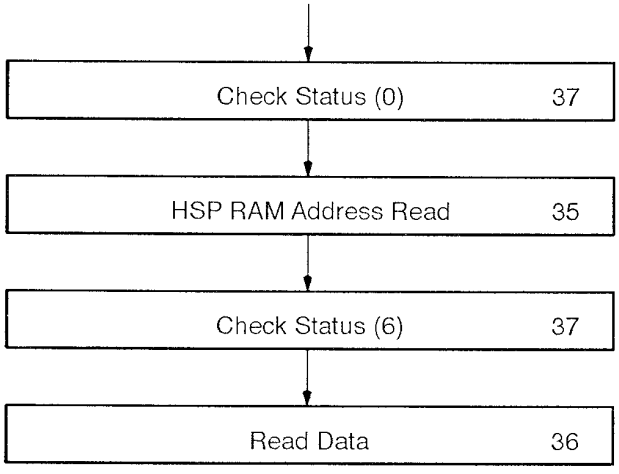

Fig. 3–26: Sequence for reading from the HSP RAM

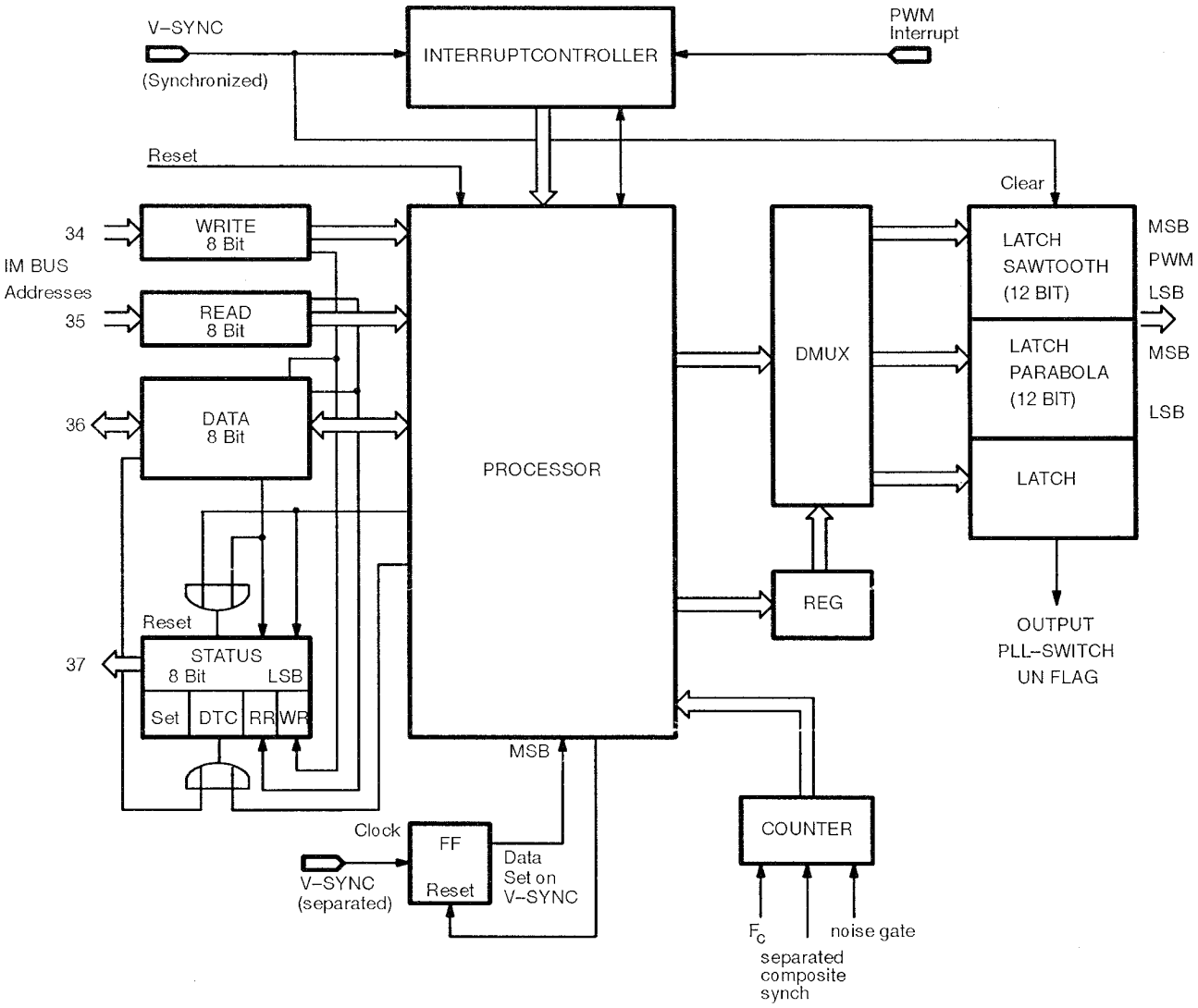

Fig. 3–27: Hardware of the HSP high–speed processor

4. Application Notes

4.1. Clamping Circuit

The resolution and the speed of the clamping loop can be adjusted by changing the coupling capacitor. As this capacitor is charged and discharged by current pulses which have a constant amplitude, the maximum change of the video signal's DC level during one horizontal period is directly correlated to that capacitance and should be set to a maximum of 10% of one A/D converter increment, e.g. < 1.5 mV, to avoid voltage ripple on the video signal. The DC current level of the external clamping circuit is given by the maximum base current of the A/D converter input (< 5 µA) and the worst case leakage current of the P.C. board. It should be chosen four times higher at least. Regarding this, the average current through the resistor between the VCU's video input and the 12 V supply should be chosen at about 20 µA, and the current for the discharging pulses, given by the resistor between video input and clamping output of the DPU, should be

$$\frac{64\ \mu s}{0.8\ \mu s} \cdot 2 \cdot 20\ \mu A = 3\ mA.$$

With this, typical application values are:
resistor to 12 V supply = 270 kΩ
resistor to clamping output = 1.8 kΩ
coupling capacitor = 2.2 µF

For non–standard signals without a back porch, there is an automatic switch in the DPU which disables back porch level clamping if the back porch level is too high compared with the sync top level. Control register "SK" serves for selecting the back porch level at which the clamping automatic switch will disable the back porch clamping mode. For example, SK = 7 means: if the back porch is 750 mV above the sync top level, only peak level clamping is possible. This measurement is performed in the peak level clamping mode only.

4.2. Horizontal Sync Separation

In order to achieve a sufficient phase resolution, the horizontal PLL needs the full 7–bit amplitude information of the horizontal sync pulses. In the synchronous mode (UN = 0), the PLL takes as sync reference all video samples that are lower than the 50% level of the sync amplitude. To achieve a better phase resolution by taking more sync pulse samples, the separation level is set to 50% plus eight A/D increments by means of control register "S 50" set to 0. If the gate is switched off by non–standard signals (with ST = 0), S 50 should be set to 1 to have a separating level of exactly 50% to avoid modulation caused by the video content.

In the peak level clamping mode, the control register "UAB" should be set to "1" to achieve a better phase resolution. At UAB = 0 and peak level clamping mode, the sync separation level is set to 125 mV above sync top, the phase resolution being reduced. At UAB = 1, the separation level is set to 250 mV above sync top, which gives an increased phase resolution. The UAB register should be set to 1 (by the CCU) only if the DPU is in the synchronous mode (UN = 0). With UAB = 1, the PLL is able to lock with a minimum sync pulse amplitude of only 220 mV. With non–standard signals, especially with VCR operation, the noise gate which eliminates all influencing of the horizontal PLL by noise during the horizontal sweep, should be switched off by ST = 0. This is recommended because the signal from most video tape recorders contains phase steps.

4.3. Vertical Sync Separation

By means of control register "BIN", the integration time for the vertical sync signal can be selected in four steps. The shortest integration time (BIN = 0) may be chosen for non–standard signals, e.g. copy–protected video tape signals with very short vertical sync pulses. In all other cases, the register should be set to BIN = 2 or 3 to have the maximal noise immunity.

Table 4–1: Matrix for control register "SK"
The voltage levels are given for the Video Amp I of the VCU

Register Value	Maximum Black Level given in A/D Increments	Maximum Difference Between Sync Top Level and Back Porch Level, given in mV
0	36	437
1	38.8	480
2	41.6	524
3	44.4	567
4	47.1	611
5	49.9	654
6	52.7	698
7	55.5	741
and so on in steps of:	2.78 Incre.	43.5 mV
until		
15	77.7	1098

Table 4–2: Matrix for control register "BIN"

Register Value	Integration Time Given in Main Clock Periods and in µs			
	PAL (17.7 MHz)		NTSC (14.4 MHz)	
	Clock P.	µs	Clock P.	µs
0	143	8	114	8
1	213	12	172	12
2	621	35	501	35
3	798	45	644	45

4.4. Synchronism Detector

As explained in section 3.3.4. by means of CCU register "SLP" the level can be selected, at which the horizontal PLL is switched to the asynchronous state. In the latter, the PLL filter is switched to wide band characteristic, the noise gate centered to horizontal sync is switched off, and the clamping circuit is forced to peak level clamping. The status can be read from CCU register "UN".

4.5. PLL Filter Characteristics

If the PLL is in the non–synchronous mode, the filter characteristic of the PLL loop is switched to wide band (filter characteristics II or IV, see Fig. 4–1). If filter II is selected (register FUN must be set to 0), the PLL has the maximum pull–in speed when the received station is changed. With filter IV (FUN = 1), the PII has a longer pull–in time, but gives less phase jitter caused by very weak signals or without reception of a TV signal. With UN = 1 the clamping circuit is forced to peak level clamping, and the noise gate centered on the horizontal sync pulse is switched off (see Table 4–3,matrix for register "FUN").

If the PLL is in the synchronous mode (UN = 0), the following filter characteristics can be selected as initial values or by means of a CCU command (see Figs. 4–1 and 4–2, frequency values related to the 1H video signal):

Filter I(FI 1 = 0), large time constant
– first corner frequency = 2.5 Hz
– maximum noise reduction
– attentuation for high frequencies = 16
– limited pull–in range of ±100 Hz
– slow transient response

This selection should be used with standard signals and for optimum noise immunity with weak signals.

Filter II, III, IV(FI 1 = 1, 2, 3)
– first corner frequencies

Filter II: 80 Hz

Filter III: 20 Hz

Filter IV: 40 Hz
– full pull–in range of ±800 Hz
– limited noise reduction
– attenuation at high frequencies = 2.5 to 3.5

These filters should be selected for signals from video tape recorders. They differ slightly with respect to the phase step answer of the PLL.

For standard signals it is suggested that the following control register values are chosen:

P = B = 0 SK = 15	switches to peak level clamping at horizontal sync amplitudes greater than 1.089 V
FUN = 0	filter II with non–synchronous PLL
FI 1 = 0	filter I for optimum noise immunity
S 50 = 0	separating level is 120 mV higher than the 50% level of the sync amplitude, for optimum phase resolution of the PLL
ST = 1	noise gate is switched on to avoid jitter caused by the video content or by noisy signals
UAB = 0	minimum sync amplitude of 120 mV for pulling–in the PLL

For non–standard signals, e.g. originating from video tape recorders or home computers, it is suggested that these register values are changed by CCU command as follows:

FUN = 0	filter II with non–synchronous PLL
FI 1 = 3	filter IV for quick transient response especially with phase steps in video tape signals
S 50 = 1	separating level at 50% of the sync amplitude to avoid phase jitter from the video content caused by the switched–off noise gate (with ST = 0)
ST = 0	noise gate is switched off to control large phase steps in video tape signals, especially during the vertical flyback time
UAB = 1	after the PLL has locked–in, the CCU should set this register to 1for a better phase resolution with peak level clamping
VA = 1	the color–locked mode of the horizontal PLL should be disabled with non–standard signals

not changed: P = B = 0, SK = 15, RF = 1

Table 4–3: Matrix for filter register "FUN"

Register Value	Filter Selection with UN = 1
0 1	II IV

Table 4–4: Matrix for filter register "FI 1"

Register Value	Filter Selection with UN = 0
0	I
1	II
2	III
3	IV

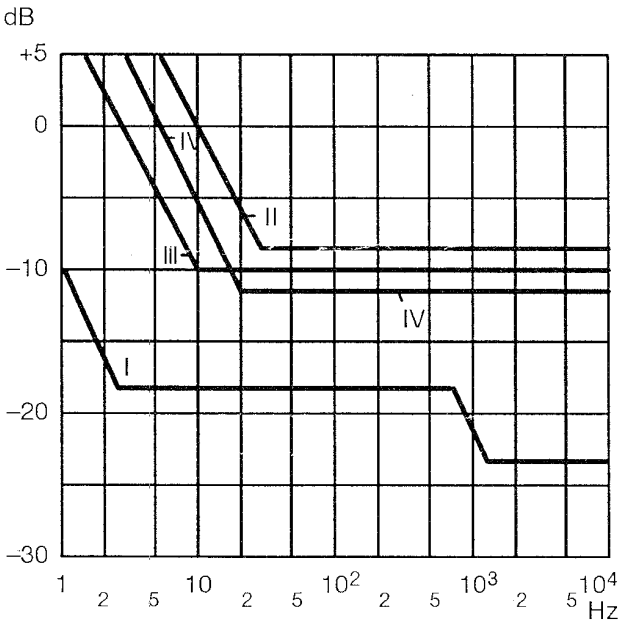

Fig. 4–1: Characteristics of the PLL phase filter for selections I to IV

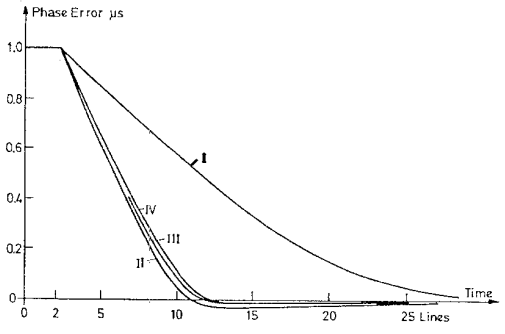

Fig. 4–2: Phase step response of the horizontal PLL circuit (Loop I and Loop II) with FI 2 = 0 and the filter sections I to IV (FI 1 = 0 to 3)

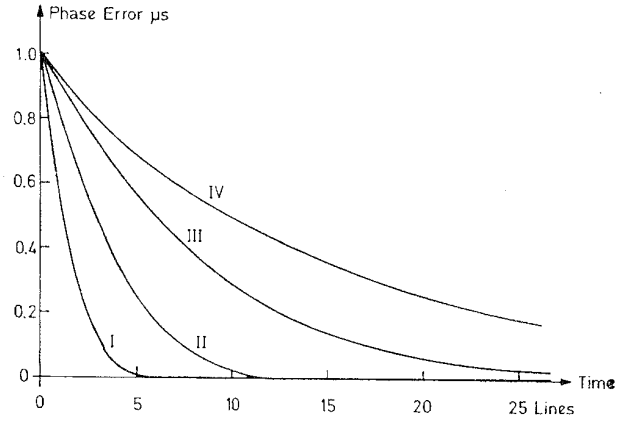

Fig. 4–3: Transient response of the second control loop for the selections I to IV

4.6. Blanking Pulses and Phase Adjustment

With register CB = 2, the horizontal blanking pulse from pin 6 has a constant phase position and pulsewidth (see Fig. 3–26). If CB is set to 3, pin 6 will supply a low level for the time the horizontal flyback input pin 7 is high. With register CB = 1, blanking is performed by the flyback pulse at pin 7 only. This means an additional blanking by the flyback pulse. By means of register "VBL" the vertical blanking time can be selected.

To set the correct phase position of the horizontal blanking pulse, the following sequence is recommended:

- set register CB 2 (blanking without flyback)
- by means of register BP adjust symmetrical position of the blanking pulse at pin 6 with respect to the blanking time in the video signal at the cathodes of the CRT
- adjust symmetrical position (horizontal) of the picture in the screen by means of register SP

Table 4–5: Matrix for control register "VBL"

Register Value	Vertical Blanking Pulsewidth given in Horizontal Periods	
	with BIN = 0 or 1	with BIN = 2 or 3
0	13	12.5
1	14	13.5
2	16	15.5
3	17	16.5
4	18.5	18
5	19.5	19
6	21.5	21
7	22.5	22

Table 4–6: Matrix for control register "BP" with S_p = 16

Register Values		Phase of the Delayed Horizontal Blanking Pulse (t_{az2}), given in Clock Periods of the ΦM Main Clock	
BPE	**BP**	**PAL**	**NTSC**
0	0	68	58
0	1	64	54
.	etc. until		
.	16	4	–6
.	17	0	–10
.	18	–4	–14
.	19	–8	–18
.	etc. until		
.	31	–56	–66
.	etc. until		
0	63	–184	–194
1	0	–188	–198
1	20	–264	–274

The typical BP register values are:
for PAL, NTSC and SECAM:
BP = 52 (with SPU processor in the system)
for RGB operation:
BP = 0

4.6.1. 16:9 Picture Tube Format

For applications with 16:9 picture tubes, the beginning and end of the vertical blanking pulse (pin 22) can be changed with the registers VBT (V–Blank–Top Screen) and VBB (V–Blank–Bottom Screen) to blank the video signal during the 'overscanning' time.

With register EVB, variable blanking can be disabled when EVB = 0 (default).

4.7. Control Loop II

By means of control register ZM, the phase comparator II can be changed from measuring the phase of the flyback pulse's leading edge (with ZM = 0) to measuring the phase of the flyback pulse's center (with ZM = 1). With the latter condition, the horizontal phase will not change at symmetrical modulation of the flyback pulsewidth and amplitude caused by extreme brightness amplitude in the video output stages.

The speed of the control loop II can be changed by setting the filter register FI 2. The settings ZM = 1 and FI 2 = 1 are recommended.

Table 4–7: Matrix for filter register "FI 2"

Register Value	Filter Selection
0	I
1	II
2	III
3	IV

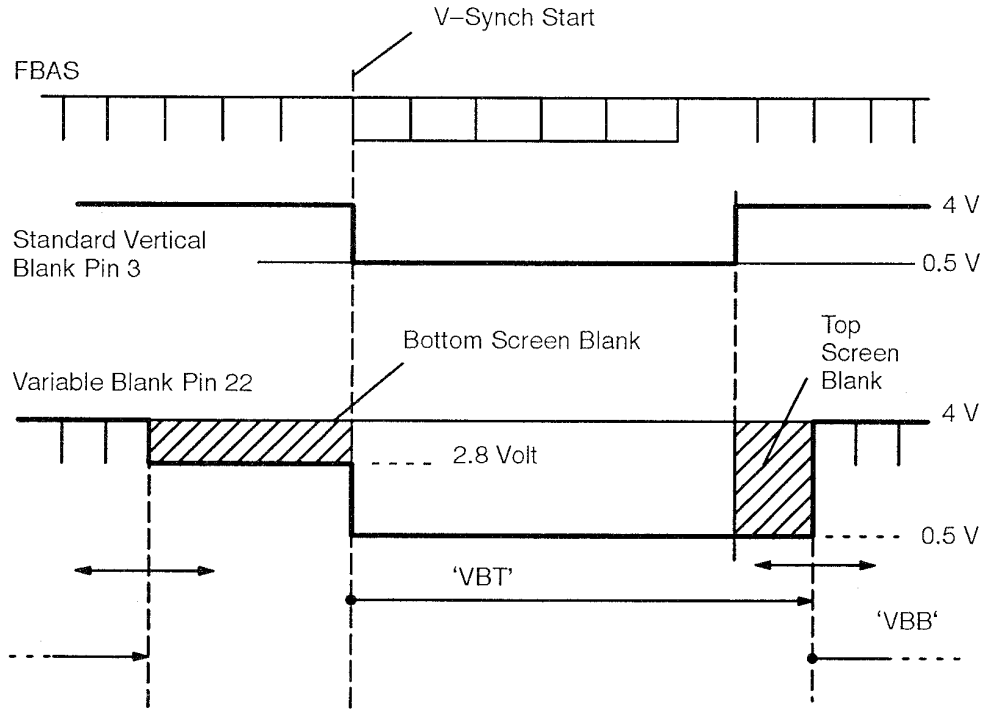

Fig. 4–4: Variable V–blank for 16:9 picture tubes at pin 22

4.8. Analog RGB Signals

For using the DPU with an analog generated RGB signal, the horizontal and vertical sync pulses (composite sync signal) must be fed to one of the two video inputs of the VCU... Video Codec. By means of register "BP", the phase of the horizontal blanking pulse at pin 6 of the DPU must be adjusted to the correct phase with respect to the RGB signal.The horizontal phase of the flyback pulse with respect to the video signal can be adjusted in the range of ±3.5 µs by means of register "SP". The registers BP and SP can be used for an application with a different video processor, and a different video processing time (see Table 4–6).

4.9. Changing the Standard

For changing the TV standard, the main clock frequency $f_{\Phi M}$ must be changed. This can cause a loss of data in the DPU. To avoid this, the start oscillator (see section 3.4.) has been implemented which is driven by a 4 MHz clock applied to pin 34, and which provides a stable horizontal output pulse at pin 31 during clock frequency change. Additionally, the DPU requires a reset signal after every changing of the clock signal. This reset signal can be applied to pin 5 by hardware from a CCU port (at this time, pin 36 must be at +5 V), or the register "RES" must be set to 1 for a short time (10 µs min.) by CCU software.

After the reset described, the DPU supplies a 15.5 kHz output pulse at pin 31, until the new CCU data is received (with FL = 0). The following sequence is recommended for changing the main clock frequency $f_{\Phi M}$:

- set register FL = 1
- delay of min. 2 ms
- set register RES = 1
- change the clock frequency $f_{\Phi M}$
- set register RES = 0 after the clock frequency is stabilized
- set registers for the new standard with new ZN value and registers SC = 1 and FL = 0, to get synchronized horizontal output pulses at pin 31. Register FL must not be changed to 0 before the ZN register is changed to the correct value.
- set blanking register BL back to 0

5. Control and Status Registers

The following Tables 5–1 to 5–6 show the organization of the control and status registers, horizontal and vertical. For data transfer, it is assumed that 16 bits are transferred for each address, with the unused bits set to zero. The test mode is selected by "TE" = 2. Please note that the addresses of the CCU registers may be altered.

During the start–up sequence the CCU has to load the adjustment values for the vertical deflection into the RAM of the HSP high–speed processor. The parameters and addresses are shown in Table 5–6.

Table 5–1: Control and status registers
Typical register values are given in decimal figures. Values in brackets apply to NTSC with 14.3 MHz.

	IM Bus Address	Bit No. MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
Horiz. Control Register	32	SP Phase Shift								IL Output Pulsewidth			VGS Pin 19 Switch	SC Protection Circuit off	FL Start Oscill. free run	ZN Horizontal Standard	
		16								26			0	1	0	2(1)	
	33	FUN Filter for non–sync PLL	FI 1 PLL Filter		ST Noise Gate	FI 2 Filter for Control Loop II		SA SE PLL Mode Switch		ZM Center of Flyback	VE VA Color–locked Mode Switch		BL Blanking Pin 6	RF Noise Filter	UHD Disable Pin 8	CLD Clamp. Disable	X
		0	0		1	1		0		1	0	1	0	1	0	0	
	41	TE Test Mode Enable		S50 Sync. Separ. Level	UAB Peak Level Separ.	SK Max. Back Porch Level				P B Clamping Switch		IOP Interlace Option		RES Reset	VBE	ASK Old Skew Data	X
		1		0	0	15				0		0	0	0	0	0	
	42	CB Comp. Blank.	BP Horizontal Blanking Phase							IMS	BPE	X	X	X	X	X	X
		3	52							0	0						
Vertical Control	34	*)								HSP RAM Address Write							
	35	*)								HSP RAM Address Read							
	36	*)								HSP Data I/O							
	37	*)								HSP Status							
	38	GH Lock–Out Time		FF Lock–In Time	KA Disable Lock Mode	NC Vertical Standard	AE Trigger Window	TI Vertical Sync Pin 38	ZS Inter–lace on/off	FZ 2x Hor. Freq. Pin 39	VB Force to Locked Mode	BIN Vertical Sync. Integration Time	VBL Vertical Blanking Pulsewidth				DVS 2 V mode
		2		1	0	0(1)	0	1	1	1	1	2	4(0)				0
	47	EVB Enable Variable V–Blank	VBT Vertical Blanking Top Screen						VBB Vertical Blanking Bottom Screen								
Status Reg.	Horiz. 39									T8 Test					PI Clam–ping status	UN Synchr. Detec–tor	VU Stan–dard Signal detector
	Vert. 40														TF Measu–ring Window	AE Working Window	AO Vertical Locked

*) for addresses 34 to 37, the HSP registers are only 8–bit wide

X = Bits must be set to zero for receive registers and are "don't care" for transmit registers.

Table 5–2: Control register horizontal (IM Bus)

IM Bus Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
32	ZN	0 to 1	1	–	horizontal standard 0 = Text display mode, 60 Hz,624 lines 1 = NTSC, 60 Hz, 525 lines, 2 = PAL, 50 Hz, 625 lines, 3 = D2–MAC mode, PAL with $f_{\Phi M}$ = 20.25 MHz
32	FL	2	1	0	1 = the protection circuit is free–running **DPU 2553** at 15.500 kHz and **DPU 2554** at 31.00 kHz, and the output frequency at pin 31 is not synchronized or influenced by the video signal (e.g. for Teletext)
32	T1	2	1	0	only active in test mode. In this case, FL is out of function. 0 = input for externally–separated sync pulses (pin 6) 1 = output for the separated composite sync signal (pin 6)
32	SC	3	0	1	disables the protection circuit in the same way as pin 33 being at low or high potential. 0 = normal protection function 1 = protection circuit disabled
32	VGS	4	0	0	1 = the undelayed horizontal blanking pulse at pin 19 is switched off (High state) during the vertical blanking time (22 lines). Due to this, the gain of the input amplifier of the VCU video codec is not doubled during vertical blanking. 0 = the undelayed horizontal blanking pulse at pin 19 is valid continuously.
32	IL	5 to 10	27 (16 with DPU 2554)	26	duration of the horizontal output pulses at pin 31: **DPU 2553:** 1 to 63 µs in steps of 1µs **DPU 2554:** 1 to 31 µs in steps of 1µs. Values exceeding 31 are identical to (IL–32).
32	SP	11 to 5	16	16	phase position between center of sync pulses and leading edge of horizontal flyback pulse with ZM = 1 and flyback pulse duration of 12 µs (PAL) or 10.9 µs (NTSC) or 6 µs (**DPU 2554**, PAL) or 5.45 µs (**DPU 2554**, NTSC) **PAL and SECAM:** **DPU 2553** 0:t_{SZ} = –3.83 µs; 31:t_{SZ} = +3.15 µs in steps of 0.225 µs **DPU 2554**, ZM = 1 0:t_{SZ} = +1.01 µs; 31:t_{SZ} = +4.5 µs in steps of 0.112 µs **DPU 2554**, ZM = 1 0:t_{SZ} = –2.02 µs; 31:t_{SZ} = +1.5 µs in steps of 0.112 µs **NTSC:** **DPU 2553** 0:t_{SZ} =–5.4 µs; 31:t_{SZ} = +3.2 µs in steps of 0.28 µs **DPU 2554**, ZM = 0 0:t_{SZ} =–0.56 µs; 31:t_{SZ} = +3.8 µs in steps of 0.14 µs **DPU 2554**, ZM = 1 0:t_{SZ} =–2.8 µs; 31:t_{SZ} = +1.55 µs in steps of 0.14 µs

Table 5–2: Control register horizontal, continued

IM Bus Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
33	CLD	1	0	0	1 = the clamping outputs pin 4 and pin 21 are set to high impedance state (disabled clamping)
33	UHD	2	0	0	1 = pin 24 is switched to the high impedance state (used in D2–MAC mode)
33	RF	3	0	1	additional noise filter during sweep–time for non–standard signals 1 = noise filter active
33	BL	4	1	0	1 =blanking mode, switches pin 22 to high impedance. The maximum voltage at pin 22 is set to 2.8 V by the VCU.
33	VA	5	0	0	1 = locking of the horizontal frequency with the color subcarrier is disabled. The standard signal detector switches automatically if VA=VE=0.
33	VE	6	1	0	1 = locking of the horizontal frequency with the color subcarrier is active. The standard signal detector switches automatically if VA=VE=0.
33	ZM	7	0	1	1 = the center of the flyback pulse instead of the leading edge is taken as reference for the phase comparator II.
33	SE	8	0	0	1 = horizontal PLL is forced to synchronous operation, i.e. large PLL filter time constant and back porch clamping of the composite video signal
33	SA	9	0	0	1 = horizontal PLL is forced to non–synchronized operation, i.e. small PLL filter time constant and peak clamping of the composite video signal. The synchronism detector switches automatically, if SE and SA = 0
33	FI2	10 to 11	2	1	selection of the filter time constant for the phase comparator II: 0 = smallest time constant 3 = largest time constant
33	ST	12	1	1	0 = noise gate for the horizontal PLL is switched off
33	FI1	13 to 14	0	0	Selection of the filter time constant for the phase comparator I
33	FUN	15	0	0	filter selection for non–synchronous PLL (with UN = 1)

Table 5–2: Control register horizontal, continued

IM Bus Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
41	ASK	1	0	0	1 = at pin 7 is the output of the skew data which is compatible with the DPU 2540 0 = see Fig. 3–8
41	VBE	2	0	0	1 = at pin 3 is the output of the single–scan vertical blanking pulse at vertical double–scan mode. 0 = pin 3 is in the high–impedance state
41	RES	3	0	0	1 = software reset. Has the same effect as if pin 5 is taken to ground, except the following: Pin 36 is set to +5 V internally, to get horizontal output pulses at pin 31 with 4 MHz at pin 34. This is required after changing the main clock frequency $f_{\Phi M}$ between 14, 17 or 20 MHz.
41	IOP	4 to 5	0	0	with "DVS" = 0: 1 = the interlace control output pin 39 is enabled (see Figs. 3–9 and 3–10) with "DVS" = 1: 0 = full interlace mode (pin 39 in high–impedance mode) 1 = non–interlace mode 2 = semi–interlace mode
41	B	6	0	0	1 = clamping circuit is forced to back porch clamping
41	P	7	0	0	1 = clamping circuit is forced to peak level clamping. The clamping circuit is switched automatically if P = B = 0
41	SK	8 to 11	7	15	Selection of the maximum difference between sync top and back porch level for back porch clamping
41	UAB	12	0	0	1 = higher sync separation level for the horizontal PLL with peak level clamping
41	S50	13	0	0	1 = the additional offset to the 50% separation level for the horizontal PLL is switched off
41	TE	14 to 15	0	0	2 = test mode is enabled 0, 1 or 3 = normal operation
42	BPE	6	0	0	1 = an offset of 256 clock periods delay to the "BP" value is selected
42	IMS	7	0	0	0 = all IM bus addresses are enabled (default) 1 = all IM bus addresses are disabled with exception of address 42
42	BP	8 to 13	18	52 with SPU and DTI	phase of the delayed horizontal blanking pulse at pin 22
42	CB	14 to 15	3	3	selects three different modes of horizontal blanking: 0 = no blanking 1 = blanking is performed with the flyback pulse at pin 23 only. This option can also be used for RGB video applications. 2 = blanking is performed only with the standard blanking pulse which can be phase–shifted by register "BP" 3 = blanking is performed with the standard blanking pulse and the flyback pulse of pin 23

Table 5–3: Control register vertical (IM Bus)

IM Bus Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
34	HSPW	0 to 7	–	–	HSP write address
35	HSPR	0 to 7	–	–	HSP read address
36	HSPD	0 to 7	–	–	HSP Data port
37	HSPS	0 to 7	–	–	HSP status Byte
38	DVS	0	0	0	1 = vertical double–scan frequency is selected (100 Hz or 120 Hz) 0 = vertical display frequency 50 Hz or 60 Hz is selected
38	VBL	1 to 3	4	PAL 4 NTSC 0	Selection of the vertical blanking pulsewidth
38	BIN	4 to 5	2	2	Selection of the integration time for the vertical sync
38	VB	6	0	1	0 = locking of the vertical frequency with the horizontal frequency switched on, if KA = 0. In the case VB = 1 and KA = 0, the DPU switches to locked operation automatically.
38	FZ	7	1	1	only active in test mode
38	ZS	8	1	1	0 = the interlace is switched off, e.g. for Teletext with DC coupled vertical output stages
38	TI	9	1	1	only active in test mode
38	AE	10	0	0	1 = wide trigger window (vertical) is selected
38	NC	11	0	–	1 = 525–line standard is selected 0 = 625–line standard is selected
38	KA	12	0	0	1 = locking of the vertical frequency with the horizontal frequency is disabled
38	FF	13	1	1	1 = smallest time constant is selected (ca. 1.7 s) for switching–on the vertical locking 0 = large time constant is selected (ca. 3.3 s)
38	GH	14 to 15	2	2	Time constant for switching–off the vertical locking: 0 = 67 ms, 1 = 134 ms, 2 = 200 ms, 3 = 270 ms
47	VBB	0 to 8	0	–	selection of bottom screen blanking phase in steps of 1 horizontal line
47	VBT	9 to 14	0	–	selection of top screen blanking phase in steps of 1 horizontal line
47	EVB	15	0	–	1 = enabled of the variable vertical balnking at pin 22 with registers VBB and VBT for 16:9 screen format applications

Table 5–4: Status register horizontal

IM Bus Address	**Abbreviation of parameters**	**Bit No. (LSB = 0)**	**Function**
39	VU	0	1 = locking between horizontal frequency and clock frequency is operating 0 = locking is not in use
39	UN	1	1 = the horizontal PLL is not synchronized 0 = synchronized
39	PI	7	1 = peak level clamping is in operation. If the horizontal PLL is synchronized (UN = 0), this also means that the difference between sync top and back porch level is greater than the selected level in register "SK". 0 = back porch clamping is in operation
39	T8	3 to 7	for test purposes

Table 5–5: Status register vertical

IM Bus Address	Abbreviation of parameters	Bit No. (LSB = 0)	Function
40	A0	0	1 = the vertical output frequency is locked to the horizontal frequency
40	AE	1	0 = the working–counter of the vertical synchronization is acting with the narrow trigger window
40	TF	2	1 = the trigger window of the measuring counter is closed

5.1. Status and Control Registers of the HSP Processor

Table 5–6: Addresses and parameters to be loaded into the RAM of the HSP high–speed processor, and HSP status to be read from the RAM

HSP RAM Address	Parameter	Typical Values DVS = 0 PAL 17.7 MHz	Typical Values DVS = 0 NTSC 14.3 MHz	Description
0 1	S_{0L}* S_{0H}	96 9	240 13	S correction, High Byte Low Byte
6 7	S_{1L} S_{1H}	200 0	200 0	Vertical Symmetry
8 9	H_{0L} H_{0H}	96 9	0 14	Vertical Slope
14	A_0	100	100	Vertical Phase
15 16	P_{0L}* P_{0H}	128 28	0 75	Curvature East–West Correction, Parabola I
21 22	Z_{0L} Z_{0H}	64 2	208 3	Trapezoidal Correction, Parabola I
23 24	P_{1L}* P_{1H}	128 7	128 7	Curvature East–West Correction, Parabola II
29 30	Z_{1L} Z_{1H}	80 7	32 0	Trapezoidal Correction, Parabola II
35	Y_0	100	100	Horizontal Amplitude
38 39	k_1 k_2	40 134	27 89	Switchover Step from Parabola I to Parabola II, given in Calculation Steps of the HSP, Divided by 2 Switchover Step from Parabola II to Parabola I
47	Gate	120	96	Gate Pulsewidth for the Synchronism Detector given in ΦM Main Clock Periods
48 50	KS_1 KS_2	4 32	4 32	Weighting Factor for in–Gate Sync Pulses Weighting Factor for out–Gate Sync Pulses
59	FK	1	1	Coefficient for the Filter of the Synchronism Detector
61	SLP	20	20	Switching Level for the PLL Filter Switch
HSP Status RAM Addresses				
42	VP			Vertical Period of the Received Video Signal
63	SD			Output Information of the Synchronism Detector for Muting

* The minimum value for these Bytes is "1"

6. IM Bus

The INTERMETALL Bus (IM Bus for short) has been designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means that the CCU acts as a master whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, data is bidirectional. Bidirectionality is achieved by using open–drain outputs with On–resistance of 150 Ohm maximum.

The 2.5 kOhm pull–up resistor common to all outputs is in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 6–1; the times are specified under "Recommended Operating Conditions". In the high operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signals to Low level, indicating an address transmission, and sets the CL signal to Low level as well, to to switch the first bit on the data line. Thereafter, eight address bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits 8 to 16 clock pulses, and accordingly one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB.

The low clock level after the last clock pulse switches the line to High level. After this the completion of the bus transaction is signaled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

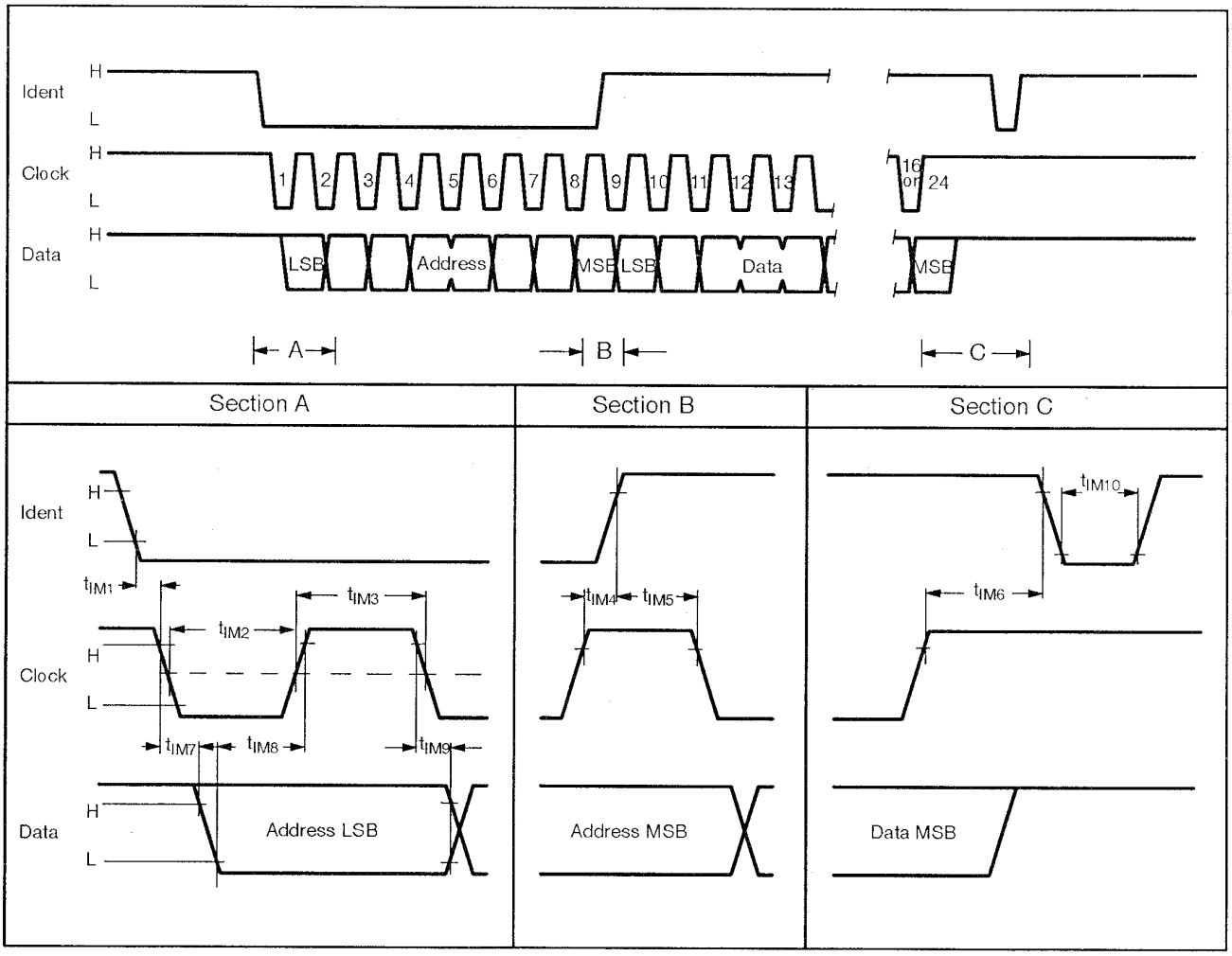

Fig. 6–1: IM bus waveforms

ITT Semiconductors Group
World Headquarters
INTERMETALL
Hans-Bunte-Strasse 19
D-7800 Freiburg
Tel. (0761) 517-0, Telex 772 715
Telefax (0761) 517-174

Printed in Germany
by A. Simon & Sohn, Freiburg (5/92)
Order No. 6251-329-2E

End of Data Sheet

Back to Summary

Back to Data Sheets ICs

Semiconductors