NCP1600

Product Preview
High Voltage PFC Controller with Standby Power Saving

The NCP1600 is an active power factor controller that functions as a boost pre–converter in off–line power supply applications. NCP1600 is optimized for low to medium power, high–density power supplies requiring a minimum board area, reduced component count and low power dissipation. The two comparators (C6, C7) are built in this device to improve power standby efficiency. With these two comparators, the PFC controller automatically switches itself in between normal mode and standby mode (skip or off mode) to save power consumption at light load.

The NCP1600 can pursuit follower boost operation that is an innovative mode allowing a drastic size reduction of both the inductor and the power switch. Ultimately, the solution system cost is significantly lowered. NCP1600 can also be working in a traditional constant output voltage mode, any intermediary solutions can be easily implemented. This flexibility makes it ideal to optimally cope with a wide range of applications.

Features
- Loseless Off–Line Start–Up
- Standard Constant Output Voltage or "Follower Boost" Mode
- PFC Enter Skip Mode and Off Mode at Light Load Condition
- Selectable Switching Frequency Clamp
- Disable Pin to Stop PFC Operation
- Restart Delay Timer
- Input UVLO with Hysteresis
- Feedback Loop Open Detection
- Output Overvoltage Comparator
- Switch Mode Operation: Voltage Mode
- Latching PWM for Cycle–by–Cycle On–Time Control
- Constant On–Time Operation That Saves the Use of an Extra Multiplier
- Totem Pole Output Gate Drive
- Improved Regulation Block Dynamic Behavior
- Internally Trimmed Reference Current Source
- Internal Leading Edge Blanking (LEB) for Noise Immunity

Typical Applications
- Monitor/TV Power Supplies
- PC Power Supplies
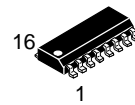- Notebook PC Adapters
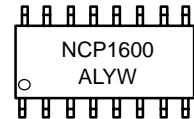- Medium Power Adapters

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MARKING DIAGRAM

SO–16
D SUFFIX
CASE 751B

NCP1600
ALYW

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS

AGnd	1	16	Line
Vref	2	15	NC
Restart Delay	3	14	Freq. Clamp
FB_In	4	13	Vcon
CS	5	12	CT
Mir_Out	6	11	VCC
Vth	7	10	Gate
STB	8	9	PGnd
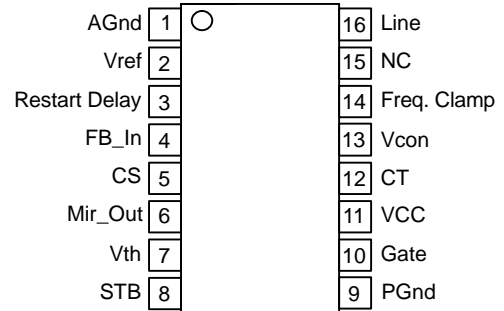
(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP1600D	SO–16	48 Units/Rail

NCP1600

NCP1600

Line
16

"Suffer 25 V$_{max}$"

Q1
Z15V

V$_{REF}$

RD
3

Q2

Output_Ctrl

BK2
Timer

Q   R

BK1

V$_{REF}$ V$_{REF}$
                 Enable
I$_{REF}$ I$_{REF}$

C1
UVLO

V$_{CC}$
11

15 V/10 V

A$_{Gnd}$
1

RS Latch

−60 mV

Output
C2

S   Q
R
R   FF1
R
R $\overline{Q}$

Th_Stdwn

Q3
Gate
10
Q4

I$_{REF}$ (205 μA)
ICS2

V$_{REF}$
2

3   2
NOR2
4   1
5

High

P$_{Gnd}$
9

ON

L.E.B.
BK3

SW2

NOR1

Output_Ctrl

OR1

Frequency
Clamp
BK4

FC
14

CS
5

11 V

NT1

C5
Output

AND1
3

1   2

UVP
+   C3
−

Output

1 V

OVP
−   C4
+

Output

3.8 V

BK5
V$_{REF}$
V$_{REG}$
IO

V$_{Con}$
13

CT
12

15 pF

11 V

SW1

Output_Ctrl

ON

IO
IO

IO   I$_{REF}$

Gnd

STB
8

Output
C7
−
+

0.5 V

Output   C6
−   +

Iosc−ch=2*Io*Io*/Iref

ICS1
I$_{REF}$

FB In
4

11 V

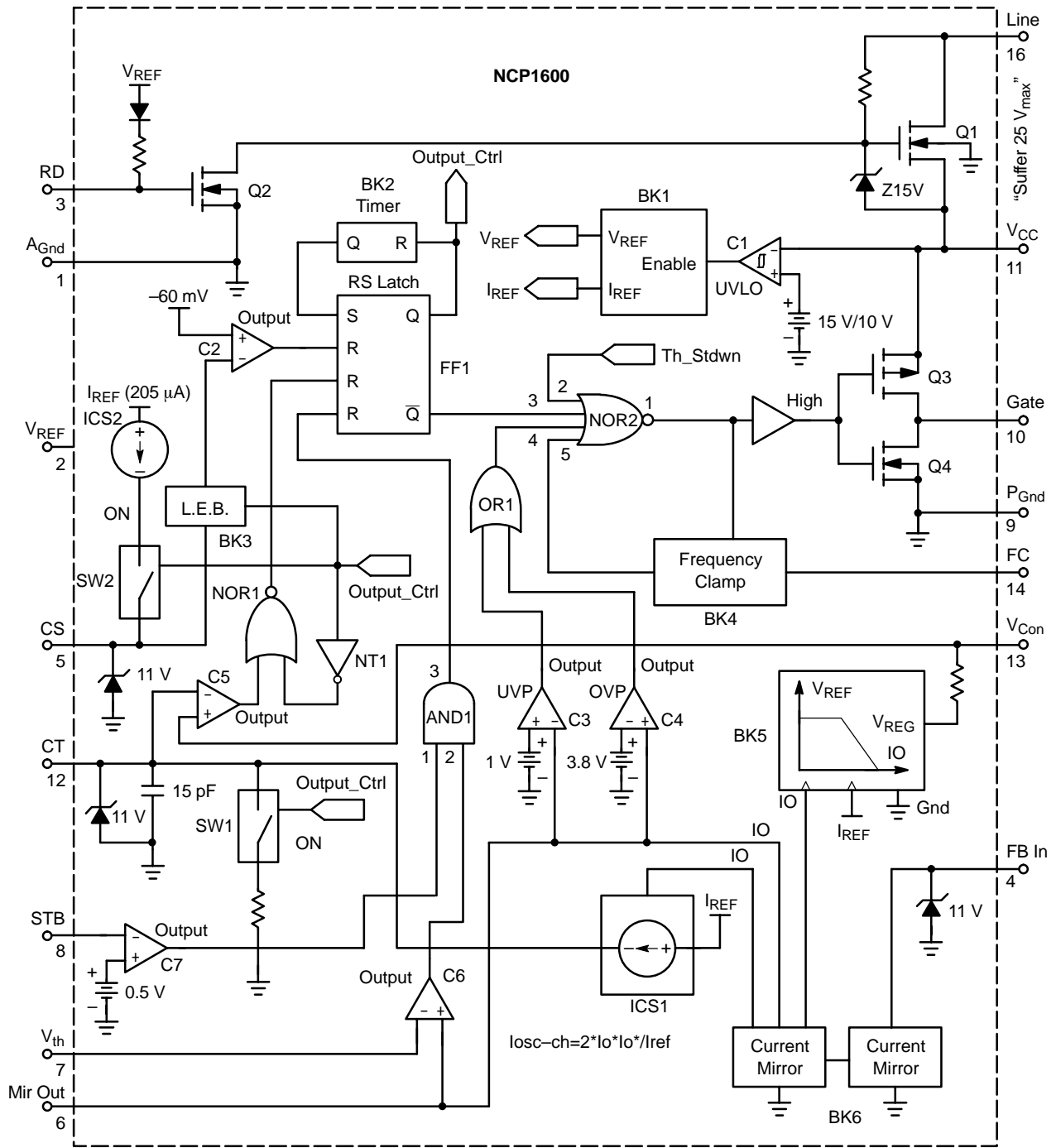V$_{th}$
7

Mir Out
6

Current
Mirror

Current
Mirror

BK6

Figure 1. Detailed Block Diagram
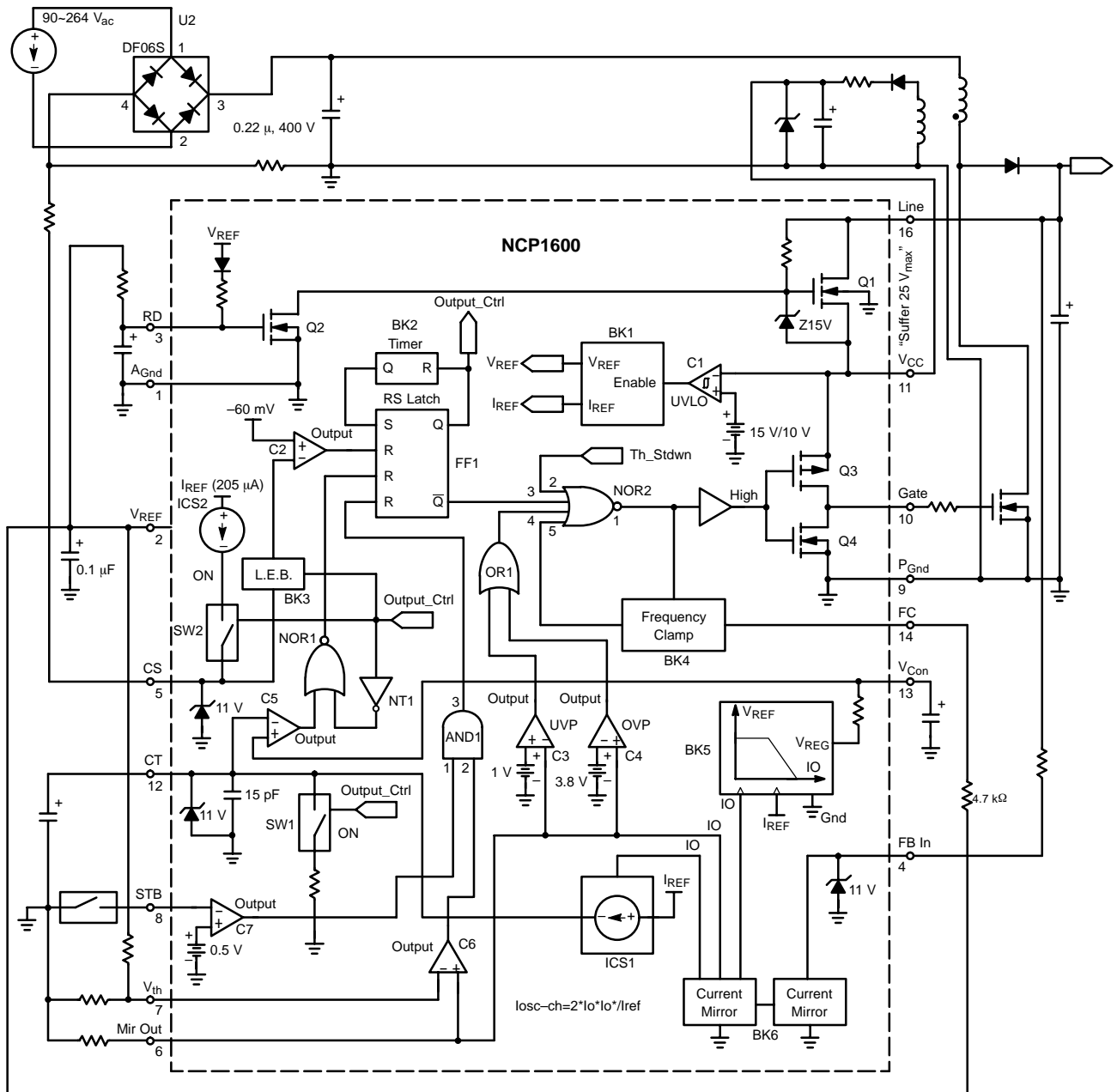
Figure 2. Representative Application Circuit

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	AGnd	Analog Ground.
2	Vref	Output reference voltage 6.5 V.
3	Restart Delay	This pin is high impedance input and the pin connecting R,C to setup the Delay Time. After this delay time, IC will turns off internal start–up FET Q1 during start–up.
4	FB_Input	This pin designed to receive a current that is proportional to pre–converter output voltage.
5	CS	This pin is designed to receive a negative voltage signal proportional to the current flowing through the inductor. This information is generally built using a sense resistor. The Zero Current Detection prevents any restart as long as the pin 5 voltage is below (–60 mV). This pin is also used to perform the peak current limitation. The resistor connected between the pin and the current–sense–resistor programs the overcurrent threshold.
6	Mir_Out	The Current Mirror output one current which is same to pin 4 (FB_Inut) input current. This current information is used for disabling PFC boost pre–converter at standby, Overvoltage and Undervoltage protection.
7	Vth	This pin divided the reference voltage to design the minimum threshold voltage of PFC Output Voltage during standby.
8	STB	PFC boost pre–converter standby pin. The PFC enters stand–by mode (PFC boost pre–converter enter both skip mode and off mode) when voltage at this pin falls below 0.5 V. This pin also can be connected to PWM feedback pin.
9	PGnd	Power Ground.
10	Gate	The gate drive current capability is suited to drive an IGBT or a power MOSFET.
11	VCC	This pin is the positive supply of the IC. The circuit turns on when VCC becomes higher than 15 V, the operating range after start–up being 8.0 V up to 30 V.
12	CT	The circuit uses an on–time control mode. This on–time is controlled by comparing the C_T voltage to the V control voltage. C_T is charged by the squared feedback current.
13	Vcon	This pin makes available the regulation block output. The capacitor connected between this pin and ground, adjusts the control bandwidth. It is typically set below 20 Hz to obtain a non–distorted input current.
14	Frequency Clamp	By connecting R.C. on this pin to setup the maximum switch frequency.
15	NC	No connection.
16	Line	This pin connects directly to the rectified AC line voltage source.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Transient)	V_{CC}	30	V
Power Supply Voltage (Operating)	V_{CC}	25	V
Line Voltage	V_{Line}	500	V
Input Voltage	V_{in1}	−1.0 to +10	V
Frequency Clamp Input	V_{in2}	−1.0 to +30	V
Restart Diode Current	I_{in}	5.0	mA
Output Current, Source or Sink	I_o	1.0	A

Power Dissipation and Thermal Characteristic
  D Suffix, Plastic Package Case 751B
  Maximum Power Dissipation @ T_A = 70°C
  Thermal Resistance, Junction–to–Air
	P_D
	$R_{\theta JA}$
		550
		145
			mW
			°C/W

Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: ESD data available upon request.
1. This device series contains ESD protection and exceeds the following tests:
  Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22–A114.
  Machine Model (MM) ±200 V per JEDEC standard: JESD22–A115.
2. Latch–up Current Maximum Rating: 150 mA per JEDEC standard: JESD78.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J–STD–020A.

ELECTRICAL CHARACTERISTICS (V_{CC} = 17 V, for typical values T_A = 25°C, for min/max values T_A = −25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATION SECTION					
Regulation High Current Reference	I_{ref}	195	200	205	µA
Ratio (Regulation Low Current Reference)/I_{ref}	I_{reg-L}/I_{reg-H}	0.965	0.97	0.98	−
$V_{control}$ Impedance	$Z_{vcontrol}$	−	300	−	kΩ
Feedback Pin Clamp Voltage @ I_{FB} = 100 µA Feedback Pin Clamp Voltage @ I_{FB} = 200 µA	V_{FB-100} V_{FB-200}	1.5 2.0	2.1 2.6	2.5 3.0	V
VOLTAGE REFERENCE					
Voltage Reference (I_O = 0 mA)	V_{ref}	6.4	6.5	6.6	V
Line Regulation (V_{CC} = 11 V to 25 V)	Reg_{line}	−	5.0	125	mV
Load Regulation (Io = 0 to 5.0 mA)	Reg_{load}	−	5.0	125	mV
Total Output Variation Over Line, Load and Temperature	V_{ref}	6.25	6.5	6.75	V
Maximum Output Current	I_O	5.0	10	−	mA
FREQUENCY CLAMP					
Frequency Clamp Input Threshold	$V_{th (FC)}$	1.9	2.0	2.1	V
Frequency Clamp Capacitor Reset Current (V_{FC} = 0.5 V)	I_{Reset}	0.5	1.7	4.0	mA
Frequency Clamp Disable Voltage	V_{DFC}	7.0	7.5	8.0	V
V_{CC} HYSTERESIS					
Start–up Threshold (V_{CC} Increasing)	$V_{th(ON)}$	14	15	16	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	9.0	10	11	V
Hysteresis	V_H	−	5.0	−	V
TIMER					
Minimum Off Time	t_{off}	1.5	2.1	2.7	µs

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 17 V, for typical values T_A = 25°C, for min/max values T_A = −25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Maximum Oscillator Swing	ΔVT	1.4	1.5	1.6	V
Charge Current @ I_{FB} = 100 μA	$I_{charge-100}$	87.5	100	112.5	μA
Charge Current @ I_{FB} = 200 μA	$I_{charge-200}$	350	400	450	μA
Ratio Multiplier Gain Over Maximum Swing	K_{OSC}	5600	6400	7200	1/(V,A)
Average Internal Oscillator Pin Capacitance Over Oscillator Maximum Swing (CT Voltage Varying From 0 up to 1.5 V)	C_{int}	10	15	20	pF
Discharge Time	T_{disch}	−	0.5	1.0	μS
CURRENT SENSE SECTION					
Zero Current Detection Comparator Threshold	V_{ZCD-th}	−90	−60	−30	mV
Negative Clamp Level (Ics–pin = −1.0 mA)	C_{I-neg}	−	−0.7	−	V
Bias Current @ Vcs = Vzcd–th	I_{b-cs}	−0.2	−	−	μA
Propagation Delay (Vcs > Vzcd–th) to Gate Drive High	T_{ZCD}	−	500	−	nS
Current Sense Pin Internal Current Source	I_{OCP}	192	205	218	μA
Leading Edge Blanking Duration	ι_{LED}	−	400	−	nS
Overvoltage Protection Propagation Delay (Vcs < Vzcd–th to Gate Drive Low)	T_{ocp}	100	160	240	nS
DRIVE OUTPUT					
Source Resistance (C_T = 0 V, V_{Gate} = 14 V) Sink Resistance (C_T = 2.0 V, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	17 4.0	25 10	40 17	Ω
Output Voltage Rise Time (10%–90%) (C_L = 1.0 nF)	t_r	−	50	200	ns
Output Voltage Fall Time (90%–10%) (C_L = 1.0 nF)	t_f	−	50	200	ns
Output Voltage in Undervoltage (V_{CC} = 10 V, I_{sink} = 1.0 mA)	$V_{O(UV)}$	−	−	0.25	V
OVERVOLTAGE PROTECTION SECTION					
Overvoltage Protection Threshold (C4 Comparator)	V_{C4}	3.75	3.8	3.85	V
Propagation Delay (Vpin6 > 3.8 V to Gate Drive Low)	T_{ovp}	−	500	−	ns
UNDERVOLTAGE PROTECTION SECTION					
Undervoltage Protection Threshold (C3 Comparator)	V_{C3}	0.95	1.0	1.05	V
Propagation Delay (Vpin6 < 1.0 V to Gate Drive Low)	T_{UVLO}	−	500	−	ns
STANDBY SECTION					
Standby Threshold (C7 Comparator)	V_{C7}	0.45	0.5	0.55	V
Propagation Delay (Vpin8 < 0.5 V to Gate Drive Low)	T_{ovp}	−	500	−	ns
THERMAL SHUTDOWN SECTION					
Thermal Shutdown Threshold	T_{stdwn}	−	150	−	°C
Hysteresis	ΔT_{stdwn}	−	30	−	°C
TOTAL DEVICE					
Line Start–up Current (V_{CC} = 0 V, V_{Line} = 50 V)	I_{SU}	5.0	16	25	mA
Line Operating Current (V_{CC} = $V_{TH(ON)}$, V_{Line} = 50 V)	I_{OP}	3.0	12.9	20	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF) V_{CC} Static Operating Current (Io = 0)	I_{CC}	− −	5.3 3.0	8.5 −	mA
Line Pin Leakage (V_{LINE} = 500 V)	I_{Line}	−	30	80	μA

DETAILED OPERATING DESCRIPTION

Introduction

The need of meeting the requirements of legislation on line current harmonic content, results in an increasing demand for cost effective solutions to comply with the Power Factor regulations. This data sheet describes a monolithic controller specially designed for this purpose.

Most off–line appliances use a bridge rectifier associated to a huge bulk capacitor to derive raw DC voltage from the utility AC line.
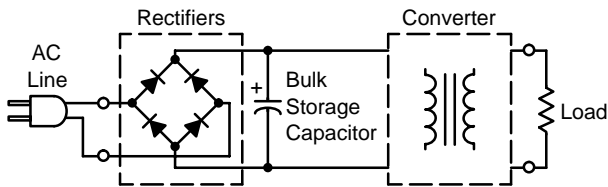

Figure 3. Typical Circuit Without PFC

This technique results in a high harmonic content and in poor power factor ratios. In effect, the simple rectification technique draws power from the mains when the instantaneous AC voltage exceeds the capacitor voltage.

This occurs near the line voltage peak and results in a high charge current spike. Consequently, a poor power factor (in the range of 0.5–0.7) is generated, resulting in an apparent input power that is much higher than the real power.
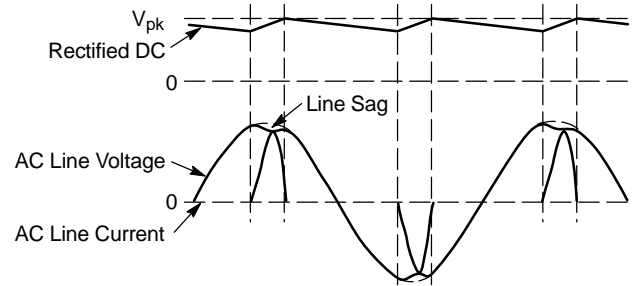

Figure 4. Line Waveforms Without PFC

Active solutions are the most popular way to meet the legislation requirements. They consist of inserting a PFC pre–regulator between the rectifier–bridge and the bulk capacitor. This interface is, in fact, a step–up SMPS that outputs a constant voltage while drawing a sinusoidal current from the line.

Figure 5. PFC Preconverter

The NCP1600 was developed to control an active solution with the goal of increasing its robustness while lowering its global cost.

Operating Description

The NCP1600 is optimized to just as well drive a free running as a synchronized discontinuous voltage mode.

It also features valuable protections (overvoltage and undervoltage protection, overcurrent limitation, ...) that make the PFC pre–regulator very safe and reliable while requiring very few external components. In particular, it is able to safely face any uncontrolled direct charges of the output capacitor from the mains which occur when the output voltage is lower than the input voltage (start–up, overload, ...).

In addition to the low count of elements, the circuit can be running in an innovative mode named "Follower Boost" that permits significant reduction of the size of the pre–converter inductor and power MOSFET. With this technique, the output regulation level is not forced to a constant value, but can vary according to the AC line

amplitude and to the output power. The gap between the output voltage and the AC line is then lowered, what allows the pre–converter inductor and power MOSFET size reduction. Finally, this method brings significant cost reduction. A description of the functional blocks is given below.

Regulator Section

Connecting a resistor between the output voltage to be regulated and the Pin 4, a feedback current is obtained.

Typically, this current is built by connecting a resistor between the output voltage and the Pin 4. Its value is then given by the following equation:

$$I_{pin4} = \frac{V_O - V_{pin4}}{R_O}$$

where:

R_O is the feedback resistor,

V_O is the output voltage,

V_{pin4} is the Pin 4 clamp value.

The feedback current is compared to the reference current so that the regulation block outputs a signal following the characteristic depicted in Figure 6.

According to the power and the input voltage, the output voltage regulation level varies between two values $(V_o)_{reg-L}$ and $(V_o)_{reg-H}$ corresponding to the I_{reg-L} and I_{reg-H} levels.
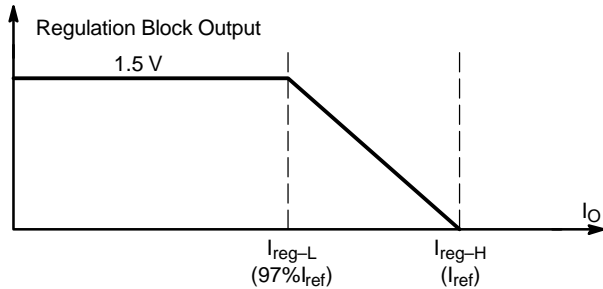

Figure 6. Regulation Characteristic

The feedback resistor must be chosen so that the feedback current should equal the internal current source I_{reg-H} when the output voltage exceeds the chosen upper regulation voltage $[(V_o)_{reg-H}]$. Consequently:

$$R_o = \frac{(V_o)regH - V_{pin4}}{I_{regH}}$$

In practice, Vpin3 is small compared to $(V_o)_{regH}$ and this equation can be simplified as follows (I_{regH} being also replaced by its typical value 200 μA):

$$R_o \approx 5 \times (V_o)regH \qquad \text{in } k\Omega$$

The regulation block output is connected to the Pin 13 through a 300 KΩ resistor. The Pin 13 voltage ($V_{control}$) is compared to the oscillator saw–tooth for PWM control. An external capacitor must be connected between Pin 13 and ground, for external loop compensation. The bandwidth typically set below 20 Hz so that the regulation block output should be relatively constant over a given AC line cycle. This integration that results in a constant on–time over the AC line period, prevents the mains frequency output ripple from distorting the AC line current.

Oscillator Section

The oscillator consists of three phases:

- Charge Phase: The oscillator capacitor voltage grows up linearly from its bottom value (ground) until it exceeds $V_{control}$ (regulation block output voltage). At that moment, the PWM latch output gets low and the oscillator discharge sequence is set.

- Discharge Phase: The oscillator capacitor is abruptly discharged down to its valley value (0 V).

- Waiting Phase: At the end of the discharge sequence, the oscillator voltage is that maintained in a low state until the PWM latch is set again.
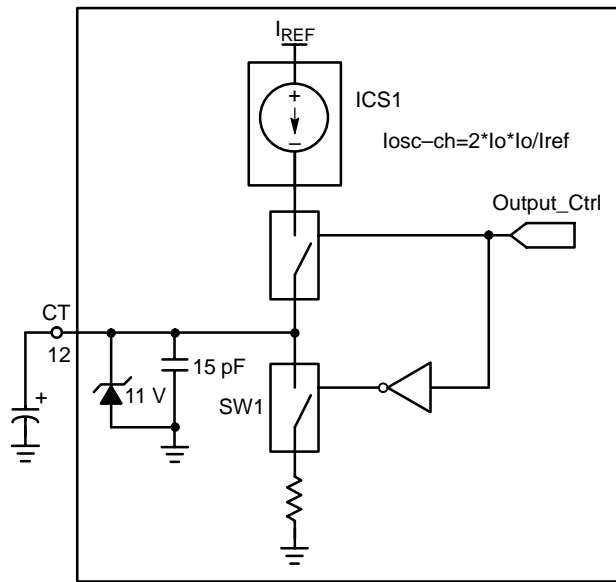

Figure 7. Oscillator

The oscillator charge current is dependent on the feedback current (Io). In effect:

$$I_{charge} = 2 \times \frac{I_o^2}{I_{ref}}$$

where:

I_{charge} is the oscillator charge current,

I_o is the feedback current (drawn by pin 4),

Iref is the internal reference current (200 μA).

So, the oscillator charge current is linked to the output voltage level as follows:

$$I_{charge} = \frac{2\,(V_o - V_{pin4})^2}{R_o^2 \times I_{ref}}$$

where:

V_o is the output voltage,

R_o is the feedback resistor,

V_{pin4} is the Pin 4 Clamp voltage.

In practice, V_{pin4} that is in the range of 2.5 V, is very small compared to V_o. The equation can then be simplified by neglecting V_{pin4}:

$$I_{charge} \approx \frac{2 \times V_o^2}{R_o^2 \times I_{ref}}$$

It must be noticed that the oscillator terminal (Pin 12) has an internal capacitance (C_{int}) that varies versus the Pin 12 voltage. Over the oscillator swing, its average value typically equals 15 pF (min 10 pF, max 20 pF). The total oscillator capacitor is then the sum of the internal and external capacitors.

$$C_{pin12} = C_T + C_{int}$$

PWM Latch Section

The NCP1600 operates in voltage mode: the regulation block output $V_{control}$ (Pin 13 voltage) is compared to the oscillator saw–tooth so that the gate drive signal (Pin 10) is high until the oscillator ramp exceeds $V_{control}$. The on–time is then given by the following equation:

$$t_{on} = \frac{C_{pin12} \times V_{control}}{I_{charge}}$$

where:

t_{on} is the on–time,

C_{pin12} is the total oscillator capacitor (sum of the internal and external capacitor),

I_{charge} is the oscillator charge current (Pin 12 current),

$V_{control}$ is the Pin 13 voltage (regulation block output).

Consequently, replacing I_{charge} by the expression given in the **Oscillator Section**:

$$t_{on} = \frac{R_o^2 \times I_{ref} \times C_{pin12} \times V_{control}}{2 \times V_o^2}$$

One can notice that the on–time depends on V_o (pre–converter output voltage) and that the on–time is maximum when $V_{control}$ is maximum (1.5 V typically).

At a given Vo, the maximum on–time is then expressed by the following equation:

$$\langle t_{on} \rangle max = \frac{R_o^2 \times I_{ref} \times C_{pin12} \times \langle V_{control} \rangle max}{2 \times V_o^2}$$

This equation can be simplified replacing:

$$\frac{2}{I_{ref} \times \langle V_{control} \rangle max} \qquad \text{by } K_{osc}$$

Refer to **Electrical Characteristics, Oscillator Section**. Then:

$$\langle t_{on} \rangle max = \frac{C_{pin12} \times R_o^2}{K_{osc} \times V_o^2}$$

This equation shows that the maximum on–time is inversely proportional to the squared output voltage. This property is used for follower boost operation (refer to **Follower Boost** section).

Current Sense Block

The inductor current is converted into a voltage by inserting a ground referenced resistor (R_{cs}) in series with the input diodes bridge (and the input filtering capacitor). Therefore a negative voltage proportional to the inductor current is built:

$$V_{cs} = -(R_{cs} \times I_L)$$

where:

I_L is the inductor current,

R_{cs} is the current sense resistor,

V_{cs} is the measured R_{cs} voltage.

The negative signal V_{cs} is applied to the current sense through a resistor R_{OCP}. This pin is internally protected by a negative clamp (–0.7 V) that prevents substrate injection.

As long as the Pin 5 voltage is lower than (–60 mV), the Current Sense comparator resets the PWM latch to force the gate drive signal low state. In that condition, the power MOSFET cannot be on.

During the on–time, the Pin 5 information is used for the overcurrent limitation while it serves the zero current detection during the off time.
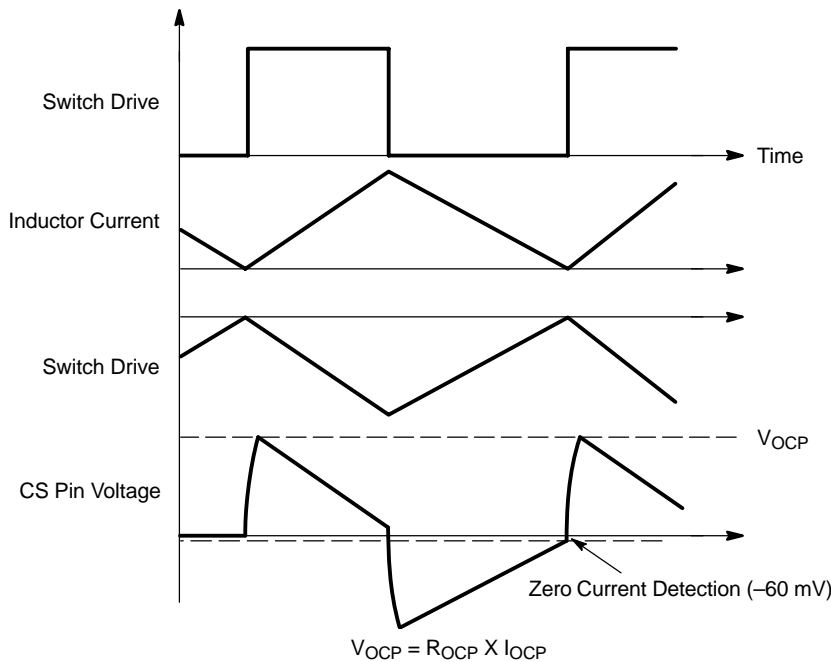
Figure 8. Current Sensing

Zero Current Detection

The Zero Current Detection function guarantees that the MOSFET cannot turn on as long as the inductor current hasn't reached zero (discontinuous mode).

The Pin 5 voltage is simply compared to the (–60 mV) threshold so that as long as V_{cs} is lower than this threshold,

the circuit gate drive signal is kept in low state. Consequently, no power MOSFET turn on is possible until the inductor current is measured as smaller than (60 mV/R_{cs}) that is, the inductor current nearly equals zero.
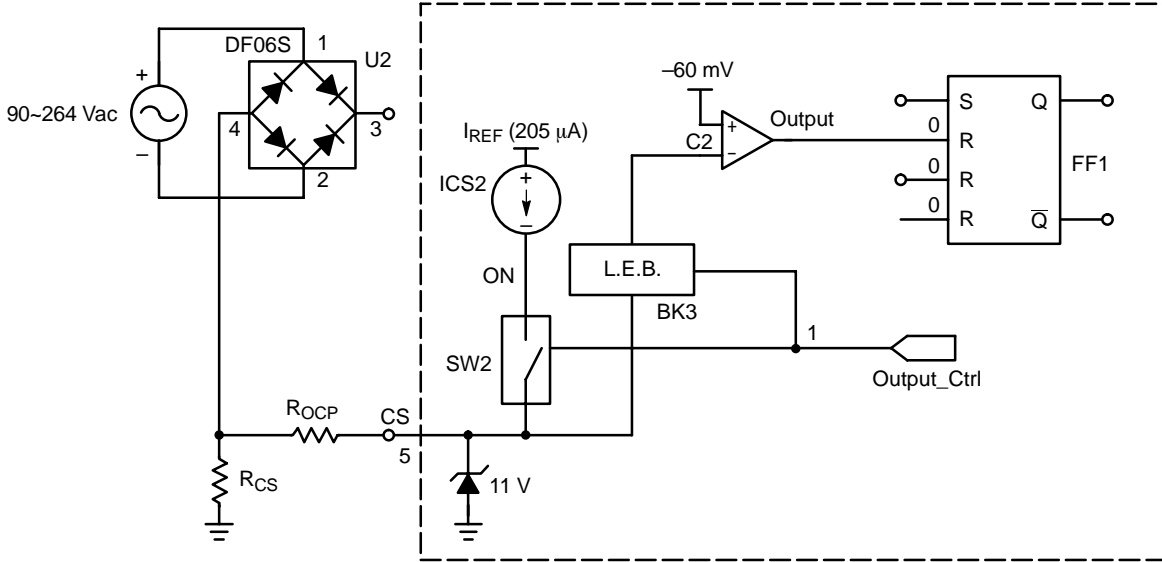
Figure 9. Current Sense Block

OCP (Overcurrent Protection)

During the power switch conduct (i.e. when the Gate Drive pin voltage is high), a current source is applied to the Pin 5. A voltage drop V_{OCP} is then generated across the resistor R_{OCP} that is connected between the sense resistor and the Current Sense pin (refer to Figure 9). So, instead of V_{cs}, the sum($V_{cs} + V_{OCP}$) is compared to (–60 mV) and the maximum permissible current is the solution of the following equation:

$$- (R_{CS} \times I_{pk(max)}) + V_{OCP} = - 60 \, mV$$

where:

$I_{pk(max)}$ is the maximum allowed current,

R_{cs} is the sensing resistor.

The overcurrent threshold is then:

$$I_{pk(max)} = \frac{(R_{OCP} \times I_{OCP}) + (60 \times 10^{-3})}{R_{CS}}$$

where:

R_{OCP} is the resistor connected between the pin and the sensing resistor (R_{cs}),

I_{OCP} is the current supplied by the Current Sense pin when the gate drive signal is high (power switch conduction phase). I_{OCP} equals 205 μA typically.

Practically, the V_{OCP} offset is high compared to 60 mV and the precedent equation can be simplified. The maximum current is then given by the following equation:

$$I_{pk(max)} \approx \frac{R_{OCP\langle k\Omega\rangle}}{R_{CS\langle\Omega\rangle}} \times 0.205\langle A\rangle$$

Consequently, the R_{OCP} resistor can program the OCP level whatever the R_{cs} value is. This gives a high freedom in the choice of R_{cs}. In particular, the inrush resistor can be utilized.

An LEB (Leading Edge Blanking) has been implemented. This circuitry disconnects the Current Sense comparator from Pin 5 and disables it during the first 400 ns of the power switch conduction. This prevents the block from reacting on the current spikes that generally occur at power switch turn on. Consequently, proper operation does not require any filtering capacitor on Pin 5.

OVP (Overvoltage Protection)

Referring to Figure 10, Current Mirror output I_o is relating to PFC output voltage. The current I_o flows into the external resistor and a voltage drop developed across Pin 6. This voltage then is compared with the Overvoltage Protection Threshold, V_{C4}, 3.8 V, when the voltage is higher than the V_{C4}, the OVP comparator, C4 will be enabled and the PFC gate drive disabled as a result to keep the bulk capacitor voltage below the set level. By selecting the value of the external resistor, the OVP voltage can then be determined. With this feature, the maximum bulk capacitor voltage can be set to value below 400 V so that lower cost bulk capacitor can be used.
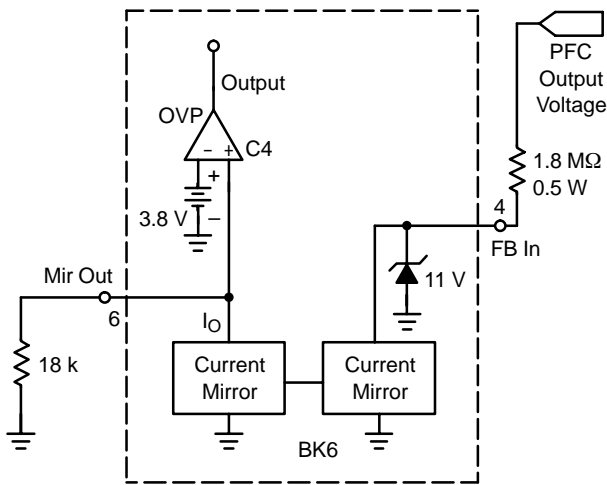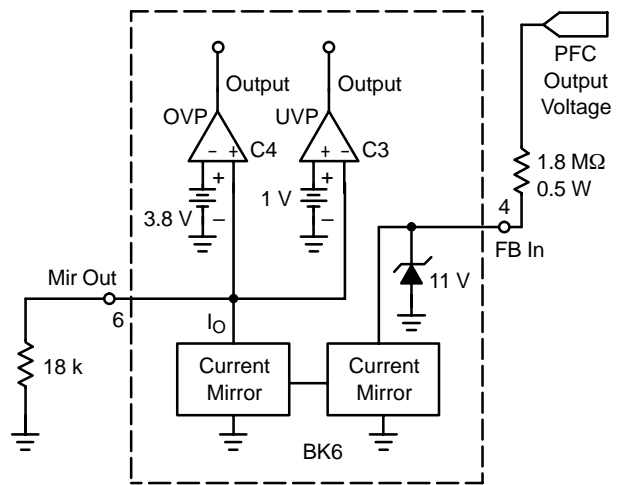
Figure 10. Overvoltage Protection

Figure 11. Undervoltage Detection

Undervoltage Protection and Feedback Loop Open Detection

Refer to Figure 11, similarly, the PFC function will be bypassed until Pin 6 voltage exceed 1.0 V. This feature is used to avoid the PFC drawing high current while the line voltage fall below a reasonable level in order to protect the power elements. This protection feature is also applicable for Feedback Loop Open Detection, i.e. while the feedback resistor is open, no current flowing into the FB_In pin (Pin 4), hence the voltage across Pin 6 will be diminished and the protection will be activated.

Switching Frequency Clamp

Refer to Figure 12, Switching Frequency Clamp. The frequency clamp function can be disabled by pulling the FC pin voltage higher than frequency clamp threshold. While the frequency clamp function is disabled, the PFC gate drive turn–on depends on zero–current–detection of CS pin.

By connecting RC to frequency clamp pin, the PFC gate drive turn–on depend on both FC pin voltage and CS pin's zero–current–detection. When FC pin voltage reach its threshold, PFC gate drive turn–on by zero–current–detection of CS pin.
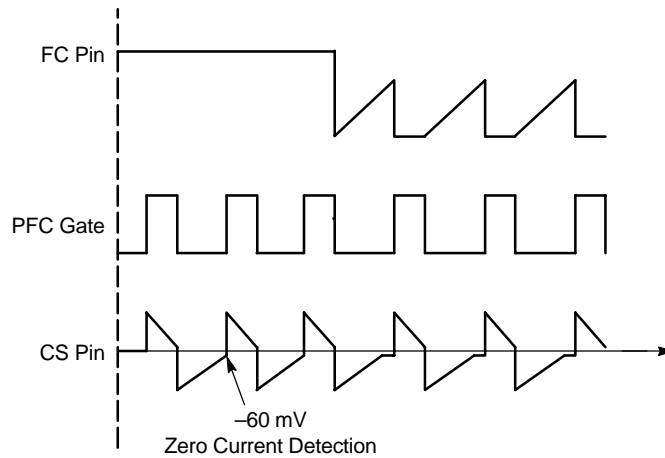
Figure 12. Switch Frequency Clamp

For best results, the minimum off–time, determined by the values of R and C on FC pin, should be chosen so that $t_{s(min)} = t_{on} + t_{off(FC)}$. Output drive is inhibited when the voltage at the frequency clamp input is less than 2.0 V. When the output drive is high, C is discharged through an internal 100 μA current source. When the output drive switches low, C7 is charged through R_{FC}. The drive output is inhibited until the voltage across C_{FC} reaches 2.0 V, establishing a minimum off–time where:

$$t_{off} = -(R_{FC})(C_{FC})\log_e\left[1 - \frac{2}{V_{ref}}\right]$$

Output Section

The output stage contains a totem pole optimized to minimize the cross conduction current during high speed operation. The gate drive is kept in a sinking mode whenever the Undervoltage Lockout is active. The rise and fall times have been controlled to typically equal 50 ns while loaded by 1.0 nF.

Reference Section

An internal reference current source (I_{ref}) is trimmed to be $\pm 2.5\%$ accurate over the temperature range (the typical value is 200 μA). I_{ref} is the reference used for the regulation. An internal reference voltage (V_{ref}) is trimmed to be $\pm 1.53\%$ accurate over the temperature range (the typical value is 6.5 V).

Thermal Shutdown

An internal thermal circuitry is provided to disable the circuit gate drive and then to prevent it from oscillating, if the junction temperature exceeds 150°C typically. The output stage is again enabled when the temperature drops below 120°C typically (30°C hysteresis).

Follower Boost Operation

Traditional PFC pre–converters provide the load with a and regulated voltage that generally equals 230 V or according to the mains type (U.S., European, or universal). In the "Follower Boost" operation, the pre–converter output regulation level is not fixed but varies linearly versus the AC line amplitude at a given input power.
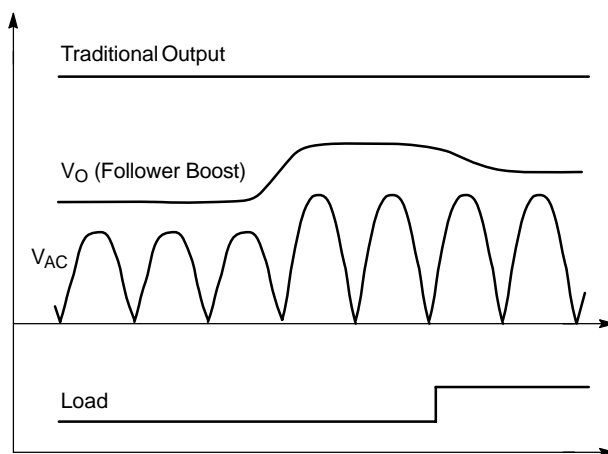
Figure 13. Follower Boost Characteristics

This technique aims at reducing the gap between the output and the input voltages to minimize the boost efficiency degradation.

Follower Boost Benefits

The boost presents two phases:
- The on–time during which the power switch is on.
  The inductor current grows up linearly according to a slope (V_{in}/L_p), where V in is the instantaneous input voltage and L_p the inductor value.
- The off–time during which the power switch is off.
  The inductor current decreases linearly according to the slope (V_o–V_{in})/L_p, where V_o is the output voltage. This sequence that terminates when the current equals zero, has a duration that is inversely proportional to the gap between the output and input voltages.

Consequently, the off–time duration becomes longer in follower boost.

Consequently, for a given peak inductor current, the longer the off time, the smaller power switch duty cycle and then its conduction dissipation. This is the first benefit of this technique: the MOSFET on–time losses are reduced.

The increase of the off time duration also results in a switching frequency diminution (for a given inductor value). Given that in practice, the boost inductor is selected big enough to limit the switching frequency down to an acceptable level, one can immediately see the second benefit of the follower boost: it allows the use of smaller, lighter and cheaper inductors compared to traditional systems. Finally, this technique utilization brings a drastic system cost reduction by lowering the cost of both the inductor and the power switch.
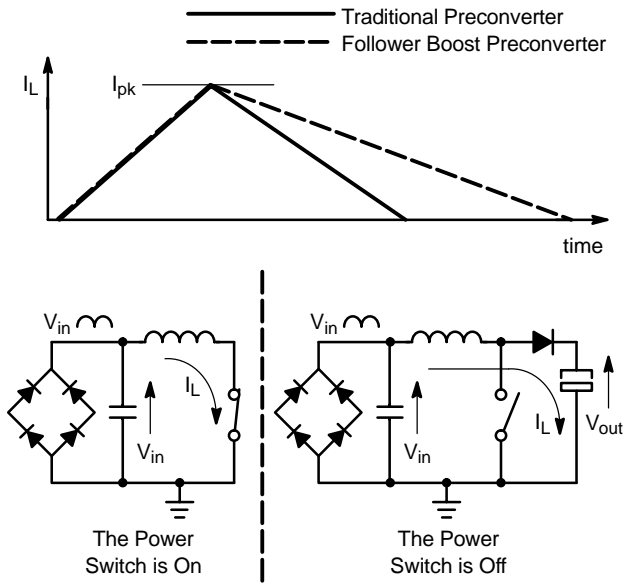
Figure 14. Off–Time Duration Increase

Follower Boost Implementation

In the NCP1600, the on–time is controlled differently according to the feedback current level. Two areas can be defined:

- When the feedback current is higher than I_{regL} (refer to regulation section), the regulation block output ($V_{control}$) is modulated to force the output voltage to a desired value.

- On the other hand, when the feedback current is lower than I_{regL}, the regulation block output and therefore, the on–time are maximum. As explained in **PWM Latch Section,** the on–time is then inversely proportional to the output voltage square. The Follower Boost is active in these conditions in which the on–time is simply limited by the output voltage level. Note: In this equation, the feedback pin voltage (V_{pin1}) is neglected compared to the output voltage (refer to the **PWM Latch Section**).

$$t_{on} = \langle t_{on}\rangle\, \text{max} = \frac{C_{pin12} \times R_o{}^2}{K_{osc} \times V_o{}^2}$$

where:

C_{pin12} is the total oscillator capacitor (sum of the internal and external capacitors – $C_{int} + C_T$),

K_{osc} is the ratio (oscillator swing over oscillator gain),

V_o is the output voltage,

R_o is the feedback resistor.

On the other hand, the boost topology has its own rule that dictates the on–time necessary to deliver the required power:

$$t_{on} = \frac{4 \times L_p \times P_{in}}{V_{pk}{}^2}$$

where:

V_{pk} is the peak AC line voltage,

L_p is the inductor value,

P_{in} is the input power.

Combining the two equations, one can obtain the Follower Boost equation:

$$V_o = \left(\frac{R_o}{2}\right)\sqrt{\frac{C_{pin12}}{K_{osc} \times L_p \times P_{in}}} \times V_{pk}$$

Consequently, a linear dependency links the output voltage to the AC line amplitude at a given input power.
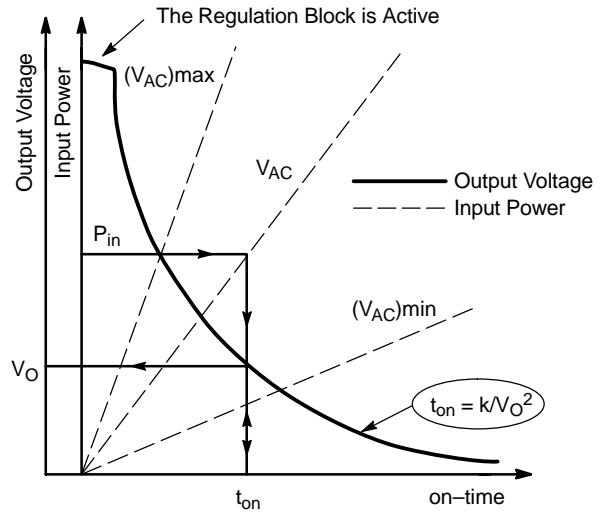
Figure 15. Follower Boost Characteristics

The behavior of the output voltage is depicted in Figures 15 and 16. In particular, Figure 15 illustrates how the output voltage converges to a stable equilibrium level. First, at a given AC line voltage, the on–time is dictated by the power demand. Then, the follower boost characteristic makes correspond one output voltage level to this on–time.

Combining these two laws, it appears that the power level forces the output voltage.

One can notice that the system is fully stable:

- If an output voltage increase makes it move away from its equilibrium value, the on–time will immediately diminish according to the follower boost law. This will result in a delivered power decrease. Consequently, the supplied power being too low, the output voltage will decrease back.

- In the same way, if the output voltage decreases, more power will be transferred and then the output voltage will increase back.
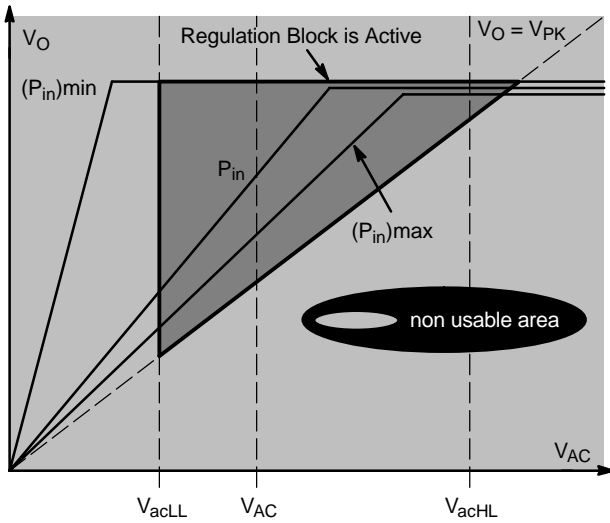
Figure 16. Follower Boost Output Voltage

Mode Selection

The operation mode is simply selected by adjusting the oscillator capacitor value. As shown in Figure 16, the output voltage first has an increasing linear characteristic versus the AC line magnitude and then is clamped down to the regulation value. In the traditional mode, the linear area must be rejected. This is achieved by dimensioning the oscillator capacitor so that the boost can deliver the maximum power while the output voltage equals its regulation level and this, whatever the given input voltage.

Practically, that means that whatever the power and input voltage conditions are, the follower boost would generate output voltages values higher than the regulation level, if there was no regulation block.

In other words, if $\langle Vo \rangle_{regL}$ is the low output regulation level:

$$\langle V_O \rangle regL \leq \frac{R_O}{2} \times \sqrt{\frac{C_T + C_{int}}{K_{osc} \times L_p \times \langle P_{in} \rangle max}} \, V_{pk}$$

Consequently,

$$C_T \geq - C_{int} + \frac{4 \times K_{osc} \times L_p \times \langle P_{in} \rangle max \times \langle V_O \rangle regL^2}{R_O^2 \times V_{pk}^2}$$

Using I_{regL} (regulation block current reference), this equation can be simplified as follows:

$$C_T \geq - C_{int} + \frac{4 \times K_{osc} \times L_p \times \langle P_{in} \rangle max \times I_{regL}^2}{V_{pk}^2}$$

In the Follower Boost case, the oscillator capacitor must be chosen so that the wished characteristics are obtained.

Consequently, the simple choice of the oscillator capacitor enables the mode selection.

Standby Operation

PFC boost pre–converter entering standby mode depends on the STB (Standby) pin voltage (Pin 8 voltage) which is high impedance input and can be directly connected to PWM section's Opto–coupler output to derive PWM output load information. PFC boost pre–converter will enter Standby mode when the voltage at this pin falls below 0.5 V.

While the output of C7 is low, the PFC will stay in normal operation and the AND1 gate output will keep low for all the time. When the STB pin voltage falls below the threshold, 0.5 V, the output of C7 will go high and the output of AND1 gate will depends on the output of C6. The current flowing from the current mirror on Pin 4 is equal to FB–In pin (Pin 4) current which derives from Bulk Capacitor voltage at the output. PFC pre–converter will be disabled when the voltage at Pin 6 is higher than the voltage at Pin 7. The minimum PFC output voltage can be set by Pin 7 voltage during standby mode. This voltage can be derived from the V_{ref} (Pin 2) by a potential divider network.

During standby operation, the PFC boost pre–converter will enter skip mode when AC input voltage falls below this pre–set value, the minimum PFC output voltage and PFC boost pre–converter will enter off mode when AC input voltage higher than the pre–set minimum PFC output voltage.

PACKAGE DIMENSIONS

SO–16
D SUFFIX
CASE 751B–05
ISSUE J
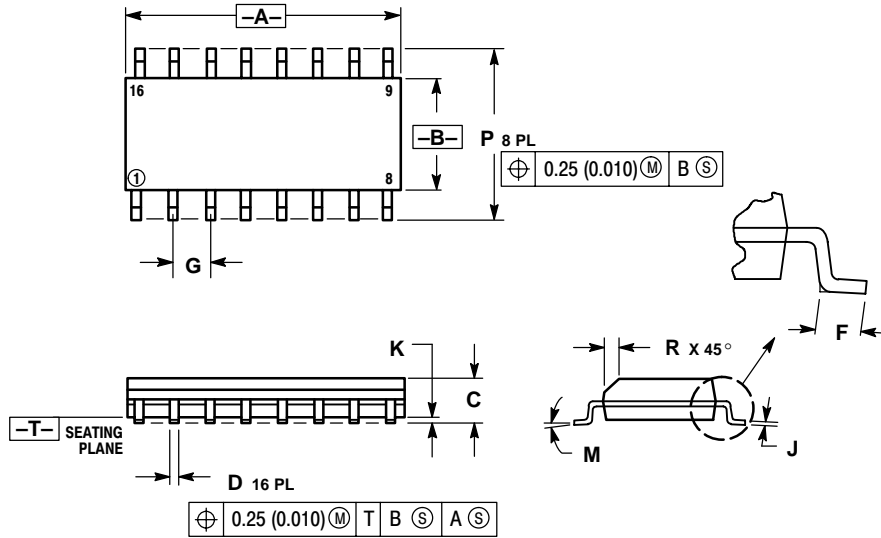
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

$\oplus$ 0.25 (0.010) Ⓜ B Ⓢ

$\oplus$ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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