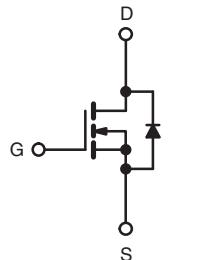
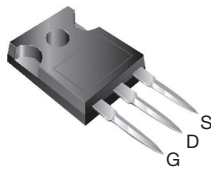


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.60
Q_g (Max.) (nC)	140
Q_{gs} (nC)	20
Q_{gd} (nC)	69
Configuration	Single

TO-247AC


N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC


RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFPC50PbF
	SiHFPC50-E3
SnPb	IRFPC50
	SiHFPC50



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	600	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current	V_{GS} at 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	11	A
			$T_C = 100\text{ }^\circ\text{C}$	7.0	
Pulsed Drain Current ^a		I_{DM}	44		
Linear Derating Factor			1.4	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy ^b		E_{AS}	920	mJ	
Repetitive Avalanche Current ^a		I_{AR}	10	A	
Repetitive Avalanche Energy ^a		E_{AR}	18	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	180	W	
Peak Diode Recovery dV/dt^c		dV/dt	3.0	V/ns	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 13\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 11\text{ A}$ (see fig. 12).
- $I_{SD} \leq 11\text{ A}$, $dI/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

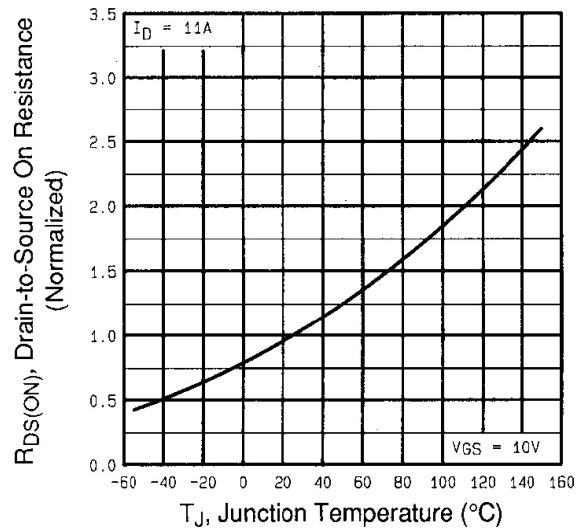
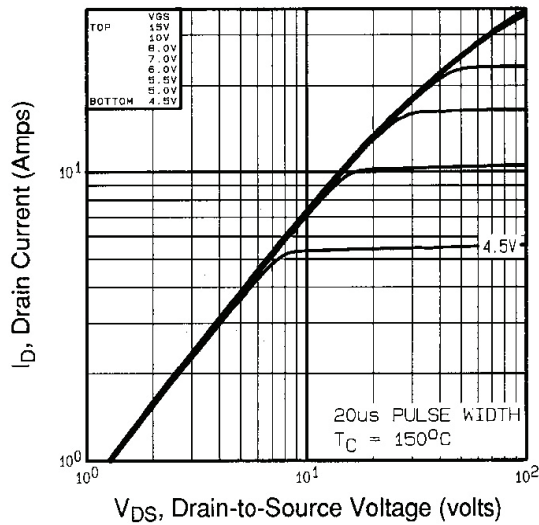
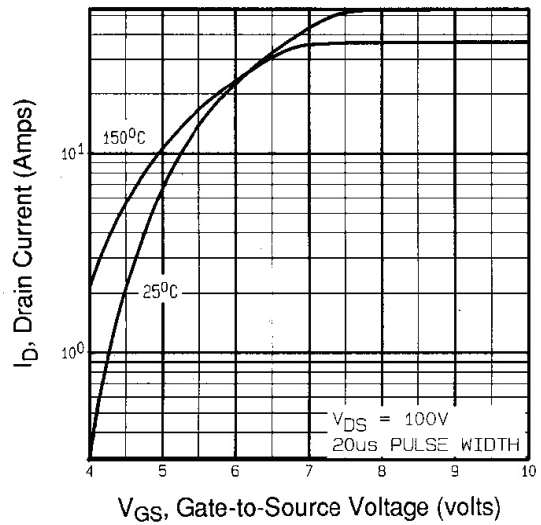
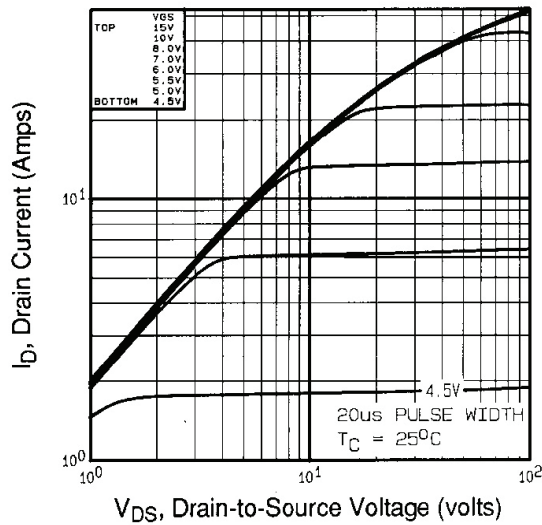
THERMAL RESISTANCE						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	-	40	°C/W	
Case-to-Sink, Flat, Greased Surface	R_{thCS}	-	0.24	-		
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	0.65		

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.78	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 6.0\text{ A}^b$	-	-	0.60	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 100\text{ V}, I_D = 6.0\text{ A}^b$		5.7	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	2700	-	pF
Output Capacitance	C_{oss}			-	300	-	
Reverse Transfer Capacitance	C_{rss}			-	61	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}, V_{DS} = 360\text{ V}$ see fig. 6 and 13 ^b	-	-	140	nC
Gate-Source Charge	Q_{gs}			-	-	20	
Gate-Drain Charge	Q_{gd}			-	-	69	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 11\text{ A}, R_g = 6.2\text{ }\Omega, R_D = 30\text{ }\Omega$, see fig. 10 ^b		-	18	-	ns
Rise Time	t_r			-	37	-	
Turn-Off Delay Time	$t_{d(off)}$			-	88	-	
Fall Time	t_f			-	36	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L_S			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	11	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	44	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 11\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 11\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	550	830	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.9	5.9	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



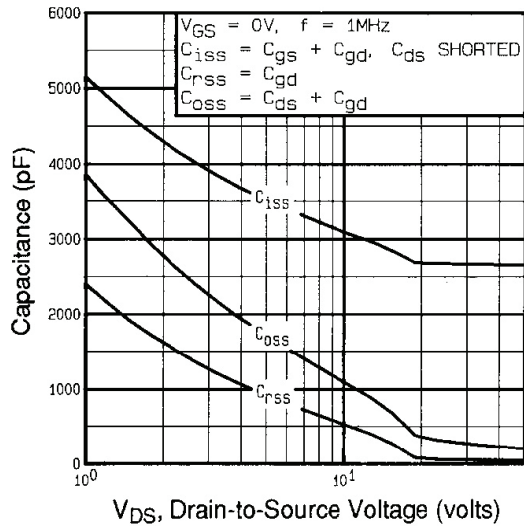


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

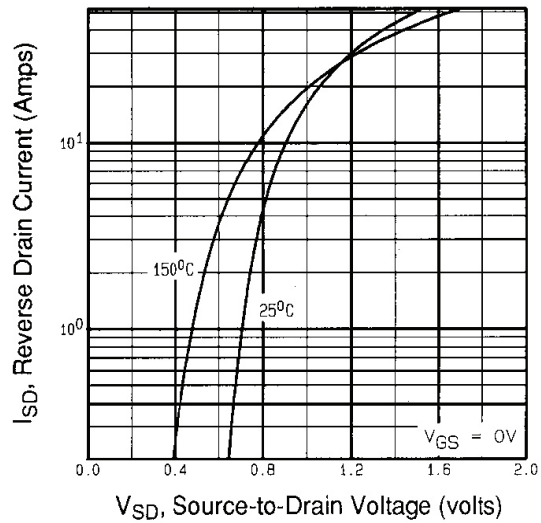


Fig. 7 - Typical Source-Drain Diode Forward Voltage

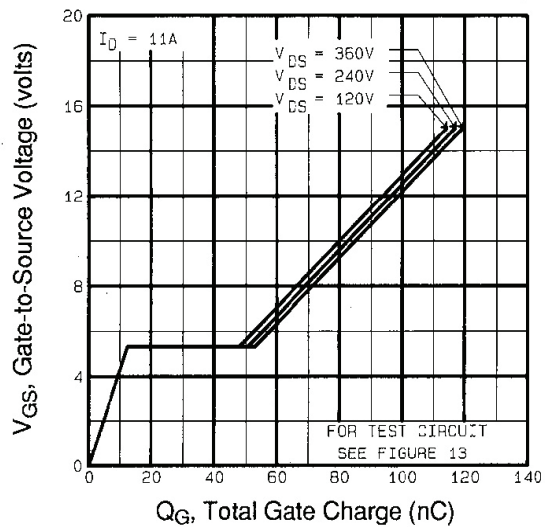


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

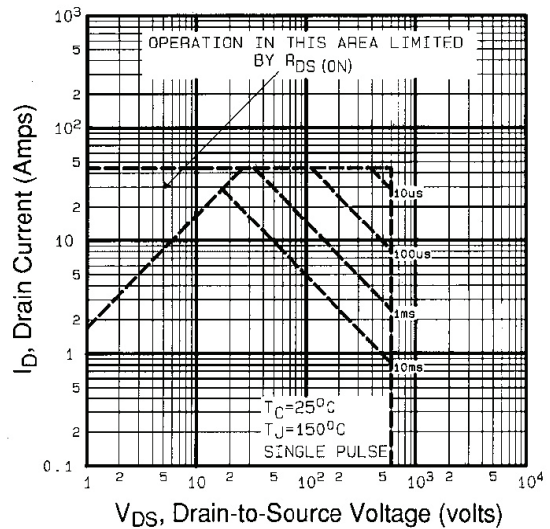


Fig. 8 - Maximum Safe Operating Area

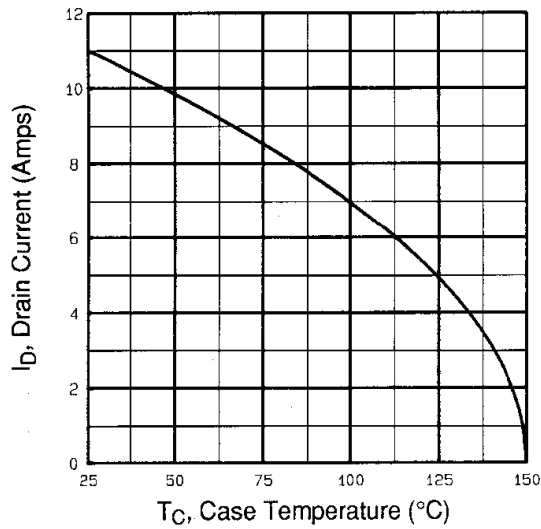


Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

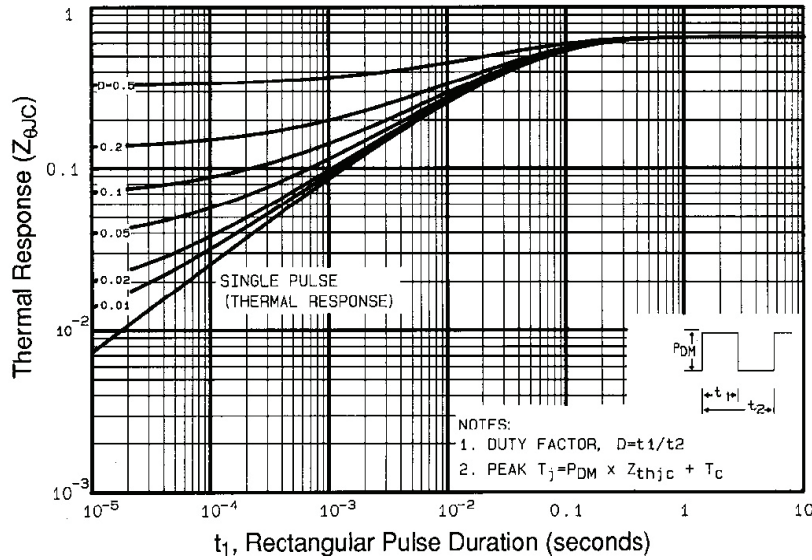


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

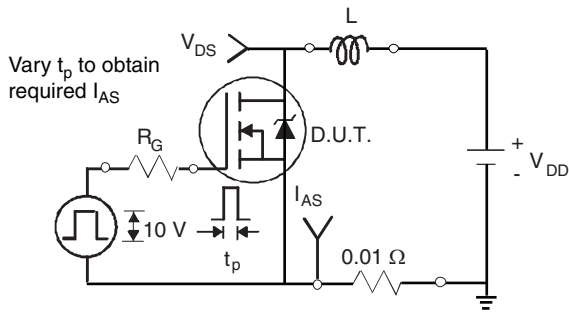


Fig. 12a - Unclamped Inductive Test Circuit

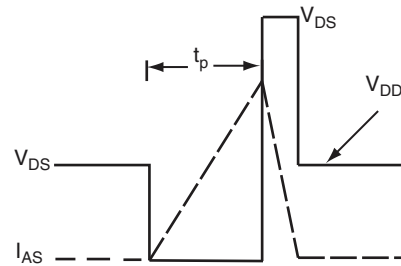


Fig. 12b - Unclamped Inductive Waveforms

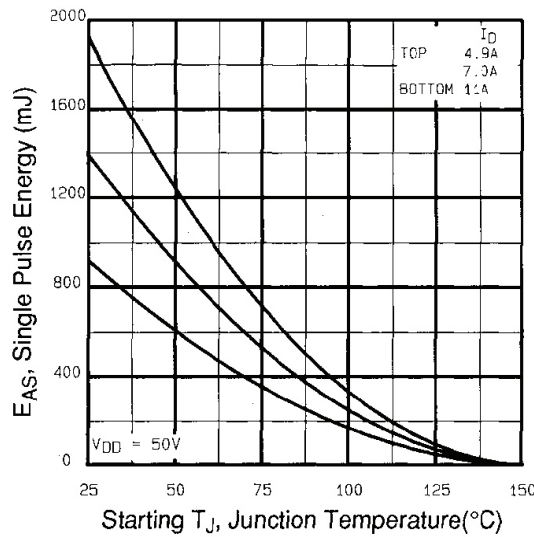


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

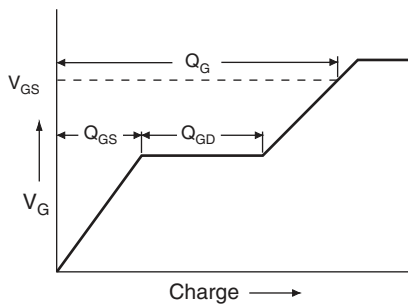


Fig. 13a - Basic Gate Charge Waveform

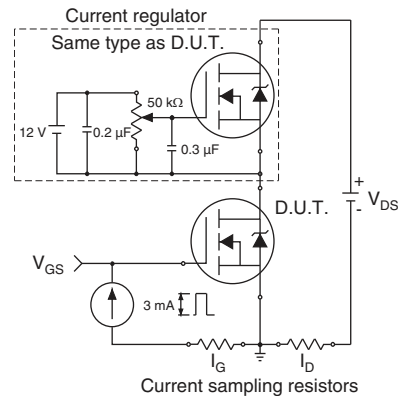
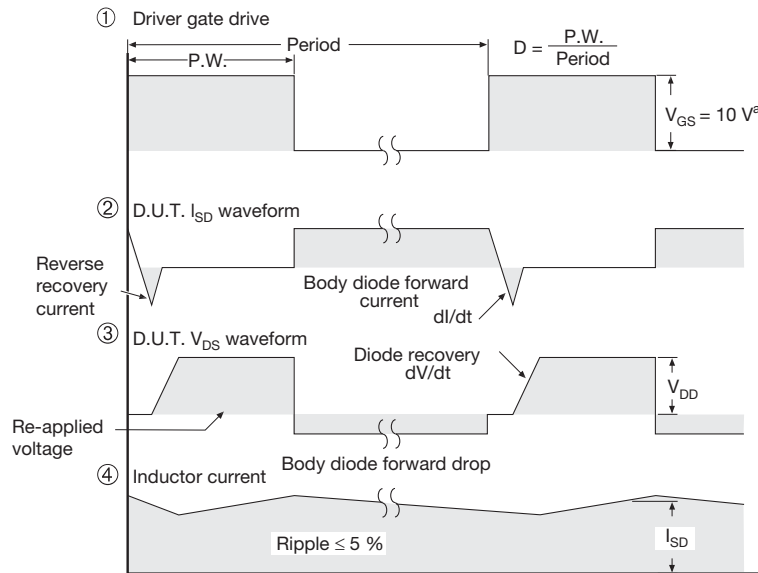
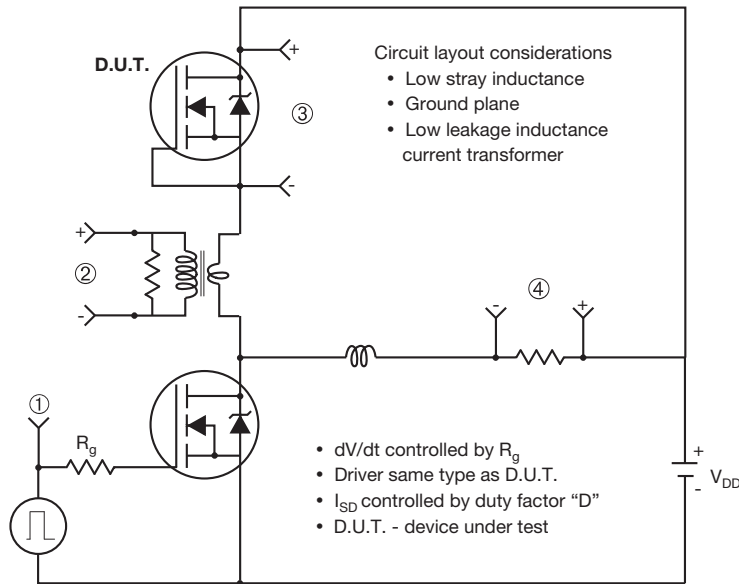


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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