



# STW80NF55-08

N-CHANNEL 55V - 0.0065Ω - 80A TO-247

STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STW80NF55-08	55 V	< 0.008 Ω	80 A

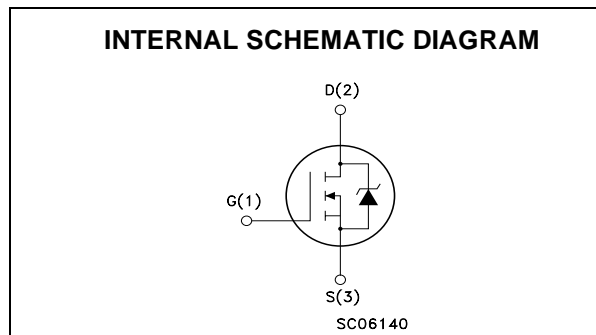
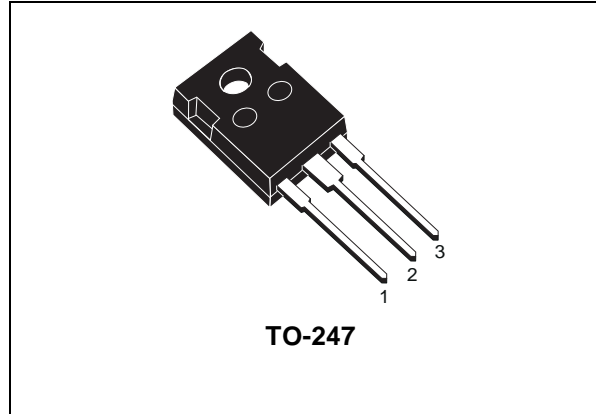
- TYPICAL R<sub>DS(on)</sub> = 0.0065Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW THRESHOLD DRIVE

### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- DC-AC & DC-DC CONVERTERS
- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	55	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	55	V
V <sub>GS</sub>	Gate- source Voltage	±20	V
I <sub>D</sub> (*)	Drain Current (continuous) at T <sub>C</sub> = 25°C	80	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	80	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	320	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	300	W
	Derating Factor	2	W/°C
E <sub>AS</sub> (1)	Single Pulse Avalanche Energy	870	mJ
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) Starting T<sub>j</sub> = 25°C, I<sub>D</sub> = 40A, V<sub>DD</sub> = 40V

(\*) Current Limited by wire bonding

## STW80NF55-08

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	55			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 40 A		0.0065	0.008	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > 2.5 V, I <sub>D</sub> = 18 A		20		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		3850		pF
C <sub>oss</sub>	Output Capacitance			800		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			250		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 27V, I_D = 40A$		25		ns
$t_r$	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		85		ns
$Q_g$	Total Gate Charge	$V_{DD} = 80V, I_D = 80A,$		115	150	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 10V$		24		nC
$Q_{gd}$	Gate-Drain Charge			46		nC

**SWITCHING OFF**

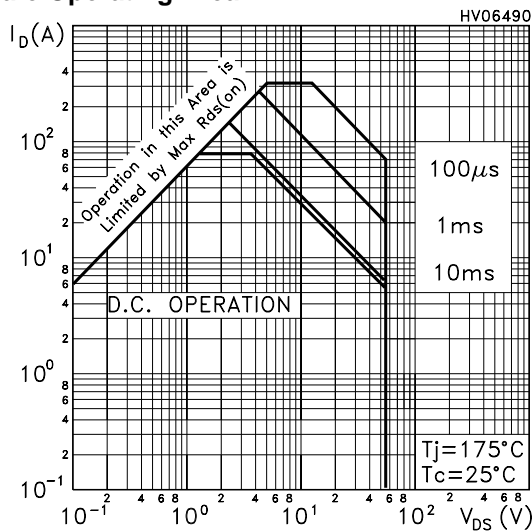
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 27V, I_D = 40A,$		70		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		25		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 44V, I_D = 80A$		85		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$		75		ns
$t_c$	Cross-over Time	(see test circuit, Figure 5)		110		ns

**SOURCE DRAIN DIODE**

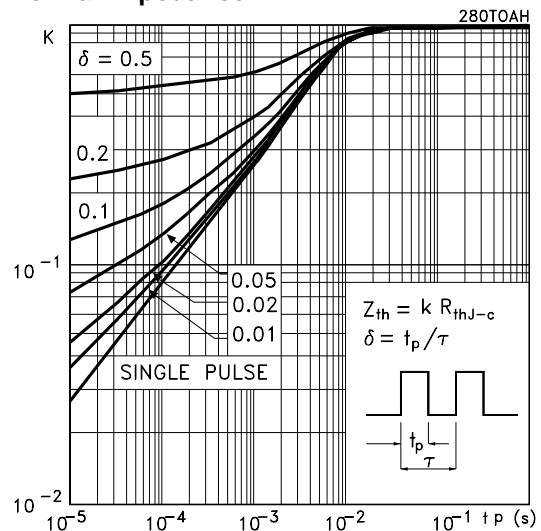
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				80	A
$I_{SDM(1)}$	Source-drain Current (pulsed)				320	A
$V_{SD(2)}$	Forward On Voltage	$I_{SD} = 80A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 80A, di/dt = 100A/\mu s,$		80		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 50V, T_j = 150^\circ C$		250		nC
$I_{RRM}$	Reverse Recovery Current	(see test circuit, Figure 5)		6.4		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
 2. Pulse width limited by safe operating area.

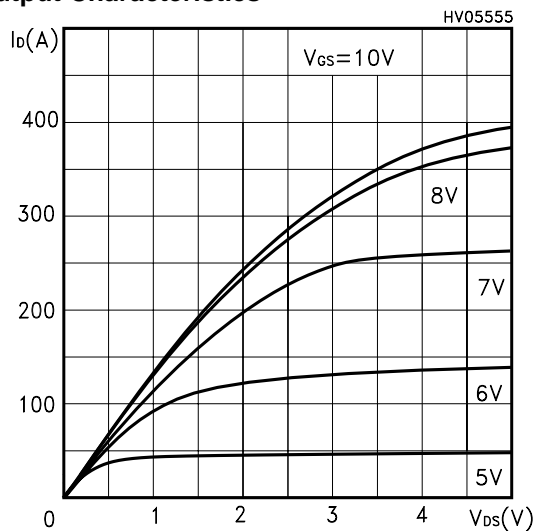
**Safe Operating Area**



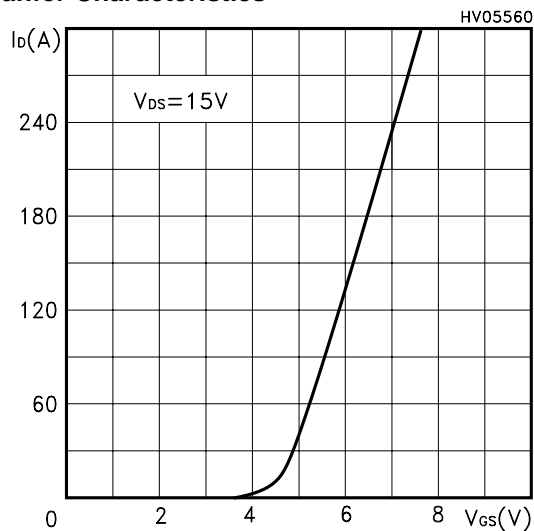
**Thermal Impedance**



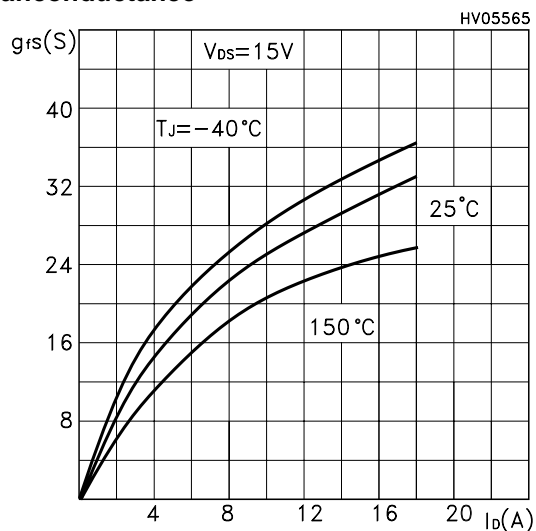
Output Characteristics



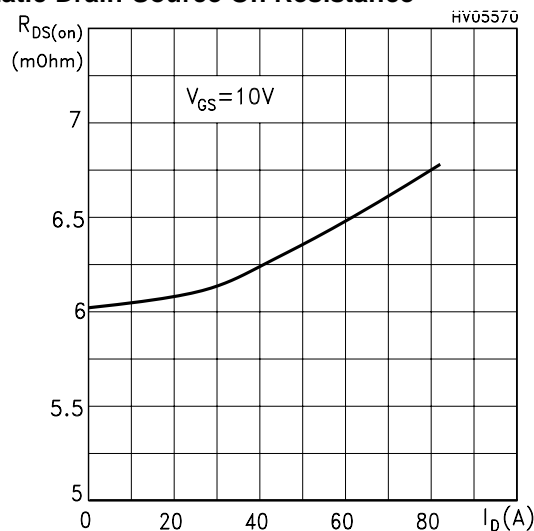
Transfer Characteristics



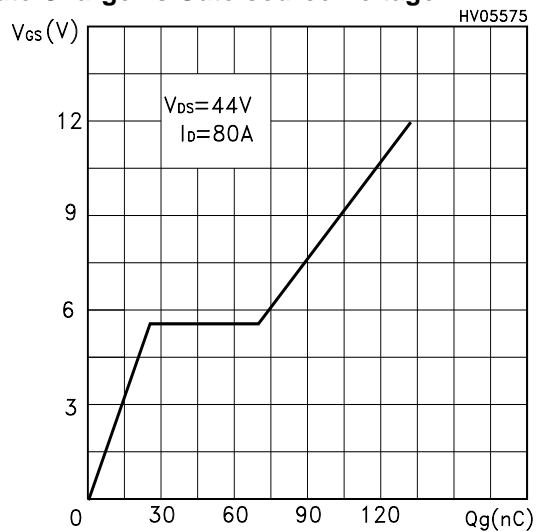
Transconductance



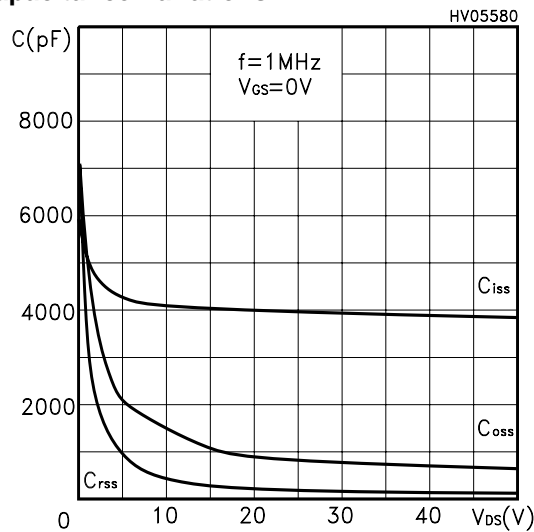
Static Drain-Source On Resistance



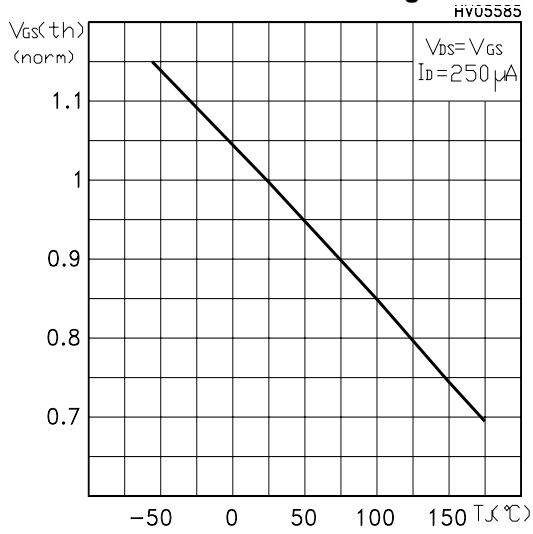
Gate Charge vs Gate-source Voltage



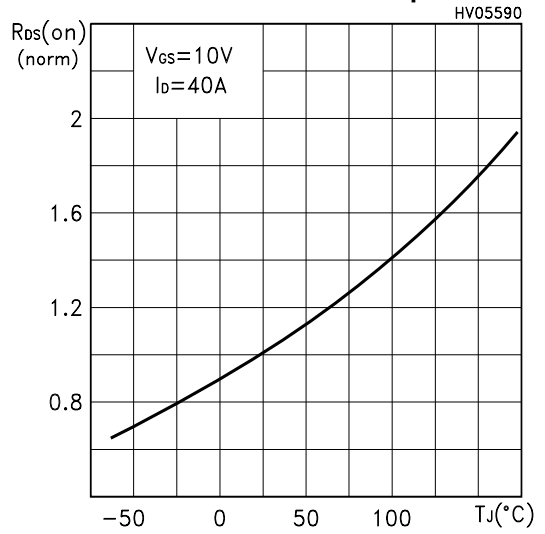
Capacitance Variations



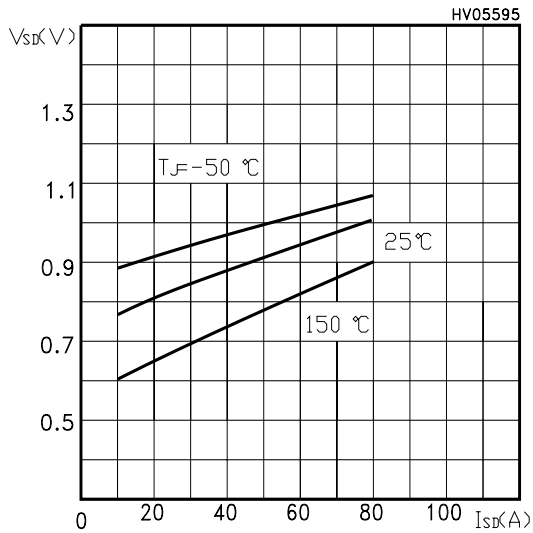
**Normalized Gate Threshold Voltage vs Temp.**



**Normalized On Resistance vs Temperature**



**Source-drain Diode Forward Characteristics**



**Normalized Breakdown Voltage vs Temperature**

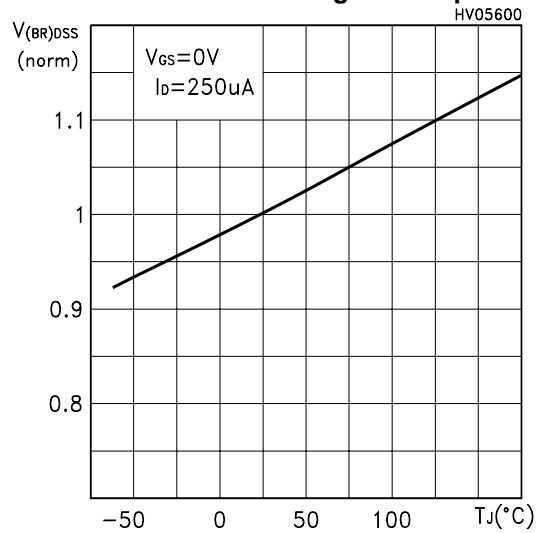


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuit For Resistive Load

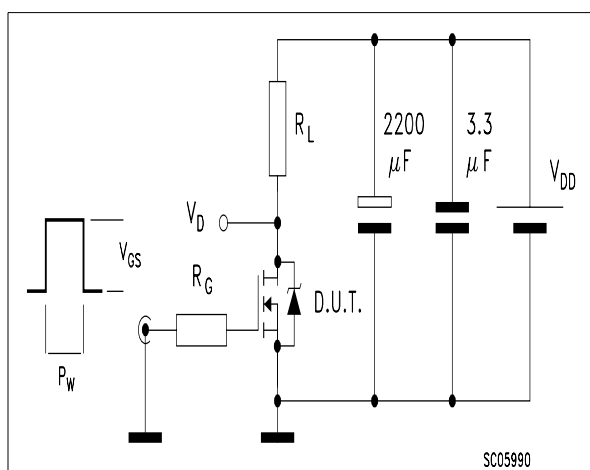


Fig. 4: Gate Charge test Circuit

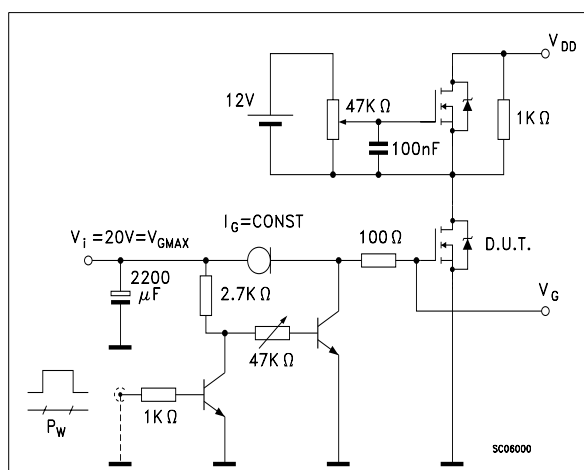
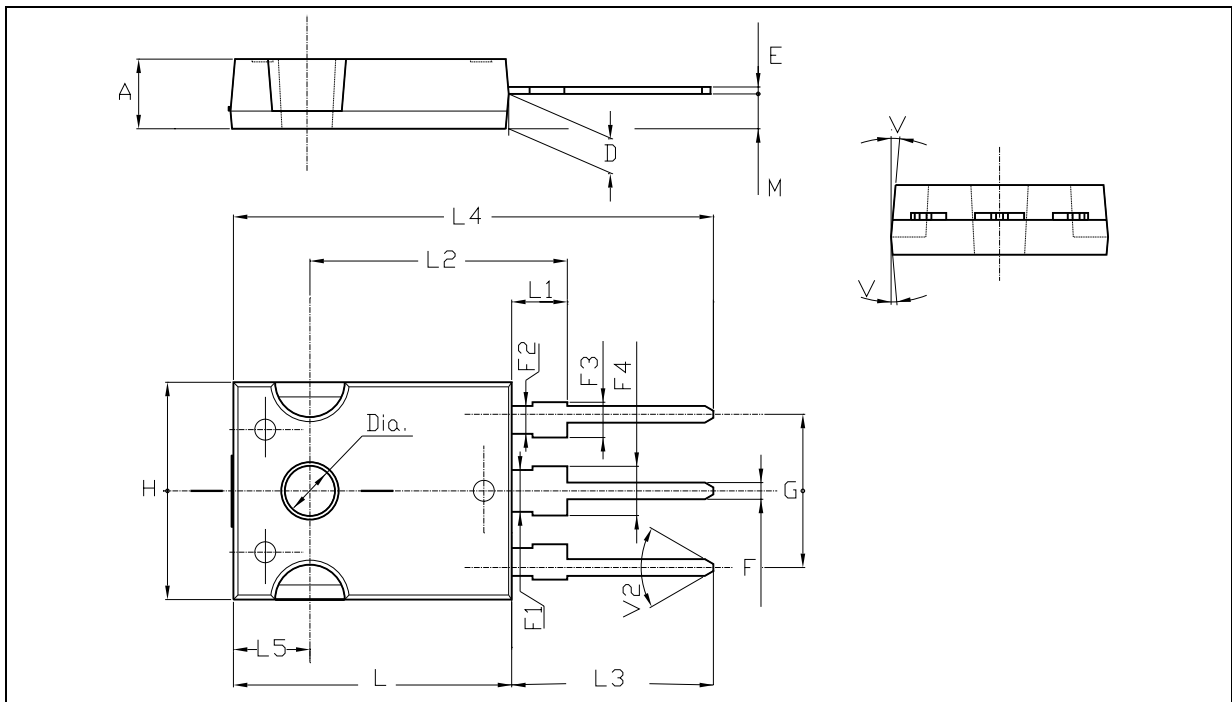


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
E	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
H	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
M	2		3	0.07		0.11
V		5°			5°	
V2		60°			60°	
Dia	3.55		3.65	0.14		0.143



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