



### General Description

The Topro TP2808 is an 8-bit microcontroller, which has an in-system programmable FLASH EPROM for firmware updating and fully compatible instruction set with the standard 8051. It contains a 128K-byte FLASH EPROM, 1K bytes of on-chip RAM, four 8-bit bi-directional and bit-addressable I/O ports, an additional 4-bit port P4, three 16-bit timer/counters, a serial port, 7-channel PWM and 4-channel 6-bit ADC, and is available in 44-pin PLCC, 44-pin QFP, 40-pin DIP package forms.

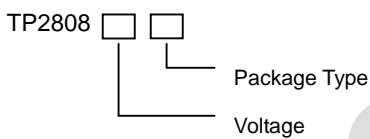
### Applications

- LCD TV
- LCD Monitor
- Flat Panel Display

### Features

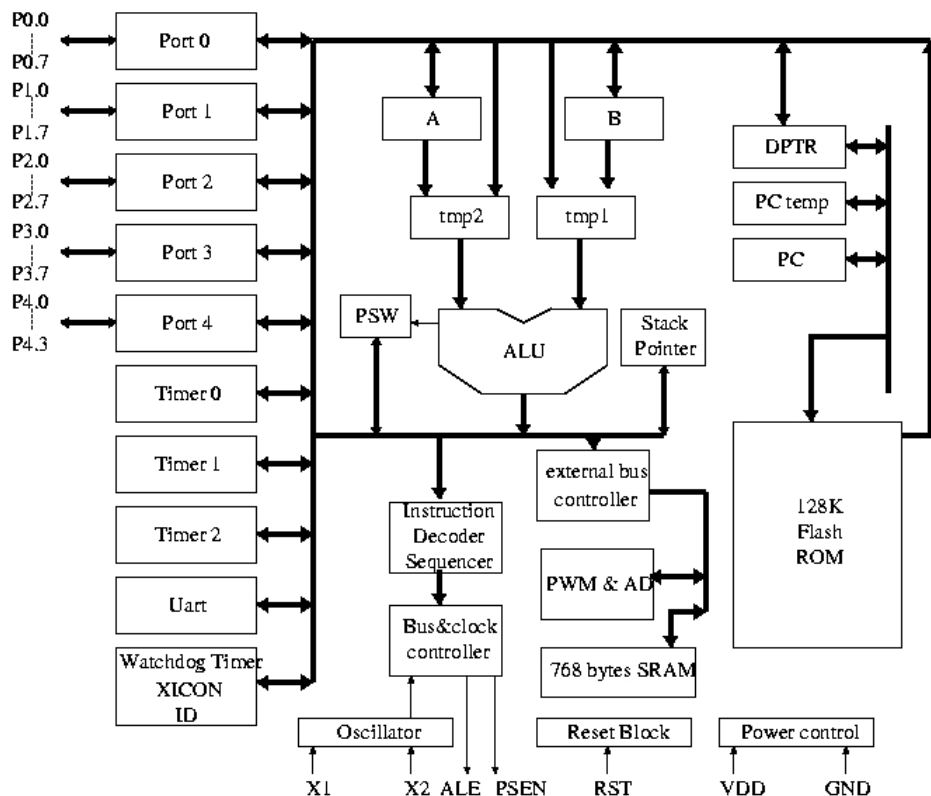
- Fully static design of 8-bit CMOS microcontroller up to 40 MHz
- 128K-byte FLASH EPROM
- Low standby current at full supply voltage
- 1K bytes of on-chip RAM (including 768 bytes of AUX-RAM, software selectable)
- Four 8-bit bi-directional ports
- One 4-bit multipurpose programmable port
- Three 16-bit timer/counters
- One full duplex serial port
- 7-channel PWM DAC
- 4-channel 6-bit ADC
- Built-in power management for low stand-by consumption
- Code protection
- Compliant with VESA DDC1/DDC2B/DDC2Bi
- Package Forms: 44-pin PLCC, 44-pin QFP, 40-pin DIP

### Ordering Information



<b>Voltage</b>	L: 3.3V H: 5V
<b>Package Type</b>	P: DIP C: PLCC Q: PQFP

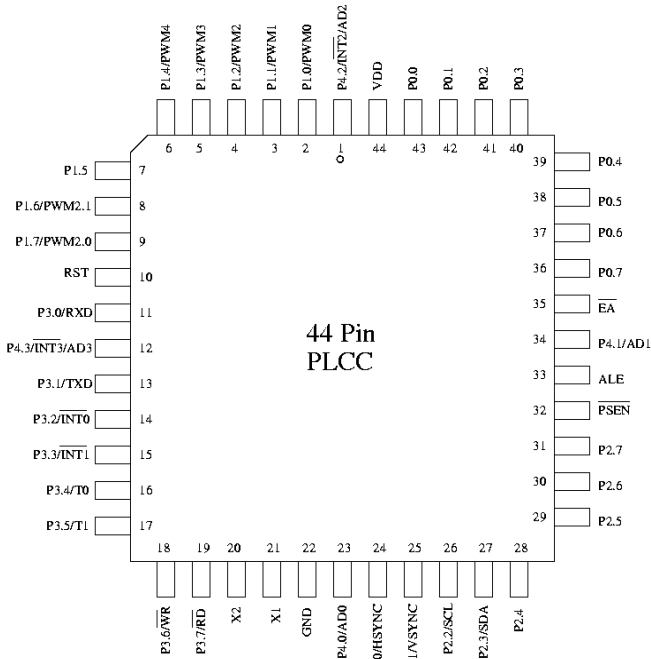
### Block Diagram



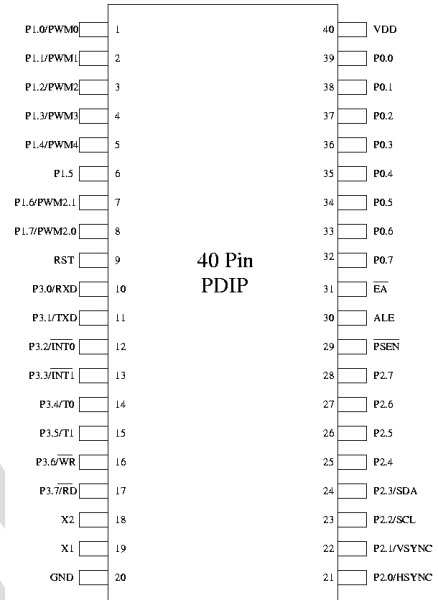


Pin Configurations

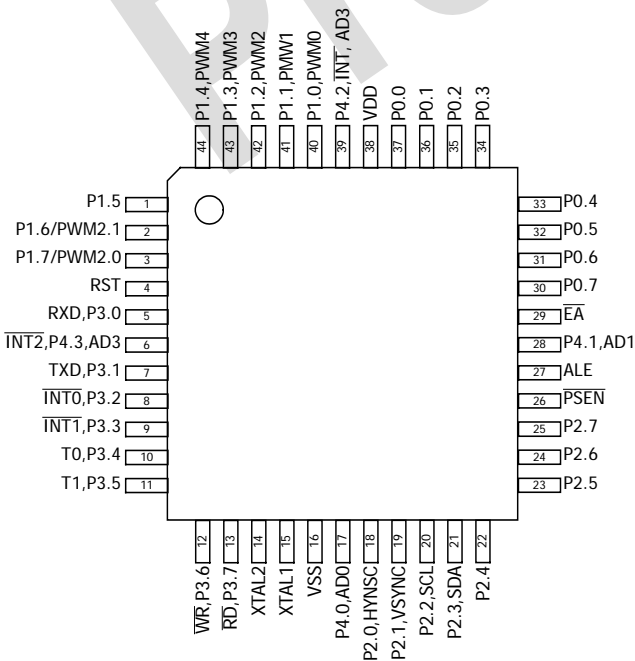
44-pin PLCC



40-pin DIP



44-pin PQFP



Pin Descriptions

Symbol	Type	Description
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high and the program counter is within the 64KB area.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESSLATCH ENABLE ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6 <sup>th</sup> of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
RST	I L	RESET A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input pin and may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output pin and is the inversion of XTAL1.
V <sub>SS</sub>	I	GROUND: ground potential
V <sub>DD</sub>	I	POWER SUPPLY: Supply voltage for operation
P0.0 - P0.7	I/O D	PORT 0: Function is the same as that of standard 8051.
P1.0/PWM0	I/O	General purpose I/O (8051 standard) / PWMDAC0 output (CMOS)
P1.1/PWM1	I/O	General purpose I/O (8051 standard) / PWMDAC1 output (CMOS)
P1.2/PWM2	I/O	General purpose I/O (8051 standard) / PWMDAC2 output (CMOS)
P1.3/PWM3	I/O	General purpose I/O (8051 standard) / PWMDAC3 output (CMOS)
P1.4/PWM4	I/O	General purpose I/O (8051 standard) / PWMDAC4 output (CMOS)
P1.5	I/O	General purpose I/O (8051 standard)
P1.6/PWM2.1	I/O	General purpose I/O (8051 standard) / PWM2.1DAC output (CMOS)
P1.7/PWM2.0	I/O	General purpose I/O (8051 standard) / PWM2.0DAC output (CMOS)
P2.0 - P2.7	I/O	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. P2.0 is also used for HSYNC input. P2.1 is also used for VSYNC input. P2.2 is also used for SCL P2.3 is also used for SDA
P3.0 - P3.7	I/O	PORT 3: Function is the same as that of the standard 8051. P3.5 is used to select the bank of 128K flash ROM
P4.0/AD0	I/O	General purpose I/O (8051 standard) / ADC input
P4.1/AD1	I/O	General purpose I/O (8051 standard) / ADC input
P4.2/INT2/AD2	I/O	General purpose I/O (8051 standard) / external interrupt input / ADC input
P4.3/INT3/AD3	I/O	General purpose I/O (8051 standard) / external interrupt input / ADC input



### Functional Description

The TP2808 architecture consists of a core controller surrounded by various registers, four general-purpose I/O ports, 1K bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both with a 64K program address space and a 64K data storage space.

#### RAM

The internal data RAM in the TP2808 is 1032 bytes and is divided into two banks: 256 bytes of scratchpad RAM and 768 bytes of AUX-RAM, both addressed by different ways.

##### 1. RAM 0H-7FH

It can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.

##### 2. RAM 80H-FFH

It can only be addressed indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected registers bank.

##### 3. AUX-RAM 0H-302H

It is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointers are R0 of the selected register bank and DPTR register. An access to external data memory locations higher than FFH will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is disabled after a reset. Setting the bit 4 in CHPCON register will enable the access to on-chip AUX-RAM. When executing from internal program memory, an access to AUX-RAM will not affect the ports P0, P2,  $\overline{WR}$  and  $\overline{RD}$ .

#### Timers 0, 1 and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for Timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate either as an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: Capture, Auto-reload, and Baud Rate Generator. The clock speed at Capture or Auto-reload mode is the same as that of Timers 0 and 1.

#### $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts,  $\overline{INT2}$  and  $\overline{INT3}$ , whose functions are similar to those of external interrupt 0 and 1 in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 8051. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ( $\overline{INT3}$ ) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

#### XICON-External Interrupt Control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2
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PX3: External interrupt 3 priority high if set.

EX3: External interrupt 3 enable if set.

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software.

PX2: External interrupt 2 priority high if set.

EX2: External interrupt 2 enable if set.

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software.



**9-source Interrupt Information**

Interrupt Source	Vector Address	Polling Sequence Within Priority Level	Enable Required Settings	Interrupt Type Edge/Level
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
External Interrupt 2	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 3	33H	6	XICON.2	XICON.0
Timer/Counter 3	3BH	7	XICON.6	XICON.3
DDC2	43h	8 (Lowest)	See DDC	IP

**Pad Function Control**

Please refer to the part of Pin Configurations for the each function.

Reg. Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>PADOPT</b>	0f50h(w)	-	-	-	-	AD3E	AD2E	AD1E	AD0E
<b>PADOPT</b>	0f51h(w)	PWMf	PWMd	-	PWM4	PWM3	PWM2	PWM1	PWM0

**PADOPT (w):** control registers in a pad mode,

all-standing for "0" in chip Reset.

AD3E = 1 -> Pin "P4.3/AD3" for AD3  
 = 0 -> Pin "P4.3/AD3" for P4.3

AD2E = 1 -> Pin "P4.2/AD2" for AD2  
 = 0 -> Pin "P4.2/AD2" for P4.2

AD1E = 1 -> Pin "P4.1/AD1" for AD1  
 = 0 -> Pin "P4.1/AD1" for P4.1

AD0E = 1 -> Pin "P4.0/AD0" for AD0  
 = 0 -> Pin "P4.0/AD0" for P4.0

PWMf = 1 -> Selection of 94KHz PWM frequency  
 = 0 -> Selection of 47KHz PWM frequency

PWMd = 1 -> PWM pulse width for 253-step

resolution

= 0 -> PWM pulse width for 256-step resolution

PWM4 = 1 -> Pin "P1.4/PWM4" for PWM4

= 0 -> Pin "P1.4/PWM4" for P1.4

PWM3 = 1 -> Pin "P1.3/PWM3" for PWM3

= 0 -> Pin "P1.3/PWM3" for P1.3

PWM2 = 1 -> Pin "P1.2/PWM2" for PWM2

= 0 -> Pin "P1.2/PWM2" for P1.2

PWM1 = 1 -> Pin "P1.1/PWM1" for PWM1

= 0 -> Pin "P1.1/PWM1" for P1.1

PWM0 = 1 -> Pin "P1.0/PWM0" for PWM0

= 0 -> Pin "P1.0/PWM0" for P1.0

**PWM DAC I**

Each 8-bit PWMDA register in XFR controls each output pulse width of PWM DAC converter. PWMf selects the frequency of PWM clocks as 47KHz or 94KHz (for X'tal frequency = 12MHz), and PWMd selects the total duty cycle step of these DAC outputs as 253 or 256. In case of PWMd = 1, writing FDH/FEH/FFH to DAC register masks output stably high and writing 00H to DAC register makes the output stably low.

Reg. Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>PWMDA</b>	0f20H(r/w)	Pulse width of PWM DAC 0							
<b>PWMDA</b>	0f21H(r/w)	Pulse width of PWM DAC 1							
<b>PWMDA</b>	0f22H(r/w)	Pulse width of PWM DAC 2							
<b>PWMDA</b>	0f23H(r/w)	Pulse width of PWM DAC 3							
<b>PWMDA</b>	0f24H(r/w)	Pulse width of PWM DAC 4							

**PWMDA (r/w):** The above-mentioned output pulse width control is used for DAC0-4.

All of PWM DAC converters, after powered on, center on value 80h.

**PWM DAC II**

The TP2808 also provides another 2-channel PWM DAC for low frequency. The frequency of PWM internal clock can be programmed by software from Fosc/1024 to Fosc/131072.

Reg. Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>PWM2EN</b>	0f5fH(r/w)	-	-	-	-	-	-	EN2	EN1
<b>PWMCTL</b>	0f5eH(r/w)	Frequency selection of PWM DAC							
<b>PWM2DA</b>	0f2fH(r/w)	Pulse width of PWM2.1 DAC							
<b>PWM2DA</b>	0f2eH(r/w)	Pulse width of PWM2.0 DAC							



**PWM2EN (r/w):** PWM 2 output enable control register.

EN2 = 1 → Pin "P1.6/PWM2.1" for PWM2.1

= 0 → Pin "P1.6/PWM2.1" for P1.6

EN1 = 1 → Pin "P1.7/PWM2.0" for PWM2.0

= 0 → Pin "P1.7/PWM2.0" for P1.7

**PWMCTL (r/w):** Frequency Adjust Control Register

PWM2 frequency is  $F_{osc}/(512 \cdot PWMCTL)$ .

**PWM2DA (r/w):** The above-mentioned output pulse width control is used for PWM2DAC0-1.

All of PWM DAC converters, after powered on, center on value 80h.

### AD Converter

The TP2808 is installed with four 6-bit A/D converters in  $V_{DD}$  ranges. Software can choose a current converting channel by setting the SAD3/SAD2/SAD1/SAD0 bits. The refresh rate of the ADC may be gained by  $OSC \text{ freq.}/1536$ . The voltage on the input pins is compared with the voltage on the internal  $V_{DD} \times N/64$ , where  $N = 0 - 63$ , by the ADC. The ADC output value is N when pin voltage is higher than  $V_{DD} \times N/64$  and lower than  $V_{DD} \times (N+1)/64$ .

Reg. Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>ADC</b>	0F10H(r)	-	-	ADC converting result					
<b>ADC</b>	0F10(w)	EADC	-	-	-	SAD3	SAD2	SAD1	SAD0

**ADC (w):** ADC control

ENADC = 1 → to enable the ADC

SAD3 = 1 → to select the ADC3 pin input

SAD2 = 1 → to select the ADC2 pin input

SAD1 = 1 → to select the ADC1 pin input

SAD0 = 1 → to select the ADC0 pin input

**ADC (r):** ADC converting result

### Chip ID

Read the SFR address 8EH. The Chip ID is 08H.

PS2, PS1, PS0: Watchdog pre-scaler timer select.

Pre-scaler is selected when set

PS2-0 as follows:

PS2	PS1	PS0	Pre-scaler Select
0	0	0	2
0	1	0	4
0	0	1	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

### Watchdog Timer

The Watchdog timer is a free-running timer, which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of divider that divides the system clock. The divider output is selectable and determines the time-out interval. When the time-out system monitor, this is important for real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked, the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The watchdog timer will be disabled on reset. In general, software should restart the watchdog timer to put it into a known state. The control bits that support the watchdog timer are discussed below.

### Watchdog Timer Control Register (8FH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ENW	CLRW	0	-	-	PS2	PS1	PS0

ENW: Enable watchdog if set.

CLRW: Clear watchdog timer and pre-scaler if set.

This flag will be cleared automatically.

BIT5: Must be "0".

### Clock

The TP2808 is to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the TP2808 relatively insensitive to duty cycle variations in the clock.

### Crystal Oscillator

The TP2808 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

### External Clock

An external clock should be connected to pin XTAL1



and pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5V.

### Power Management

#### Idle Mode

The idle mode can be entered by setting the IDL bit in the PCON register. In this mode, the internal clock to the processor is stopped, and the peripherals and the interrupt logic continue to be blocked. The processor will exit idle mode when either an interrupt or a reset occurs.

#### Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode, all of the clocks are stopped, including the oscillator. Exit from power-down mode is reached by a hardware reset or external interrupts INT0 to INT3 when enabled and set to level triggered.

#### Reduce EMI Emission

The TP2808 allows the user to diminish the gain of on-chip oscillator amplifier by using programmer to clear the B3 bit of CHPCON register. Once B3 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier. Reducing a half of gain may affect the

external crystal operating improperly at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

#### Reduce EMI Emission (Disable ALE Output)

The TP2808 allows users to reduce the EMI emission by setting the ALEdis bit in the CHPCON register. This function will disable the clock signal in Fosc/6Hz output to the ALE pin.

#### Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the TP2808 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During the reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

#### HVSYNC Wake-up Detector

There is a HSYNC and VSYNC signal detector in TP2808. It can detect HSYNC and VSYNC is present or not to wake up other IC in the system. The expressions of the registers are listed below:

Reg. name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>HCNTH</b>	F41h(r)	HF15	HF14	HF13	HF12	HF11	HF10	HF9	HF8
<b>HCNTL</b>	F42h(r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
<b>VCNTH</b>	F43h(r)	VF15	VF14	VF13	VF12	VF11	VF10	VF9	VF8
<b>VCNTL</b>	F44h(r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
<b>VCCNTH</b>	F45h(r)	VCF15	VCF14	VCF13	VCF12	VCF11	VCF10	VCF9	VCF8
<b>VCCNTL</b>	F46h(r)	VCF7	VCF6	VCF5	VCF4	VCF3	VCF2	VCF1	VCF0

#### HCNTL(r):

HF15 – HF8: high byte of H-Freq counter

#### HCNTL(r):

HF7 – HF0: low byte of H-Freq counter

#### VCNTH(r):

VF15 – VF8: high byte of V-Freq counter from VSYNC input

#### VCNTL(r):

VF7 – VF0: low byte of V-Freq counter from VSYNC input

#### VCCNTH(r):

VCF15 – VCF8: high byte of V-Freq counter extracted from HSYNC

#### VCCNTL(r):

VCF7 – VCF0: low byte of V-Freq counter extracted from HSYNC

#### NOTES:

1. HCNT = Freq (OSC)/Freq (HSYNC), it will be updated when the frequency of HSYNC continues to change for 8 pulses and at the rising edge of HSYNC.
2. VCNT = Freq (OSC)/Freq (VSYNC)/64, it will be updated when the frequency of VSYNC is changed at rising edge of VSYNC.
3. VCCNT = freq (OSC)/Freq (VSYNC extracted from HSYNC)/64, it will be updated when composite HSYNC is occurred.



## DDC & I2C Interface

The TP2808 switches to DDC2x mode when it detects a high to low transition on the SCL pin. In this mode, the Slave1 of I2C block automatically transmits/receives data to/from the I2C master. The transmitted/received data is taken-from/saved-to the AUXRAM. In simple words, TP2808 can behave as 24C01 EEPROMs. The only thing S/W needs to do is to write the EDID data to AUXRAM.

The TP2808 returns to DDC1 mode if SCL is kept high for 128 VSYNC clock period. However, it locks in DDC2B mode if a valid I2C address has been detected on SCL/SDA buses.

The TP2808 has 6 slave addresses and they are described as below:

### 1. Slave1

Its device address is fixed (A0H/A1H). In this mode, TP2808 will work as 24C01 EEPROM, and its word address can be accessed from 00H to 7FH. The data will be read/written to/from AUXRAM from address 0200H to 027FH. It is designed for DDC2/DDC2B mode and the device address can be selected as 5-bit to 7-bit mode by S/W.

### 2. Slave2

Its device address is fixed (6EH/6FH). In the write mode of Slave2, the data will be written into AUXRAM from addresses 0280H to 0302H. It will issue an interrupt when stop bit is received. In the read mode of Slave2, the interrupt will be issued when device address is match and slow down SCL until "Busy" flag is cleared. When data is transmitted, the interrupt will be issued when TXBUF is loaded into slave transmission buffer to indicate the buffer is empty. It is designed for DDC2Bi mode.

### 3. Slave3

Its device address is fixed (60H). In this mode, the TP2808 is always active at write mode. The only one byte is stored at DATA1 register and issues an interrupt when stop bit is received.

### 4. Slave4

Its device address is flexible and defined by ADDR4 register. In this mode, TP2808 works as 24C01 EEPROM, and writes/reads data to/from AUXRAM. The interrupt will not be issued in this mode.

### 5. Slave5

Its device address is flexible and defined by ADDR5 register. In this mode, the TP2808 will receives/transmits two bytes to/from DATA1 and DATA2 register. In the write mode, the interrupt will be issued when stop bit is received. The interrupt will not be issued in the read mode.

### 6. Slave6

Its device address is flexible and defined by ADDR6 register. In this mode, the TP2808 works as a simple I2C slave device. In the write mode, it will issue an interrupt when slave receives one byte data or stop bit. In the read mode, it will issue an interrupt when device address is matched or TX buffer is empty. The TX buffer will be loaded into slave transmission buffer at the beginning of slave transmission and then causes a TX buffer empty.

When the slave is too busy to response the master's requirement, there are two ways to slow down SCL. If the value of the DELLE1 register is not zero, SCL will be always pulled down a while when SCL is turned low. The period of pulling down SCL is defined as the description of DELLE1. If the value of the DELLE2 register is not zero, SCL will be pulled down a while when "Busy" flag is 1. The delay condition will be canceled only to write a 0 to "Busy" flag. When the delay conditions of DELLE1 and DELLE2 are both matched, it will delay the longest time.





Reg. name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>I2CCTL1</b>	0f01H(w)	-	-	ENI6	ENI5	-	ENI3	ENI2	ENI1
<b>I2CCTL2</b>	0f02H(w)	IP	ENI2C	-	-	-	EN3	EN2	EN1
<b>INTFLG1</b>	0f03H(r/w)	-	WI1	RI2	WI2	-	WI3	-	-
<b>INTFLG2</b>	0f04H(r/w)	-	WI5	RI6	WI6	-	-	STR	STP
<b>STUS</b>	0f05H(r/w)	-	-	-	-	-	-	-	Busy
<b>ADDR4</b>	0f06H(w)	Slave4 address							EN4
<b>ADDR5</b>	0f07H(w)	Slave5 address							EN5
<b>ADDR6</b>	0f08H(w)	Slave6 address							EN6
<b>DATA1</b>	0f09H(r/w)	RX Data of the first byte/TX buffer							
<b>DATA2</b>	0f0aH(r/w)	RX/TX Data of the second byte for Slave5							
<b>SADDR</b>	0f0bH(r)	Start address of word address							
<b>SWDLEN</b>	0f0cH(r)	Byte counter of the I2C received data							
<b>DDCFLG</b>	0f0dH(r/w)	DDC1	-	-	-	-	-	As1	As0
<b>DELLE1</b>	0f0eH(w)	Period of pulling down SCL (always)							
<b>DELLE2</b>	0f0fH(w)	Period of pulling down SCL (busy)							

**I2CCTL1 (w):** I2C control register

- ENI1: Slave1 interrupt enable bit. 1 is enabled.
- ENI2: Slave2 interrupt enable bit. 1 is enabled.
- ENI3: Slave3 interrupt enable bit. 1 is enabled.
- ENI5: Slave5 interrupt enable bit. 1 is enabled.
- ENI6: Slave6 interrupt enable bit. 1 is enabled.

**I2CCTL2 (w):** I2C control register

- IP: I2C interrupt priority bit, 1 means high priority.
- ENI2C: enable I2C slave mode, if this bit is "0", all slave functions are disable.
- EN1: Slave1 enable control. 1 is enabled.
- EN2: Slave2 enable control. 1 is enabled.
- EN3: Slave3 enable control. 1 is enabled.

**INTFLG1(r/w):** interrupt flag register, all are cleared by software.

- WI1: 1 is indicated Slave1 write mode interrupt occurred. The interrupt will be issued when Slave1 receives the stop bit. This bit will be cleared by writing a "0" to it. Writing a "1 " to it means no action.
- RI2: 1 is indicated Slave2 write mode interrupt occurred. The interrupt will issue when Slave2 transmitting data buffer is empty or word address matched. This bit will be cleared by writing a "0" to it. Writing a "1 " to it means no action.
- WI2: 1 is indicated Slave2 read mode interrupt occurred. The interrupt will issue when Slave2 receives the stop bit. This bit will be cleared by writing a "0" to it. Writing a "1 " to it means no action.
- WI3: 1 is indicated Slave3 write mode interrupt occurred. The interrupt will be issued when Slave3 receives the stop bit. This

bit will be cleared by writing a "0" to it. Writing a "1 " to it means no action.

**INTFLG2(r/w):** interrupt flag register, all are cleared by software.

- WI5: 1 is indicated Slave5 write mode interrupt occurred. The interrupt will be issued when Slave5 receives the stop bit. This bit will be cleared by writing a "0" to it. Writing a "1 " to it means no action.
- RI6: 1 is indicated Slave6 read mode interrupt occurred. The interrupt will be issued when Slave6 matches device address in the read mode or TXBUF is empty. This bit will be cleared by writing a "0" to it. Writing a "1 " to it means no action.
- WI6: 1 is indicated Slave6 write mode interrupt occurred. The interrupt will be issued when Slave6 receives one byte data or the stop bit. This bit will be cleared by writing a "0" to it. Writing a "1 " to it means no action.
- STR: interrupt is induced by re-start and address match.
- STP: interrupt is induced by stop.
- STUS (r/w):** It will be set when the interrupt is issued. They are cleared only by SW.
- Busy: MCU is busy to deal with Slave interrupt.
- ADDR4 (w):** Address and enable bit of Slave4
  - Bit7-1: Address of Slave4 to response. It is the address of I2C deleting the R/W bit.
  - EN4: Slave4 enable control. 1 is enabled.
- ADDR5 (w):** Address and enable bit of Slave5
  - Bit7-1: Address of Slave5 to response. It is the address of I2C deleting the R/W bit.



EN5: Slave5 enable control. 1 is enabled.

**ADDR6 (w):** Address and enable bit of Slave6

Bit7-1: Address of Slave6 to response. It is the address of I2C deleting the R/W bit.

EN5: Slave5 enable control. 1 is enabled.

**DATA1(r/w):**

This register stores the first byte data received from Slave3, Slave5 or slave6, and it is the transmitting buffer of Slave5 and Slave6. When I2C transmission of slave6 occurs, the buffer is load into I2C and issues a TX buffer empty interrupt.

**DATA2(r/w):**

The second byte data is received/transmitted for Slave5. The interrupt is issued when stop bit is received.

**SADDR(r):**

It is the word address when Slave1, Slave2 or Slave4 is active (as 24C01 EPPROM mode).

**SWDLEN(r):**

The total of bytes is written into AUXRAM when Slave1, Slave2 or Slave4 is active.

**DDCFLG(r/w):**

DDC1: set 1 to enable DDC1 mode.

As1, As0:

As1 = 0, As0 = 0: 7-bit address mode for Slave1

As1 = 0, As0 = 1: 6-bit address mode for Slave1

As1 = 1, As0 = 0: 5-bit address mode for Slave1

**DELCTL1 (w):**

Determine the period of pulling down SCL for each SCL low. The time is calculated by the following equation:  $1/Fosc * [300 * (DELCTL-1) + 1]$ . If its value is 00H, it will cause no any pulling down action on SCL.

**DELCTL2 (w):**

Determine the period of pulling down SCL when all busy flags are not cleared. The time is calculated by the following equation:  $1/Fosc * [300 * (DELCTL-1) + 1]$ . If its value is 00H, it will cause no any pulling down action on SCL.

### Address Mapping

	Word address	AUXRAM address
<b>Slave1</b>	00H-7FH	0200H-027FH
<b>Slave2</b>	-	0280H-0302H
<b>Slave4</b>	00-FFH	0200H-02FFH

### Operation Mode of I2C Slave

	Address	Interrupt	Function
<b>Slave1</b>	A0H/A1H	With	As 24C01, R/W (DDC2, BBC2B)
<b>Slave2</b>	6EH/6FH	With	Write data to AUXRAM from 0280H TX from TX buffer (DDC2Bi)
<b>Slave3</b>	60H	With	Store 1 byte data into register
<b>Slave4</b>	Programmable	Without	As 24C01, R/W
<b>Slave5</b>	Programmable	With	Store/transmit 2 bytes data into register
<b>Slave6</b>	Programmable	With	Simple I2C slave function



TP2808 Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B 00000000								F7
E8	ISP_CTRL 00000000	ISP_ADDR 00000000							EF
E0	+ACC 00000000								E7
D8	+P4 xxxx1111								DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000		RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 0xx00000								C7
B8	+IP 00000000							CHPCON 00000000	BF
B0	+P3 00000000								B7
A8	+1E 00000000								AF
A0	+P2 11111111								A7
98	+SCON 00000000	SBUF xxxxxxx							9F
90	+P1 11111111								97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	ID 00001000	WDTC 00000000	8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00110000	87

In-system Programming Control Register (CHPCON)

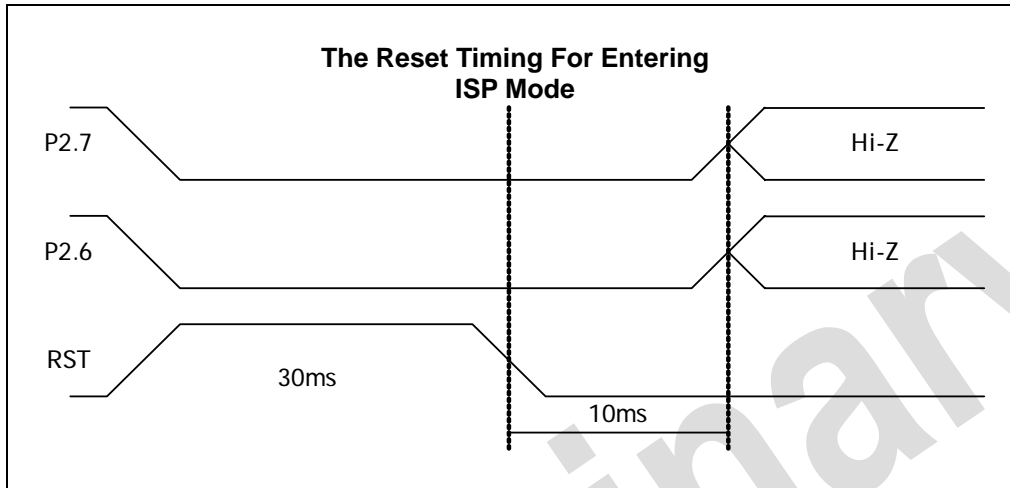
CHPCON (BFH)

Bit	Name	Function
7	SWRESET (F04KMODE)	When this bit is set to 1, and FPROGEN are set to 1, it will enforce microcontroller to reset to initial condition just like power on rest.
6	-	Reserved
5	-	Reserved
4	ENAUXRAM	1: Enable on-chip AUX-RAM, PWM and AD. 0: Disable the on-chip AUX-RAM, PWM and AD.
3	Oscillator Control	TP2808 allows the user to diminish the gain of on-chip oscillator amplifier by using programmer to set the bit B3 of CHPCON register. Once B3 is set to 0, a half of gain will be decreased. Care must be taken if the user attempts to diminish the gain of oscillator amplifier, for reducing a half of gain may improperly affect the external crystal operation at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.
2	DISALE	1: Disable ALE output 0: ALE normal output The default value of the register is 0.
1	0	Must set to 0.
0	FPROGEN	FLASH EPROM Programming Enable = 1: enable. The microcontroller enters the in-system programming mode after entering the idle mode and wake-up from interrupt. During in-system programming mode, the operation of erase, program and read are achieved when device enters idle mode. = 0 0:disable. The on-chip flash memory is read-only. In-system programmability is disabled.



ISP Mode (Boot from LDROM)

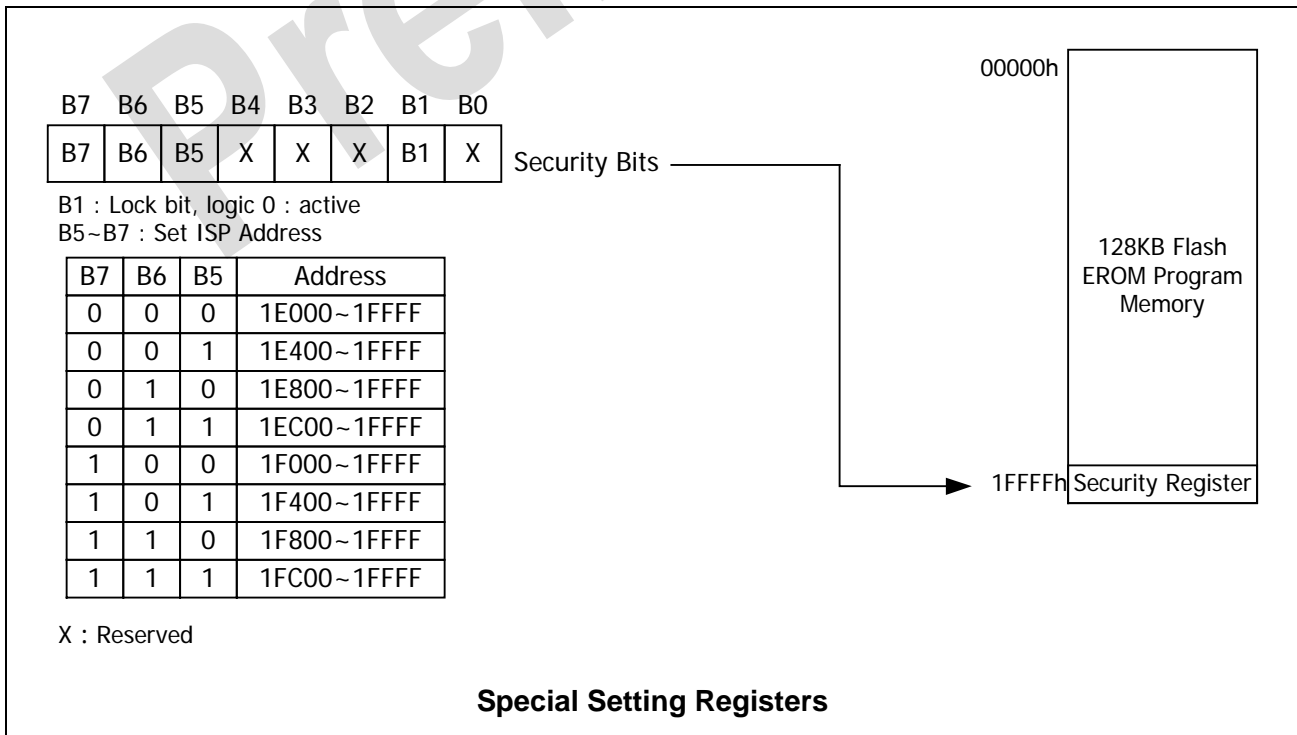
P4.3	P2.7	P2.6	MODE
X	L	L	ISP
L	X	X	ISP



Security

During the on-chip FLASH EPROM programming mode, the FLASH EPROM can be programmed and verified repeatedly. Until the code inside the FLASH EPROM is confirmed OK, the code can be protected. The protection of FLASH EPROM and those operations on it are described below.

The TP2808 has several Special Setting Registers, including the Security Register, which cannot be programmed from high to low. They can only be reset through erases-all operation.



Lock Bit

This bit is used to protect the customer's program code in the TP2808. It may be set after the programmer finishes the



programming and verifies the sequence. Once this bit is set to logic 0, both the Flash EROM data and Setting Registers cannot be accessed again.

### Absolute Maximum Ratings

( $V_{DD} - V_{SS} = 5V \pm 10\%$  for TP2808H,  $V_{DD} - V_{SS} = 3.3V \pm 10\%$  for TP2808L)

Parameter	Symbol	Ratings	Unit
DC Power Supply	$V_{DD} - V_{SS}$	-0.3 ~ +6.0	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.3 \sim V_{DD} + 0.3$	V
Operation Temperature	$T_A$	0 ~ 70	°C
Storage Temperature	$T_{STG}$	-55 ~ +150	°C

NOTE: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### DC Electrical Characteristics

( $V_{DD} - V_{SS} = 5V \pm 10\%$  for TP2808H,  $V_{DD} - V_{SS} = 3.3V \pm 10\%$  for TP2808L,  $T_A = 25^\circ\text{C}$ ,  $F_{osc} = 12\text{MHz}$ , unless otherwise specified)

Symbol	Parameter	Limit			Test Conditions
		Min	Max	Unit	
$V_{DD}$	Operating Voltage	0.9 $V_{DD}$	1.1 $V_{DD}$	V	RST=1, P0= $V_{DD}$
$I_{DD}$	Operating Current	-	20/8	mA	No load $V_{DD} = 5V/3.3V$
$I_{IDLE}$	Idle Current	-	6/3	mA	Idle mode $V_{DD} = 5V/3.3V$
$I_{PWDN}$	Power Down Current	-	100	$\mu\text{A}$	Power-down mode $V_{DD} = 5V/3.3V$
$I_{IN1}$	Input Current P1, P2, P3, P4	-50	+10	$\mu\text{A}$	$V_{IN} = 0V$ or $V_{DD}$
$I_{IN2}$	Input Current RST	-10	+300	$\mu\text{A}$	$0 < V_{IN} < V_{DD}$
$V_{IL1}$	Input Low Voltage P0, P1, P3, P4, EA	0	$0.2V_{DD} - 0.2$	V	$V_{DD}$
$V_{IL2}$	Input Low Voltage RST	0	$0.2V_{DD} - 0.2$	V	$V_{DD}$
$V_{IL3}$	Input Low Voltage XTAL1 <sup>(*)4</sup>	0	$0.2V_{DD} - 0.3$	V	$V_{DD}$
$V_{IH1}$	Output Low Voltage P1, P2, P3, P4, EA	3.5/2.6	$V_{DD} + 0.2$	V	$V_{DD} = 5V/3.3V$
$V_{IH2}$	Input High Voltage RST	3.5/2.6	$V_{DD} + 0.2$	V	$V_{DD} = 5V/3.3V$
$V_{IH3}$	Input High Voltage XTAL1 <sup>(*)4</sup>	3.5/2.6	$V_{DD} + 0.2$	V	$V_{DD} = 5V/3.3V$
$V_{OL1}$	Output Low Voltage P1, P2, P3, P4	-	0.45	V	$V_{DD} = 5V/3.3V$ $I_{OL} = +2\text{mA}$
$V_{OL2}$	Output Low Voltage P0, ALE, PSEN <sup>(*)3</sup>	-	0.45	V	$V_{DD} = 5V/3.3V$ $I_{OL} = +4\text{mA}$
$I_{SK1}$	Sink current P1, P3, P4	-	8/6	mA	$V_{DD} = 5V/3.3V$ $V_{in} = -0.45\text{V}$
$I_{SK2}$	Sink current P0, P2, ALE, PSEN	-	8/6	mA	$V_{DD} = 5V/3.3V$ $V_{in} = 0.45\text{V}$
$V_{OH1}$	Output Low Voltage P1, P2, P3, P4	2.4/2.0	-	V	$V_{DD} = 5V/3.3V$
$V_{OH2}$	Output High Voltage P0, ALE, PSEN <sup>(*)3</sup>	2.4/2.0	-	V	$V_{DD} = 5V/3.3V$
$I_{SF1}$	Source current P0, P2, P3, P4	-120/-80	-200/-120	$\mu\text{A}$	$V_{DD} = 5V/3.3V$ $V_{in} = 2.4\text{V}$

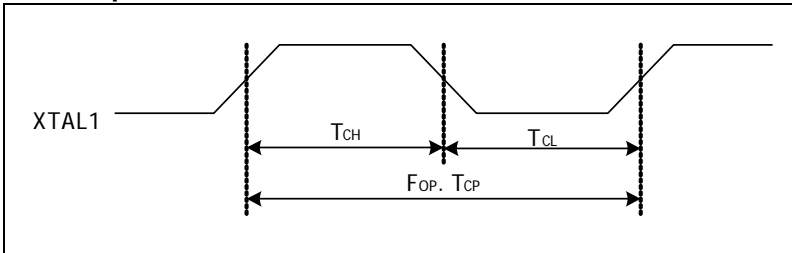
#### NOTES:

- \*1. RST pin is an Schmitt trigger input.
- \*2. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven 1 to 0. The transition current reaches its maximum value when  $V_{IN}$  approximates to 2V.
- \*3. P0, ALE and /PSEN are tested in the external access mode.
- \*4. XTAL1 is a CMOS input.

### AC Electrical Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods ( $T_{CP}$ ), and actual parts will usually experience less than a  $\pm 20$  nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

#### Clock Input Waveform



Parameter	Symbol	Limit		Unit	Notes
		Min	Max		
Operating Speed	$F_{OP}$	0	40	MHz	1
Clock Period	$T_{CP}$	25	-	nS	2
Clock High	$T_{CH}$	10	-	nS	3
Clock Low	$T_{CL}$	10	-	nS	3

- NOTES:
1. The clock may be stopped indefinitely in either state.
  2. The  $T_{CP}$  specification is used as a reference in other specifications.
  3. There are no duty cycle requirements on the XTAL 1 input.

#### Program Fetch Cycle

Parameter	Symbol	Limit			Unit	Notes
		Min	Typ	Max		
Address Valid to ALE Low	$T_{AAS}$	$1 T_{CP} -$	-	-	nS	4
Address Hold from ALE Low	$T_{AAH}$	$1 T_{CP} -$	-	-	nS	1, 4
ALE Low PSEN Low	$T_{APL}$	$1 T_{CP} -$	-	-	nS	4
PSEN Low to Data Valid	$T_{PDA}$	-	-	$2 T_{CP}$	nS	2
Data Hold after PSEN High	$T_{PDH}$	0	-	$1 T_{CP}$	nS	3
Data Float after PSEN High	$T_{PDZ}$	0	-	$1 T_{CP}$	nS	-
ALE Pulse Width	$T_{ALW}$	$2 T_{CP} -$	$2 T_C$	-	nS	4
PSEN Pulse Width	$T_{PSW}$	$3 T_{CP} -$	$3 T_{CP}$	-	nS	4

- NOTES:
1. P0.0-P0.7 remains stable throughout entire memory cycle.
  2. Memory access time is  $3 T_{CP}$ .
  3. Data have been latched internally prior to PSEN going high.
  4. " " (due to buffer driving delay and wire loading) is 20 nS.

#### Data Read Cycle

Parameter	Symbol	Limit			Unit	Notes
		Min	Typ	Max		
ALE Low to RD Low	$T_{DAR}$	$3 T_{CP} -$	-	$-3 T_{CP} +$	nS	1, 2
RD Low to Data Valid	$T_{DDA}$	-	-	$4 T_{CP}$	nS	1
Data Hold from RD High	$T_{DDH}$	0	-	$2 T_{CP}$	nS	-
Data Float from RD High	$T_{DDZ}$	0	-	$2 T_{CP}$	nS	-
RD Pulse Width	$T_{DRD}$	$6 T_{CP} -$	$6 T_{CP}$	-	nS	2

- NOTES:
1. Data memory access time is  $8 T_{CP}$ .
  2. " " (due to buffer driving delay and wire loading) is 20 nS.



Data Write Cycle

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
ALE Low WR Low	T <sub>DAW</sub>	3 T <sub>CP</sub>	-	3 T <sub>CP</sub>	nS
Data Valid to WR Low	T <sub>DAD</sub>	1 T <sub>CP</sub>	-	-	nS
Data Hold from WR High	T <sub>DWD</sub>	1 T <sub>CP</sub>	-	-	nS
WR Pulse Width	T <sub>DWR</sub>	6 T <sub>CP</sub>	6 T <sub>CP</sub>	-	nS

NOTE: " " ( due to buffer driving delay and wire loading ) is 20 nS.

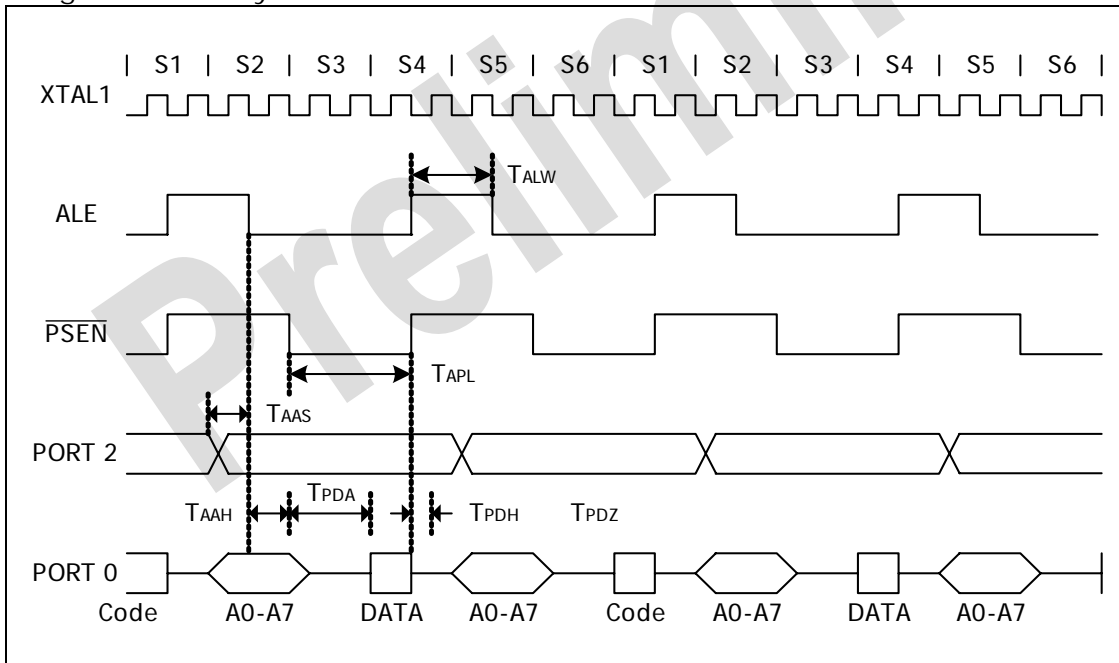
Port Access Cycle

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Port Input Setup to ALE Low	T <sub>PDS</sub>	1 T <sub>CP</sub>	-	-	nS
Port Input Hold from ALE Low	T <sub>PDH</sub>	0	-	-	nS
Port Output to ALE	T <sub>PDA</sub>	1 T <sub>CP</sub>	-	-	nS

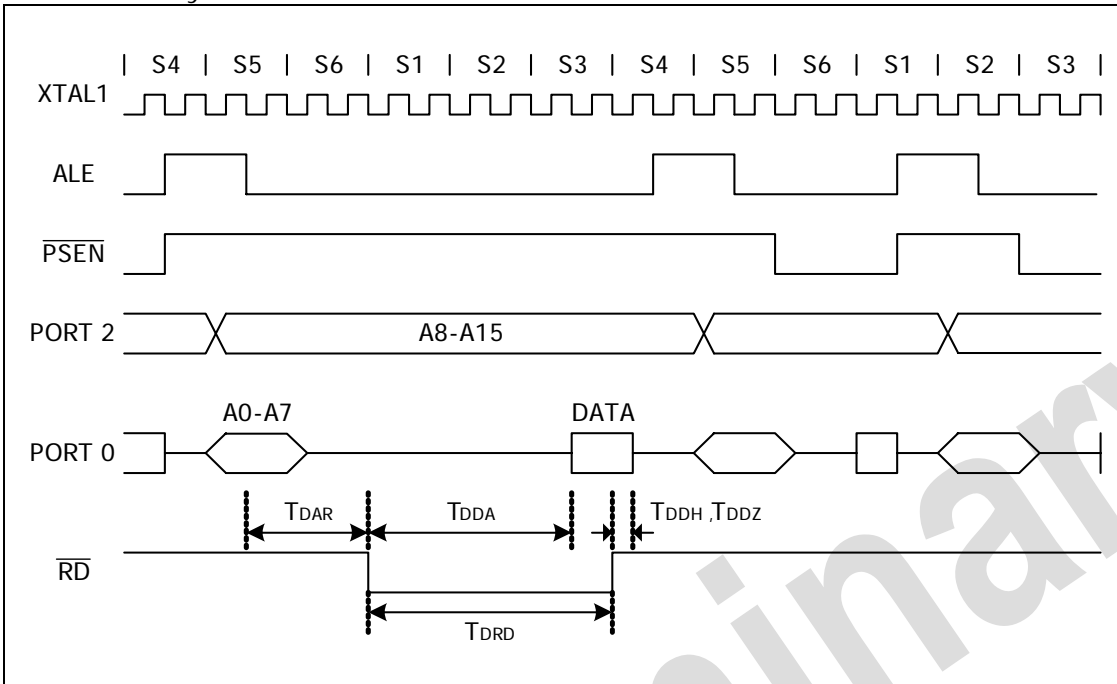
NOTE: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

Timing Waveforms of AC Electrical Characteristics

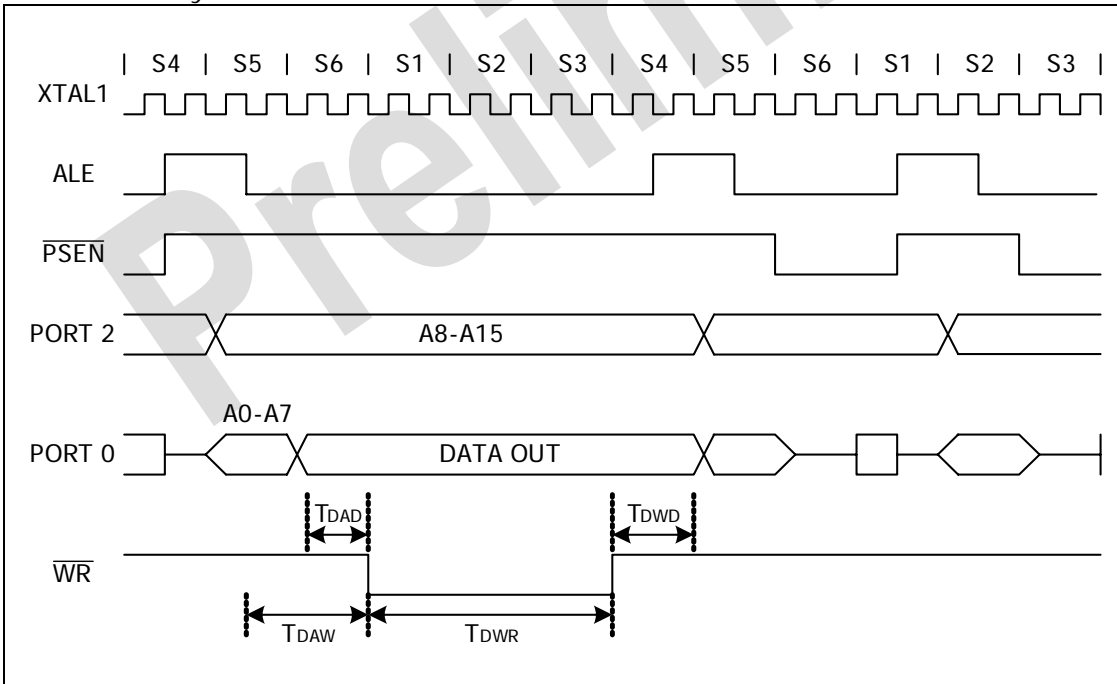
Program Fetch Cycle



### Data Read Cycle

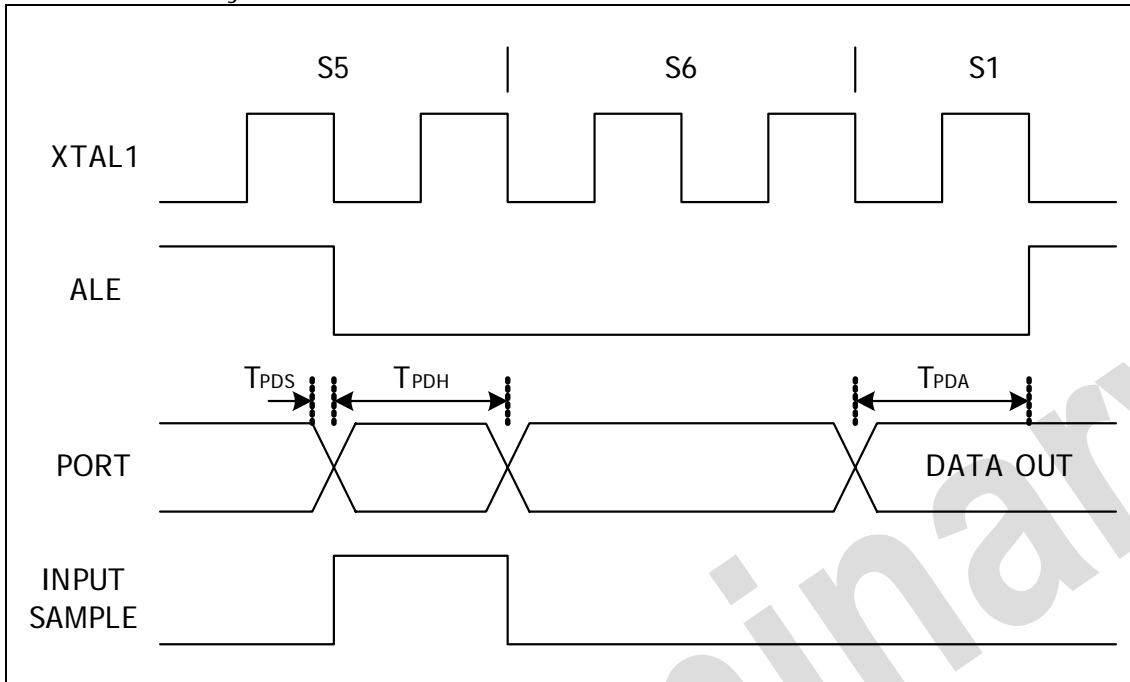


### Data Write Cycle





### Port Access Cycle



Preliminary

### Application Diagrams

#### Typical Application Circuits

#### Expanded External Program Memory and Crystal

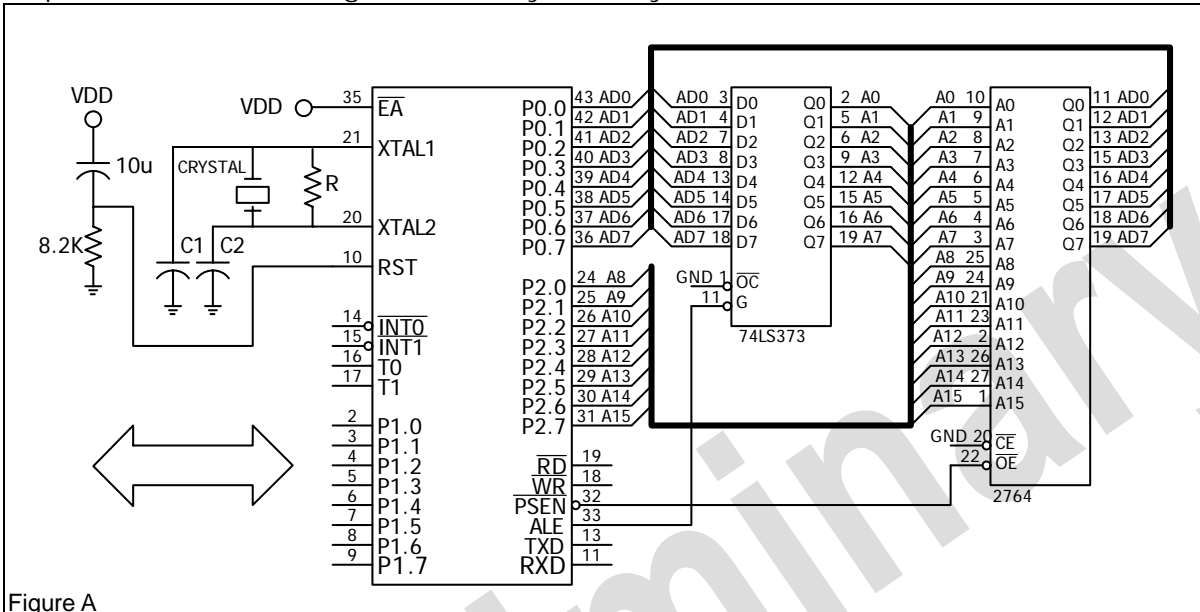


Figure A

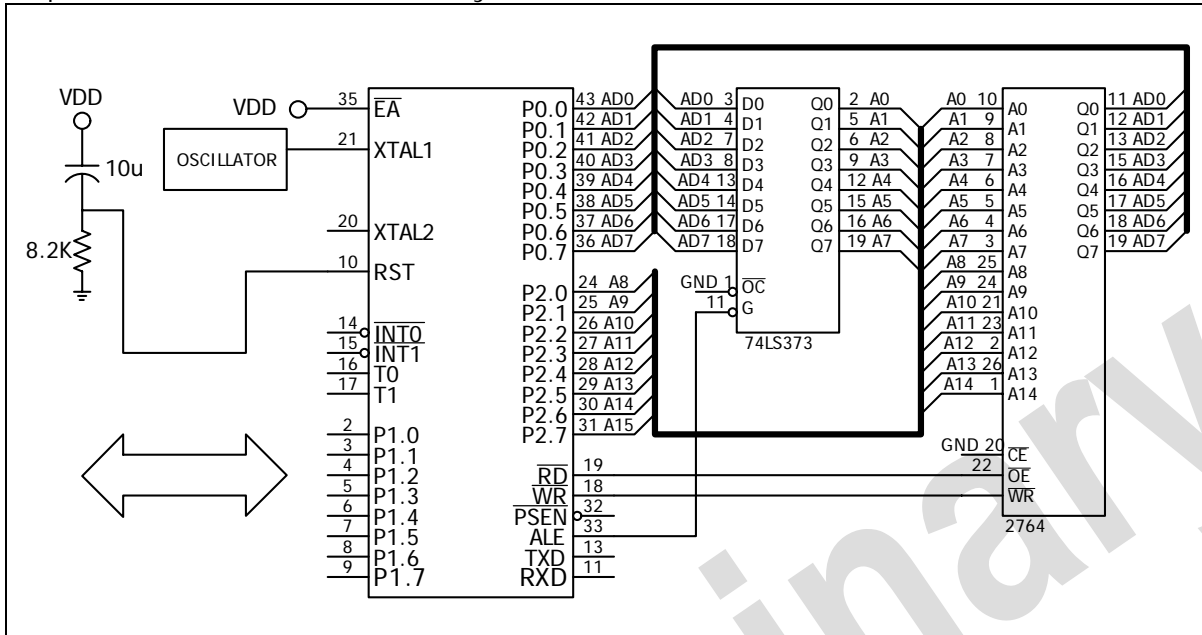
The following table shows the reference values for the crystal applications:

Crystal	C1	C2	R
6MHz	47P	47P	-
16MHz	30P	30P	-
24MHz	15P	15P	-
32MHz	10P	10P	6.8K
40MHz	5P	5P	4.7K

#### NOTES:

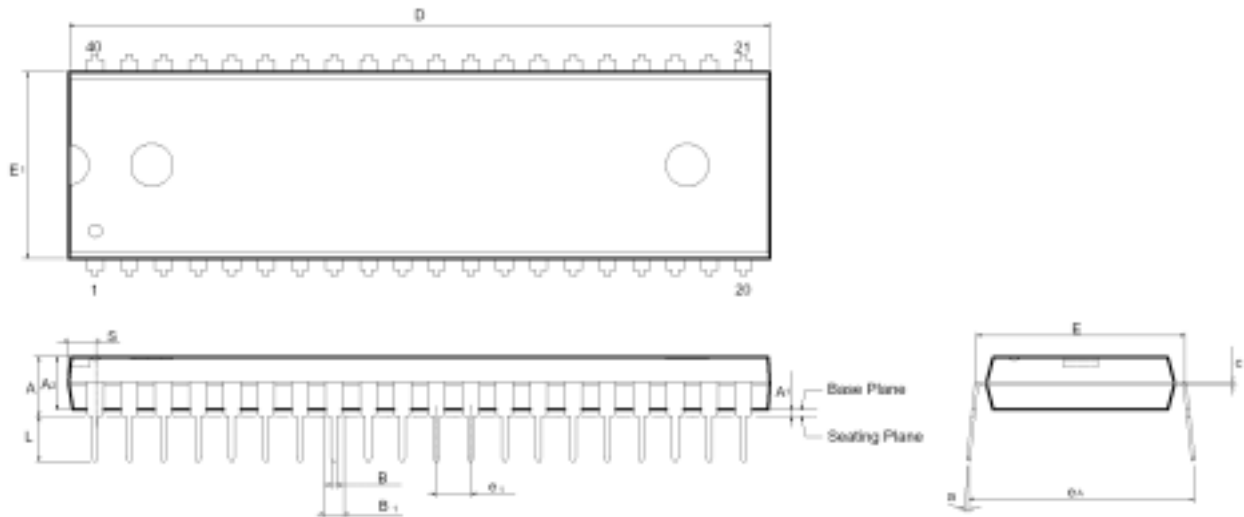
1. Please refer to Figure A for C1, C2 and R components.
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

### Expanded External Data Memory and Oscillator



### Package Information

#### 40-pin DIP



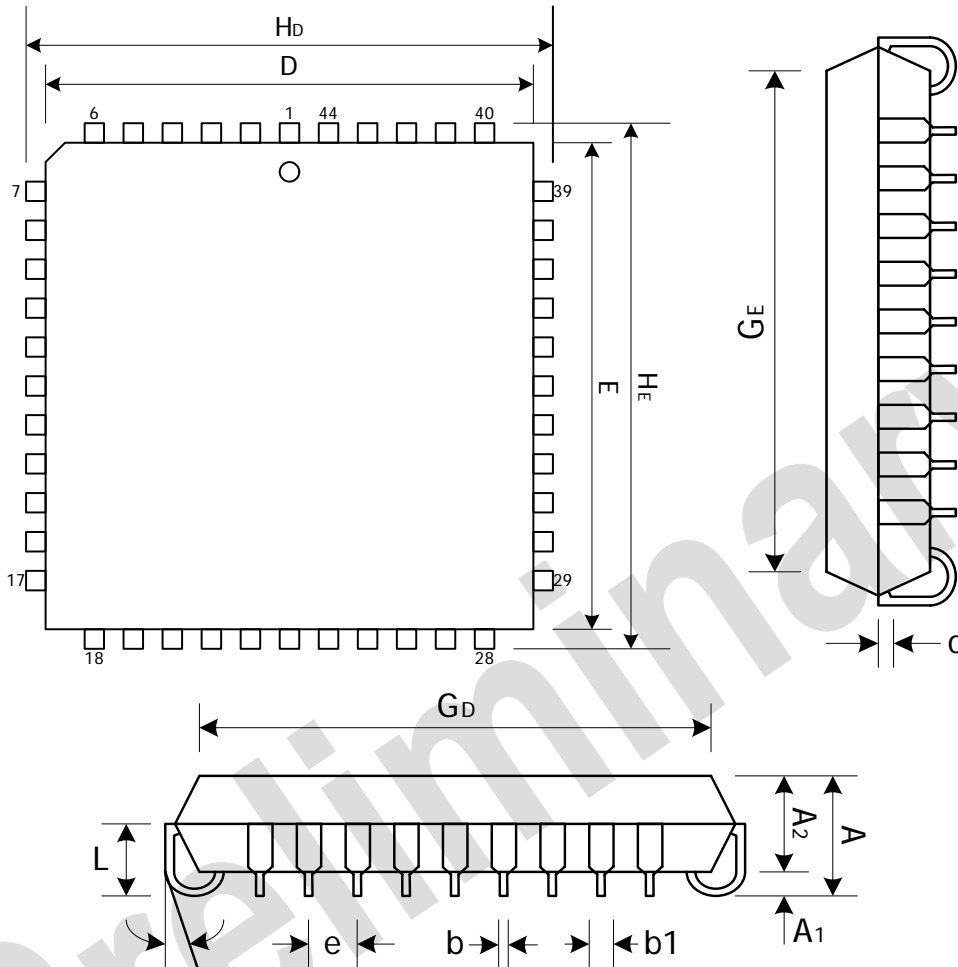
Unit: Inch

Symbol	Dimension in Inch		
	Min.	Nom.	Max.
A	—	—	0.220
A1	0.015	—	—
A2	0.150	0.155	0.160
B	—	0.018	—
B1	—	0.050	—
D	2.055	2.060	2.070
E	0.600 BSC		
E1	0.540	0.545	0.550
e1	—	0.100	—
L	0.115	0.130	0.150
a	0	7	15
eA	0.630	0.650	0.670

#### NOTES:

1. Dimension D Max. includes mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D and E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dam bar protrusion/intrusion.
5. JEDEC Outline: MS-011 AC

### 44-pin PLCC



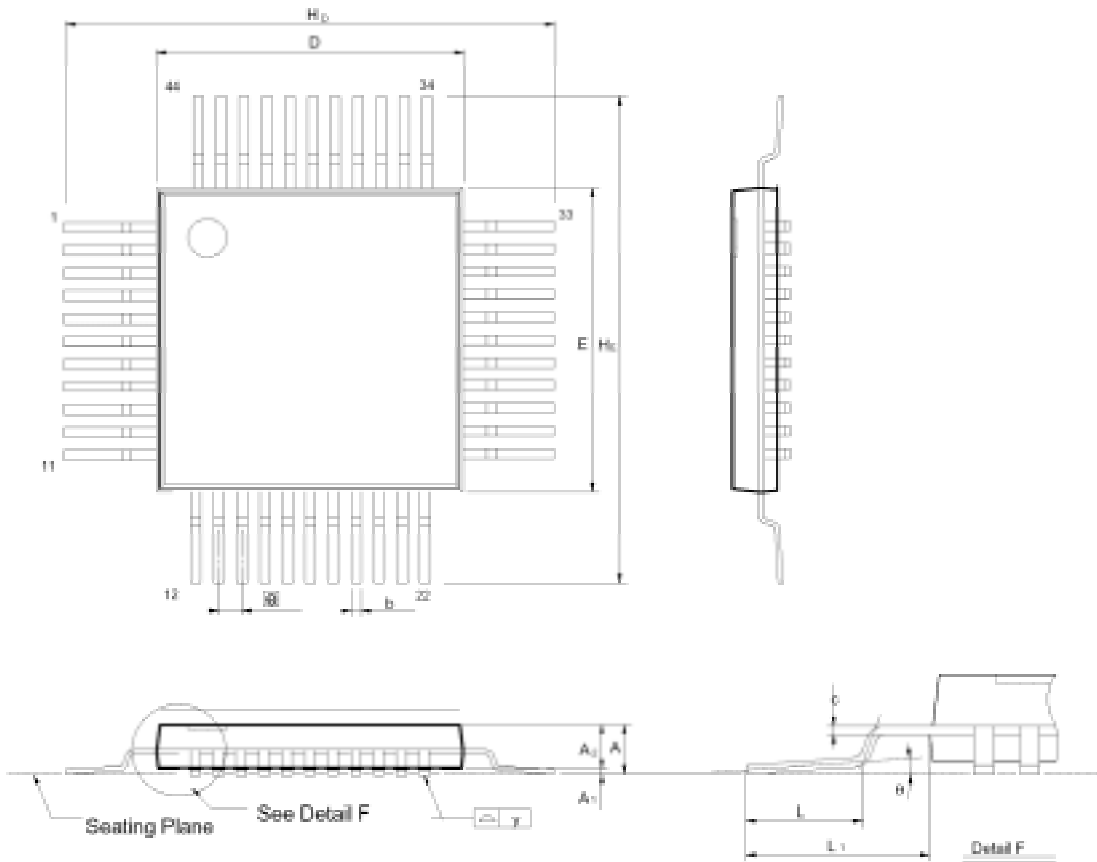
Unit: Inch

Symbol	Dimension in Inch		
	Min.	Nom.	Max.
A	—	—	0.185
A1	0.020	—	—
A2	0.145	0.150	0.155
b1	0.026	0.028	0.032
b	0.016	0.018	0.022
c	0.007	0.010	0.013
D	0.648	0.653	0.658
E	0.648	0.653	0.658
e	0.050 BSC		
$G_D$	0.590	0.610	0.630
$G_E$	0.590	0.610	0.630
$H_b$	0.680	0.690	0.700
$H_E$	0.680	0.690	0.700
L	0.090	0.100	0.110

#### NOTES:

1. Dimensions D and E do not include interlead flash and mold protrusion. Allowable protrusion is 10 mil per side.
2. Dimension b1 does not include dam bar protrusion/intrusion.
3. JEDEC Outline: M0-047 AC.

### 44-pin PQFP



Unit: Millimeter

Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	—	—	2.7
A1	0.25	—	0.5
A2	1.9	2.0	2.2
b	0.3 TYP.		
c	0.10	0.15	0.20
D	9.9	10.00	10.1
E	9.9	10.00	10.1
e	0.80 TYP.		
H <sub>b</sub>	13	13.2	13.4
H <sub>c</sub>	13	13.2	13.4
L	0.73	0.88	0.93
L1	—	1.6	—
y	0.10		
°	0°	—	7°

#### NOTES:

1. Dimensions D and E do not include interlead flash.
2. Dimension b does not include dam bar protrusion/intrusion.
3. JEDEC Outline: MO-108 AA-1.



TP2808

8051 MICROCONTROLLER WITH 128K FLASH AND ISP

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Preliminary

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