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P1 98.2

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1794 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 2.8 \Omega$ ($V_{GS} = 10 V, I_D = 3 A$)
- Low C_{iss} $C_{iss} = 1\ 000\ pF$ TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

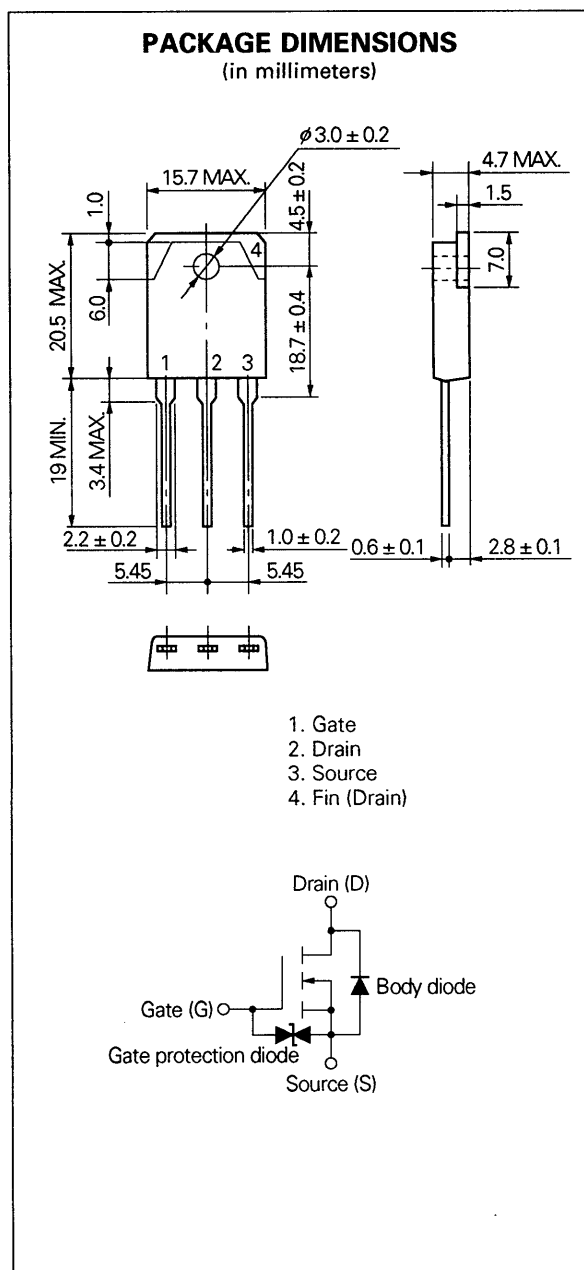
ABSOLUTE MAXIMUM RATINGS ($T_a = 25\ ^\circ C$)

| | | | |
|--|------------------|-------------|------------|
| Drain to Source Voltage | V_{DSS} | 900 | V |
| Gate to Source Voltage | V_{GSS} | ± 30 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ± 6.0 | A |
| Drain Current (pulse) | $I_{D(pulse)^*}$ | ± 12 | A |
| Total Power Dissipation ($T_c = 25\ ^\circ C$) | P_T | 100 | W |
| Channel Temperature | T_{ch} | 150 | $^\circ C$ |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ C$ |
| Single Avalanche Current | I_{AS}^{**} | 6.0 | A |
| Single Avalanche Energy | E_{AS}^{**} | 22 | mJ |

* $PW \leq 10\ \mu s$, Duty Cycle $\leq 1\ %$

** Starting $T_{ch} = 25\ ^\circ C$, $R_G = 25\ \Omega$, $V_{GS} = 20\ V \rightarrow 0$

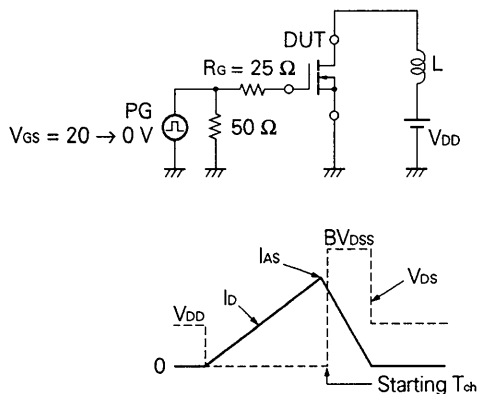
PACKAGE DIMENSIONS
 (in millimeters)



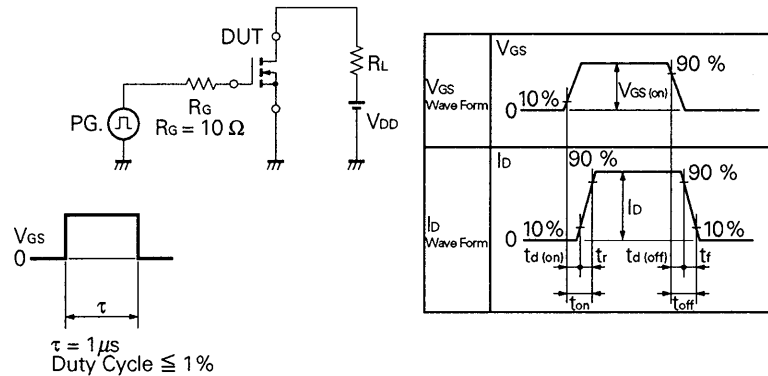
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|-------|------|------|---|
| Drain to Source On-state Resistance | R _{DS(on)} | | 2.4 | 2.8 | Ω | V _{GS} = 10 V, I _D = 3 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | 2.5 | | 3.5 | V | V _{DS} = 10 V, I _D = 1 mA |
| Forward Transfer Admittance | y _{fs} | 2.0 | 6.0 | | S | V _{DS} = 20 V, I _D = 3 A |
| Drain Leakage Current | I _{DSS} | | | 100 | μA | V _{DS} = 900 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±10 | μA | V _{GS} = ±30 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 1 000 | | pF | V _{DS} = 10 V V _{GS} = 0 f = 1 MHz |
| Output Capacitance | C _{oss} | | 170 | | pF | |
| Reverse Transfer Capacitance | C _{rss} | | 60 | | pF | |
| Turn-On Delay Time | t _{d(on)} | | 20 | | ns | V _{GS} = 10 V V _{DD} = 150 V I _D = 3 A, R _G = 10 Ω R _L = 50 Ω |
| Rise Time | t _r | | 30 | | ns | |
| Turn-Off Delay Time | t _{d(off)} | | 85 | | ns | |
| Fall Time | t _f | | 20 | | ns | |
| Total Gate Charge | Q _G | | 42 | | nC | V _{GS} = 10 V I _D = 6 A V _{DD} = 720 V |
| Gate to Source Charge | Q _{GS} | | 10 | | nC | |
| Gate to Drain Charge | Q _{GD} | | 17 | | nC | |
| Diode Forward Voltage | V _{F(S-D)} | | 0.9 | | V | I _F = 6 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 680 | | ns | I _F = 6 A di/dt = 50 A/μs |
| Reverse Recovery Charge | Q _{rr} | | 4.8 | | μC | |

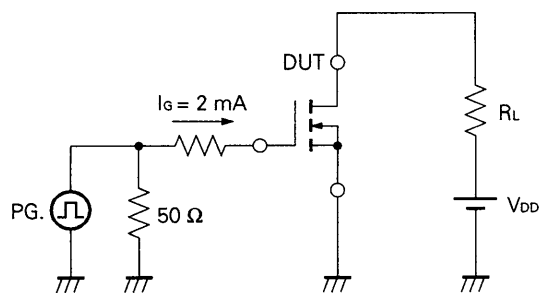
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

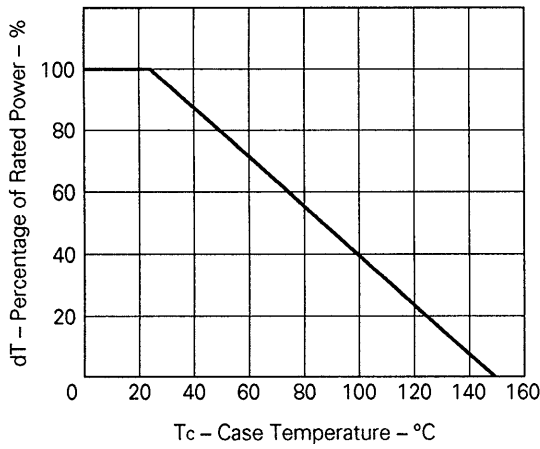


Test Circuit 3: Gate Charge

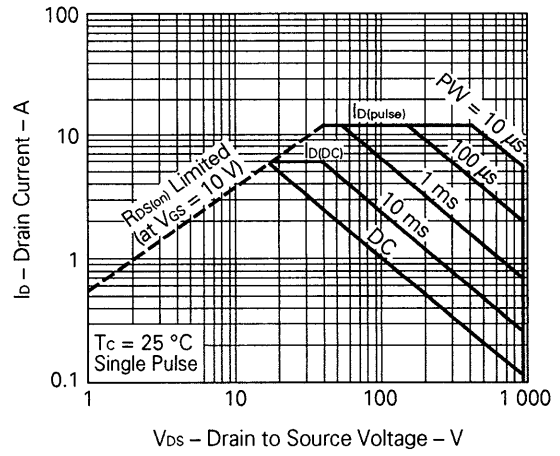


TYPICAL CHARACTERISTICS (T_a = 25 °C)

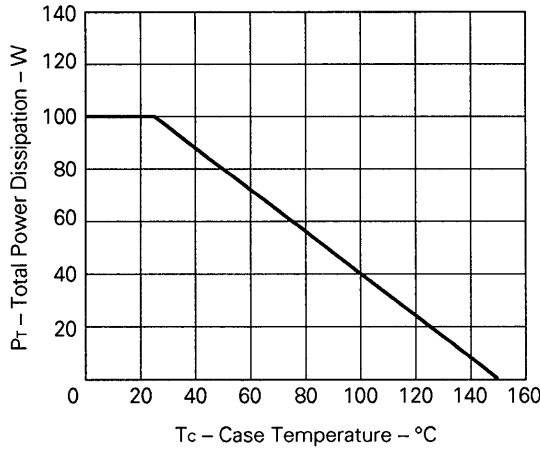
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



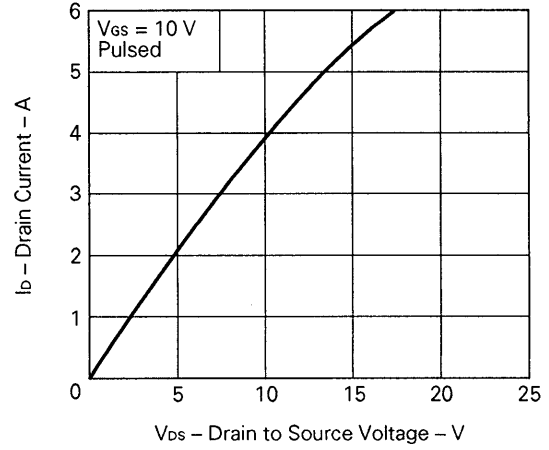
FORWARD BIAS SAFE OPERATING AREA



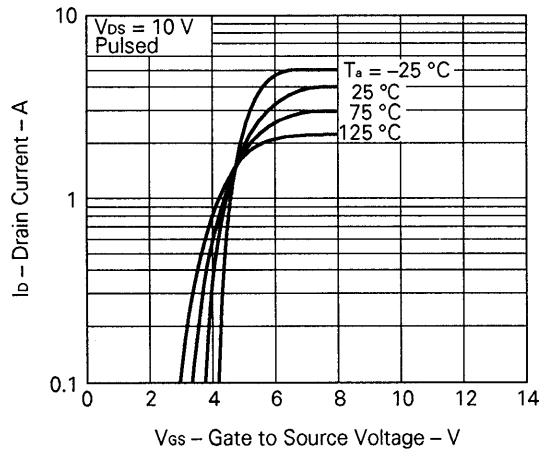
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



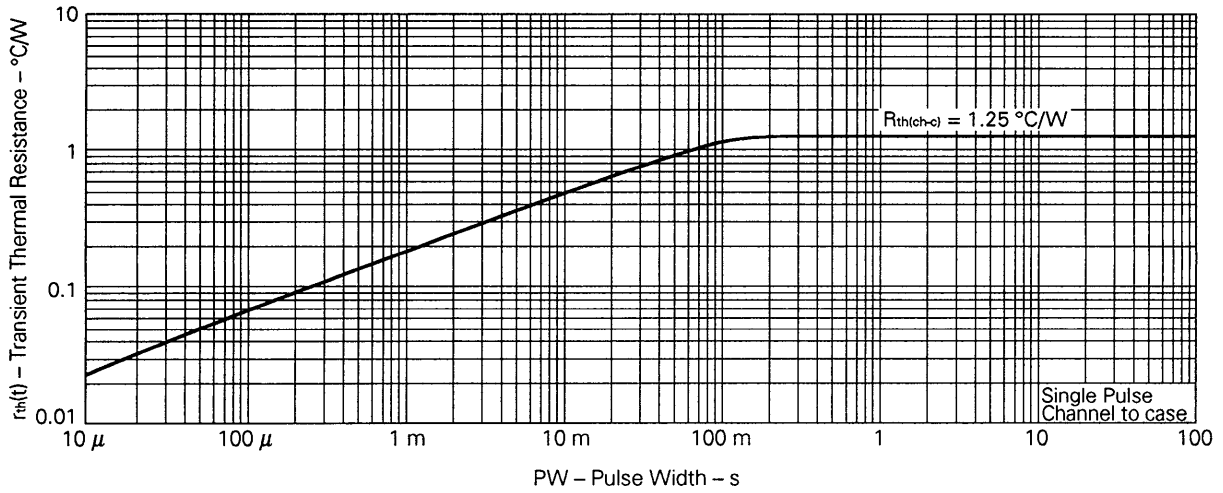
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



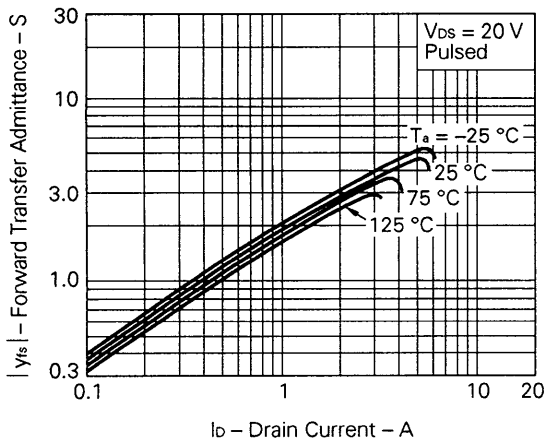
TRANSFER CHARACTERISTICS



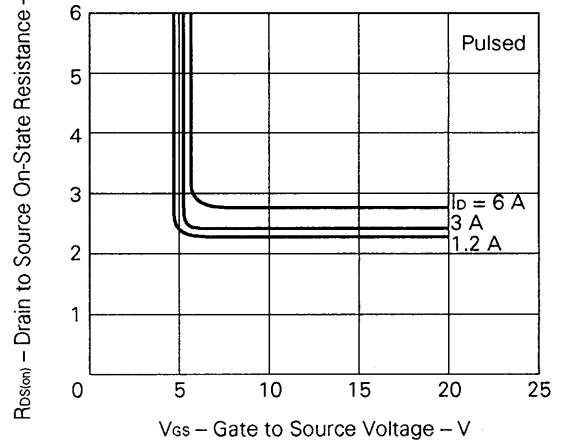
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



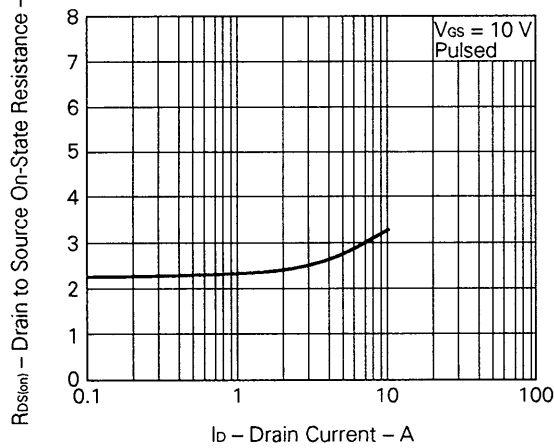
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



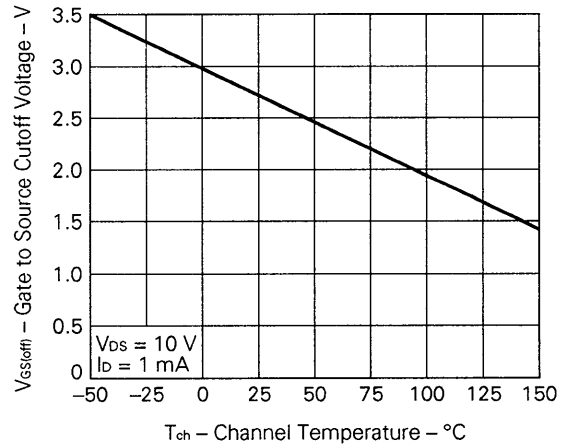
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

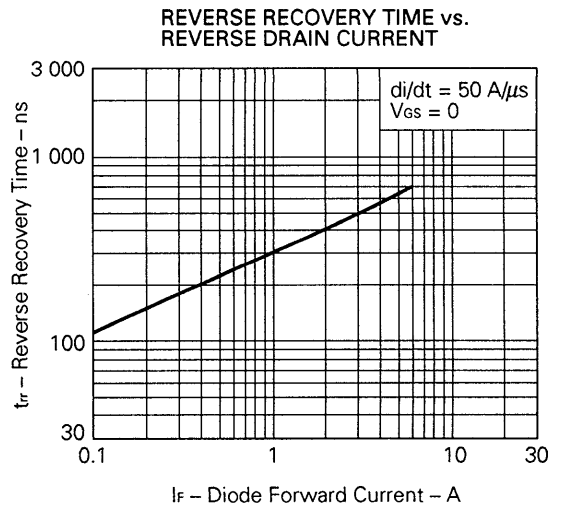
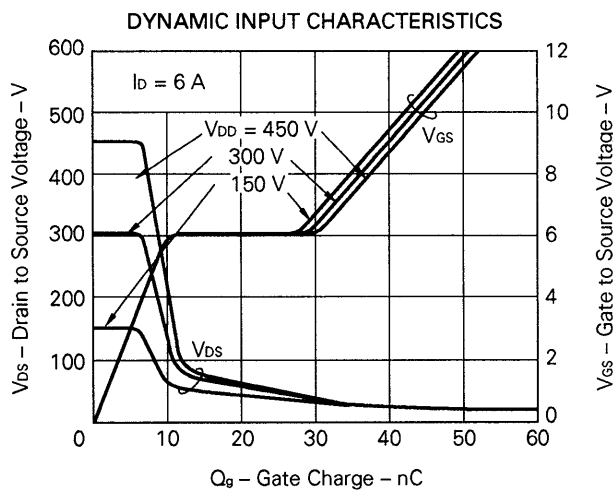
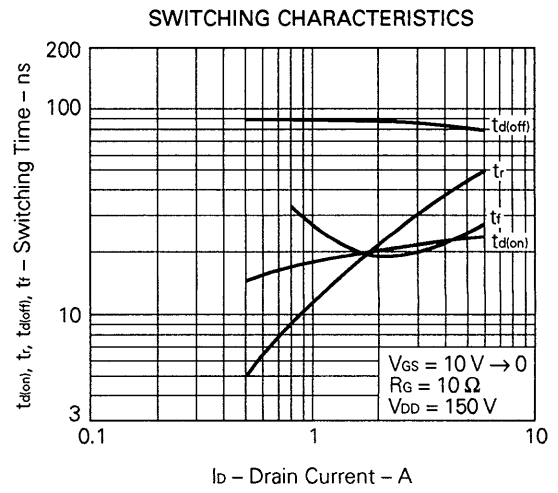
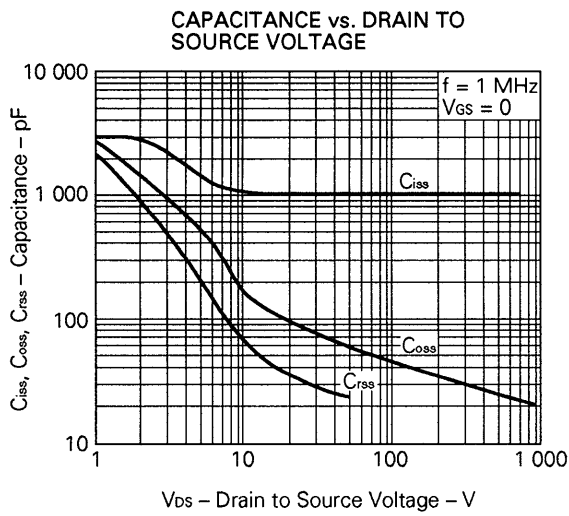
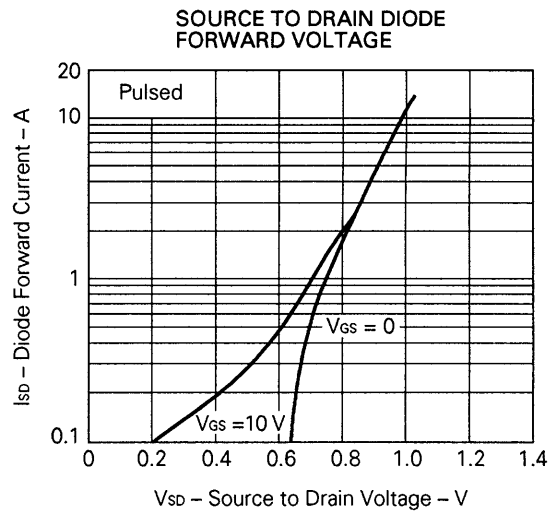
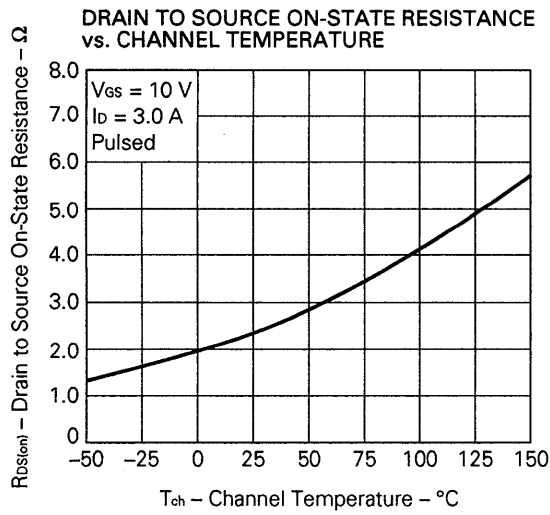


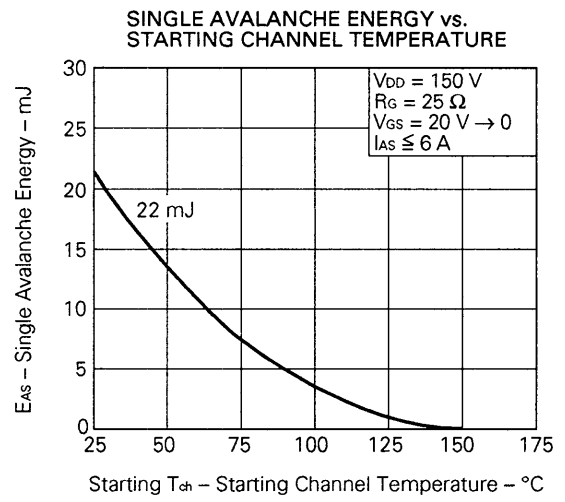
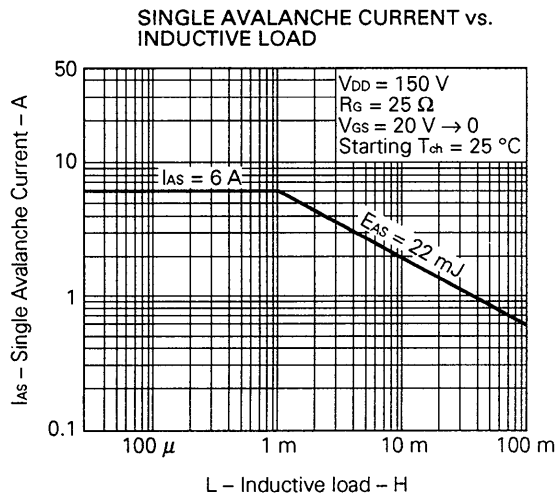
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







Reference

| Application note name | No. |
|--|----------|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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