8003
EDLC® Ethernet Data Link Controller

May 1991

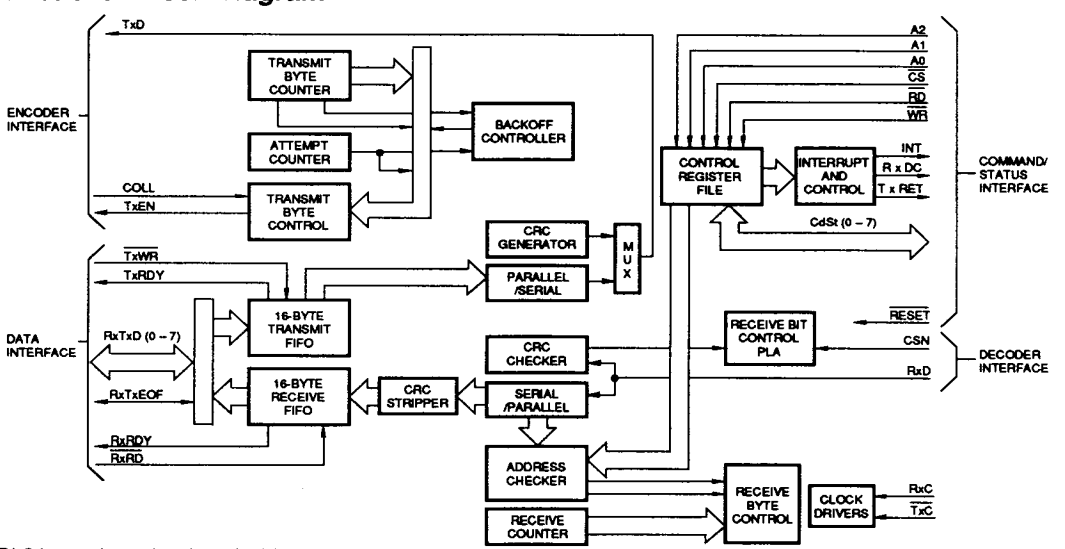
Features

- Optimized for Burst Mode DMA Applications
- 100% Ethernet/IEEE 802.3 (10BASE5) and IEEE 802.3/CHEAPERNET (10BASE2)
- 10 MHz Serial/Parallel Conversion
- Preamble Generation and Removal
- Automatic 32-Bit FCS (CRC) Generation and Checking
- Collision Handling, Transmission Deferral and Retransmission with Automatic Jam and Backoff Functions
- Error Interrupt and Status Generation
- 40 Pin DIP Package, 44 Pin PLCC
- Single 5 V± 10% Power Supply
- Standard CPU and Peripheral Interface Control Signals
- Loopback Capability for Diagnostics
- Single Phase Clock
- Inputs and Outputs TTL Compatible

Description

The SEEQ Ethernet Data Link Controller (EDLC) is designed to support Data Link Layer (layer 2) of the Ethernet specification for Local Area Networks (LAN). The system interface is optimized for ease of connection to commonly available DMA Controllers and specifically for BURST MODE OPERATION. The 8003 interfaces directly to the 8023A and 8020 Manchester Code Converters (MCC™) to complete the station resident Ethernet functions. The protocol used is Carrier Sense, Multiple Access with Collision Detection (CSMA/CD). The 8003 EDLC chip is a single VLSI device which replaces approximately 60 MSI and SSI devices. It is designed to greatly simplify the development of Ethernet communication in computer based systems. The 8003 provides an economic solution for the construction of an Ethernet node, providing high speed data communication at 10 Megabits/second and sees applications in terminals, workstations, personal computers, small business systems, and large computer systems, in both the office and industrial environment. The 8003 EDLC chip has a universal system interface compatible with almost any microprocessor, microcomputer, or system bus, allowing the system designer to make the price/performance tradeoffs for each application. The transmit and receive sections of the EDLC chip are independent

Functional Block Diagram



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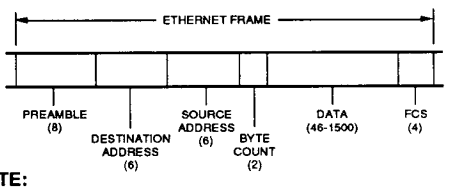
and can operate simultaneously to allow reception of a transmitted frame for use in loopback diagnostics modes.

Functional Description

Frame Format

On an Ethernet communication network, information is transmitted and received in packets or frames. An Ethernet frame consists of a preamble, two address fields, a byte-count field, a data field and a frame check sequence (FCS). Each field has a specific format which is described in detail below. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes exclusive of the preamble. The Ethernet frame format is shown below.



NOTE:
Field length in bytes in parentheses.

Preamble: *The preamble is a 64-bit field consisting of 62 alternating "1"s and "0"s followed by a "11" End-of-Preamble indicator.*

Destination Address: *The Destination Address is a 6-byte field containing either a specific Station Address, a Broadcast Address, or a Multicast Address to which this frame is directed.*

Source Address: *The Source Address is a 6-byte field containing the specific Station Address from which this frame originated.*

Byte-Count Field: *The Byte-Count Field consists of two bytes providing the number of valid data bytes in the Data Field, 46 to 1500. This field is uninterpreted at the Data Link Layer, and is passed through the EDLC chip to be handled at the Client Layer.*

Data Field: *The Data Field consists of 46 to 1500 bytes of information which are fully transparent in the sense that any arbitrary sequence of bytes may occur.*

Frame Check Sequence: *The Frame Check Sequence (FCS) field is a 32-bit cyclic redundancy check (CRC) value computed as a function of the Destination Address Field, Source Address Field, Type Field and Data Field. The FCS is appended to each transmitted frame, and used at reception to determine if the received frame is valid.*

Transmitting

The transmit data stream consists of the Preamble, four information fields, and the FCS which is computed in real time by the EDLC chip and automatically appended to the frame at the end of the serial data. The Preamble is also generated by the EDLC chip and transmitted immediately prior to the Destination Address. Destination Address, Source Address, Type Field and Data Field are prepared in the buffer memory prior to initiating transmission. The EDLC chip encapsulates these fields into an Ethernet

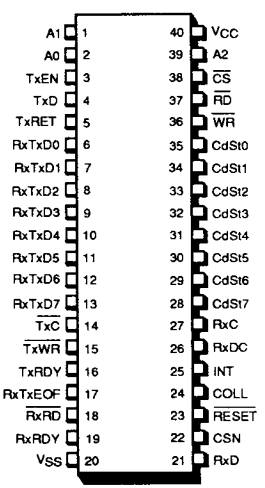


Figure 1. Dual-In-Line Top View

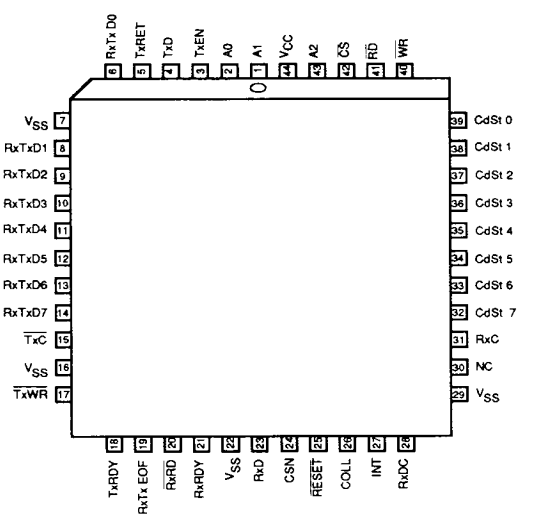


Figure 2. Plastic Leaded Chip Carrier Top view

frame by inserting a preamble prior to these information fields and appending a CRC after the information fields.

Transmission Initiation/Deferral

The Ethernet node initiates a transmission by storing the entire information content of the frame to be transmitted in an external buffer memory, and then transferring initial frame bytes to the EDLC Transmit FIFO. "Transmit-buffer to FIFO" transfers are coordinated via the $\overline{TxWR}$ and TxRDY handshake interface, i.e., bytes are written to the FIFO via $\overline{TxWR}$ only when TxRDY is HIGH. Actual transmission of the data onto the network will only occur if the network has not been busy for the minimum defer time (9.6 µs) and any Backoff time requirements have been satisfied. When transmission begins, the EDLC chip activates the transmit enable (TxEN) line concurrently with the transmission of the first bit of the Preamble and keeps it active for the duration of the transmission.

Collision

When concurrent transmissions from two or more Ethernet nodes occur (collision), the EDLC chip halts the transmission of the data bytes in the Transmit FIFO and transmits a Jam pattern consisting of 55555555 hex. At the end of the Jam transmission, the EDLC chip issues a TxRET signal to the CPU and begins the Backoff wait period.

To reinitiate transmission, the initial bytes of the frame information fields must be reloaded into the EDLC Transmit FIFO. The TxRET is used to indicate to the buffer manager the need for frame reinitialization. The reloading of the Transmit FIFO may be done prior to the Backoff interval elapsing, so that no additional delay need be incurred to retransmission.

Scheduling of retransmission is determined by a controlled randomization process called Truncated Binary Exponential Backoff. The EDLC chip waits a random interval between 0 and 2^K slot times (51.2 µs per slot time) before attempting retransmission, where "K" is the current transmission attempt number (not to exceed 10).

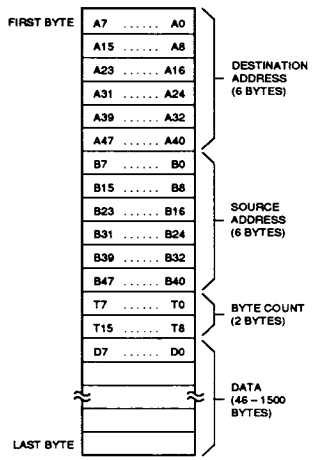


Figure 3. Typical Frame Buffer Format for Byte-Organized Memory

When 16 consecutive attempts have been made at transmission and all have been terminated due to collision, the EDLC Transmit Control sets an error status bit and issues an interrupt to the CPU if enabled.

Terminating Transmission

Transmission Terminates under the following conditions:

Normal: *The frame has been transmitted successfully without contention. Loading of the last data byte into the Transmit FIFO is signaled to the EDLC chip by activation of the RxTxEOF signal concurrently with the last byte of data loaded into the Transmit FIFO. This line acts as a*

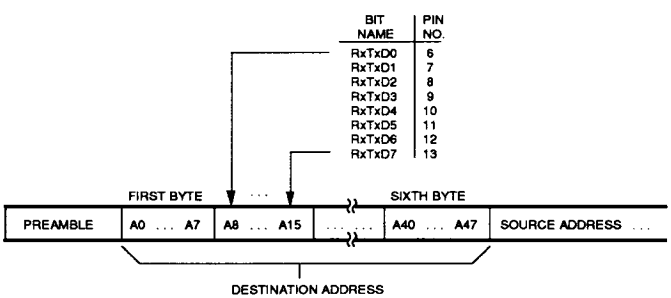


Figure 4. Bit Serialization/Deserialization

ninth bit in the Transmit FIFO. When this last byte is serialized, the CRC is appended and transmitted concluding frame transmission. The Transmission Successful bit of the Transmit Status Register will be set by a normal termination.

Collision: Transmission attempted by two or more Ethernet nodes. The Jam sequence is transmitted, the Collision status bit is set, the TxRET signal is generated, and the Backoff interval begun.

Underflow: Transmit data is not ready when needed for transmission. Once transmission has begun, the EDLC chip on average requires one transmit byte every 800 ns in order to avoid Transmit FIFO underflow (starvation). If this condition occurs, the EDLC chip terminates the transmission, issues a TxRET signal, and sets the Transmit-Underflow status bit.

16 Transmission Attempts: If a Collision occurs for the sixteenth consecutive time, the 16-Transmission-Attempts status bit is set, the Collision status bit is set, the TxRET signal is generated, and the Backoff interval begun. The counter that keeps track of the number of collisions is modulo 16 and therefore rolls over on the 17th collision.

At the completion of every transmission or retransmission, new status information is loaded into the Transmit Status Register. Dependent upon the bits enabled in the Transmit Command Register, an interrupt will be generated for the just completed transmission. In both collision and underflow the TxRET signal is activated.

Receiving

The EDLC chip is continuously monitoring the network. When activity is recognized via the Carrier Sense (CSN) line going active, the EDLC chip synchronizes itself to the incoming data stream during the Preamble, and then examines the destination address field of the frame. Depending on the Address Match Mode specified, the EDLC chip will either recognize the frame as being addressed to itself in a general or specific fashion or abort the frame reception.

Preamble Processing

The EDLC chip recognizes activity on the Ethernet via the Carrier Sense line. The Preamble is normally 64 bits (8 bytes) long. The Preamble consists of a sequence of 62 alternating "1"s and "0"s followed by "11", with the frame information fields immediately following. In order for the decoder phase-lock to occur, the EDLC chip waits 16 bit times before looking for the "11" end of preamble indicator. If the EDLC chip receives a "00" before receiving the "11" in the Preamble, an error condition has occurred. The frame is not received, and the EDLC chip begins monitoring the network for a carrier again.

Address Matching

Ethernet addresses consist of two 6-byte fields. The first bit of the address signifies whether it is a Station Address or a Multicast/Broadcast Address.

First Bit	Address
0	Station Address (Physical)
1	Multicast/Broadcast Address (logical)

Address matching occurs as follows:

Station Address: All destination address bytes must match the corresponding bytes found in the Station Address Register.

Multicast Address: If the first bit of the incoming address is a 1 and the EDLC chip is programmed to accept Multicast Addresses, the frame is received.

Broadcast Address: The six incoming destination address bytes must all be FF hex. If the EDLC chip is programmed to accept broadcast or Multicast Addresses the frame will be received.

If the incoming frame is addressed to the EDLC chip specifically (Destination Address matches the contents of the Station Address Register), or is of general or group interest (Broadcast or Multicast Address), the EDLC chip will pass the frame exclusive of Preamble and FCS to the CPU buffer and indicate any error conditions at the end of the frame. If, however, the address does not match, as soon as the mismatch is recognized the EDLC chip will terminate reception and issue an RxDC.

The EDLC chip may be programmed via the Match Mode bits of the Receive Command Register to ignore all frames (Disable Receiver), accept all frames (Promiscuous mode), accept frames with the proper Station Address or the Broadcast Address (Station/Broadcast), or accept all frames with the proper Station Address, the Broadcast Address, or all Multicast Addresses (Station/Broadcast/Multicast).

Terminating Reception

Reception is terminated when either of the following conditions occur:

Carrier Sense Inactive: Indicates that traffic is no longer present on the Ethernet cable.

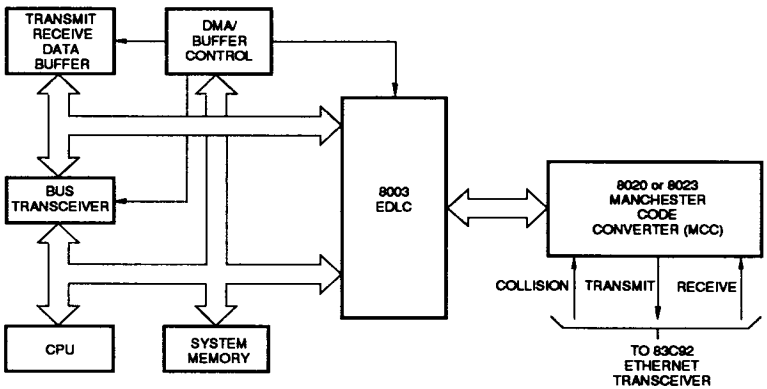


Figure 5. Typical Ethernet Node Configuration

Overflow: *The host node for some reason is not able to empty the Receive FIFO as rapidly as it is filled, and an error occurs as frame data is lost. On average the Receive FIFO must be serviced every 800 ns to avoid this condition.*

Frame Reception Conditions

Upon terminating reception, the EDLC chip will determine the status of the received frame and conditionally load it into the Receive Status Register. An interrupt will be issued if the appropriate conditions as specified in the Receive Command Register are present. The EDLC chip may report the following conditions at the end of frame reception:

Overflow: *The EDLC internal Receive FIFO overflows.*

Dribble Error: *Carrier Sense did not go inactive on a receive data byte boundary.*

CRC Error: *The 32-bit CRC transmitted with the frame does not match that calculated upon reception.*

Short Frame: *A frame containing less than 64 bytes of information was received (including FCS).*

Good Frame: *A frame is received that does not have a CRC error, Shortframe or Overflow Condition.*

System Interface

The EDLC chip system interface consists of two independent busses and respective control signals. Data is read and written over the Receive/Transmit Data Bus RxTxD (0-7). These transfers are controlled by the TxRDY and $\overline{TxWR}$ signals for transmitted data and RxRDY and $\overline{RxRD}$ for received data. All Commands and Station Addresses are written, and all status read over a separate Command/Status Bus CdSt (0-7). These transfers are controlled by the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ and A0-A2 signals. The EDLC chip's command and status registers may be accessed at any time. However, it is recommended that writing to the command register be done only during interframe gaps.

With the exception of the two Match Mode bits in the Receive Command Register, all bits in both command registers are interrupt enable bits. Changing the interrupt enable bits during frame transmission does not affect the frame integrity. Asynchronous error events, however, e.g., overflow, underflow, etc., may cause chip operation to vary, if their corresponding enable bits are being altered at the same time.

Reading the status registers may also occur at any time during transmission or reception.

Internal Register Addressing

Register Address				Register Description	
	A2	A1	A0	Read	Write
0	0	0	0	—	Station Addr 0
1	0	0	1	—	Station Addr 1
2	0	1	0	—	Station Addr 2
3	0	1	1	—	Station Addr 3
4	1	0	0	—	Station Addr 4
5	1	0	1	—	Station Addr 5
6	1	1	0	Rx Status	Rx Command
7	1	1	1	Tx Status	Tx Command

Status Registers are read only registers. Command and Station Address registers are write only registers. Access to these registers is via the CPU interface: Control signals $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and the Command/Status Data Bus CdSt (0-7).

Station Address Register

The Station Address Register is 6 bytes in length. The contents may be written in any order, with bit "0" of byte "0" corresponding to the first bit received in the data stream, and indicating whether the address is physical or logical. Bit 7 of station address byte 5 is compared to the last bit of the received destination address. The Station Address should be programmed prior to enabling the receiver.

Transmit Command Register

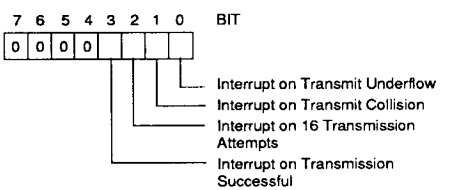
The Transmit Command Register is an interrupt mask register, which provides for control of the conditions allowed to generate transmit interrupts. Each of the four least significant bits of the register may be individually set or cleared. When set, the occurrence of the associated condition will cause an interrupt to be generated. The four specific conditions for which interrupts may be generated are:

- *Underflow*
- *Collision*
- *16 Collisions*
- *Transmission Successful*

The interrupt signal INT will be set when one or more of the specified transmission termination conditions occurs and the associated command bit has been set. The interrupt signal INT will be cleared when the Transmit Status Register is read.

All bits of the Transmit Command Register are cleared upon chip reset.

Transmit Command Register Format



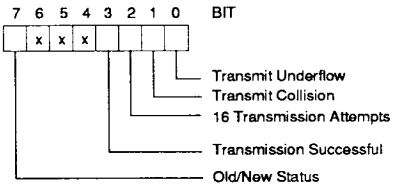
Transmission Successful is set only on the successful transmission or retransmission of a frame.

Transmit Status Register

The Transmit Status Register is loaded at the conclusion of each frame transmission or retransmission attempt. It provides for the reporting of both the normal and error termination conditions of each transmission.

The OLD/NEW status bit is set each time the Transmit Status Register is read, and reset each time new status is loaded into the Transmit Status Register. The OLD/NEW status bit is SET, and all other bits CLEARED upon chip reset.

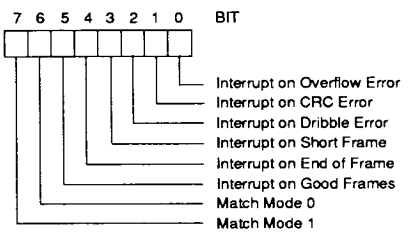
Transmit Status Register Format



Receive Command Register

The Receive Command Register has two primary functions, it specifies the Address Match Mode, and it specifies Frames-of Interest. i.e. frames whose arrival must be communicated to the CPU via interrupts and status register updates. Frames-of-Interest are frames whose status must be saved for inspection, even at the expense of losing subsequent frames.

Receive Command Register Format



Bits 0-5 specify Interrupt and Frame-of-Interest when set. Bit 4, End of Frame, specifies any type of frame except overflow.

Match Mode Definition

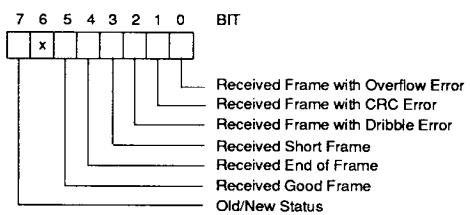
	Match Mode 1	Match Mode 0	Function
0	0	0	Receiver Disable
1	0	1	Receive All Frames
2	1	0	Receive Station or Broadcast Frames
3	1	1	Receive Station, Broadcast/Multicast Frames

Changing the receive Match Mode bits during frame reception may change chip operation and give unpredictable results.

Interrupt Enable and Frames-of-Interest
Bits 0-5 when set specify interrupt generation on occurrence of the corresponding frame reception condition. They also specify the corresponding types of frames to be Frames-of-Interest for use by the Receive Status Register to control status loading.

Receive Status Register
The Receive Status Register is normally loaded with the status of each received frame when the frame has been received or frame reception has been terminated due to an error condition. In addition, this register contains the Old/New Status bit which is set when the Receive Status Register is read or the chip is reset, and cleared only when status is loaded for a Frame-of-Interest (as defined by bits 0-5 of the Receive Command Register). All other bits are cleared upon chip reset.

Receive Status Register Format



The Old/New Status bit write-protects the Receive Status Register while it contains unread status for a Frame-of-Interest. When this bit is zero, the register is write-protected. The Old/New Status bit is cleared whenever the status of a new Frame-of-Interest is loaded into the Receive Status Register and is set after that status is read. When zero, it indicates "new status for a Frame-of-Interest".

Thus the status of any frame received following the reception of a Frame-of-Interest will not be loaded into the Receive Status Register unless the previous status has been read. If any following frame is received before the status of the previous Frame-of-Interest has been read, the new status will not be loaded, the Receive Discard (RxDC) signal will be issued and the Receive FIFO will be cleared.

With this one exception caused by a write-protect condition, the status of each frame is always loaded into the Receive Status Register on completion of reception.

Any frame received will cause an interrupt to be generated if the corresponding Interrupt Enable bit is set. This interrupt is reset upon reading the Receive Status Register.

These conditions ensure that a maximum number of good frames are received and retained.

Pin Description

The EDLC chip has four groups of interface signals:
- *Power Supply*
- *Data Buffer*
- *Encoder/Decoder*
- *Command/Status*

Power Supply

V_{cc} .....+5V
V_{ss} .....Ground

Encoder/Decoder Interface

$\overline{TxC}$ Transmit Clock (Input): *10 MHz, 50% duty cycle transmit clock used to synchronize the transmit data from the EDLC chip to the encoder. This clock runs continuously, and is asynchronous to RxC.*

TxD Transmit Data (Output): *Serial Data output to the encoder. Active HIGH.*

TxEN Transmit Enable (Output): *This signal is used to activate the encoder. It becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. Active HIGH and cleared by Reset.*

RxC Receive Data (Input): *10 MHz, 50% duty cycle nominal. The receive clock is used to synchronize incoming data to the EDLC chip from the decoder. This clock runs continuously, and is asynchronous to $\overline{TxC}$.*

RxD Receive Data (Input): *Serial input data to the EDLC chip from the decoder. Active HIGH.*

CSN Carrier Sense (Input): *Indicates traffic on the coaxial cable to the EDLC chip. Becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. Active HIGH.*

COLL Collision (Input): *Indicates transmission contention of the Ethernet cable. the Collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.*

Data Buffer Interface

RxTxD (0-7) Receive/Transmit Data Bus (I/O): *Carries Receive/Transmit data byte from/to the EDLC chip Receive/Transmit FIFOs.*

RxTxEOF Receive/Transmit End of Frame (I/O): *Indicates last byte of data on the Receive/Transmit Data Bus. Effectively a ninth bit in the FIFOs with identical timing to RxTxD (0-7). Active HIGH.*

RxRDY Receive Ready (Output): *Indicates that at least one byte of received data is available in the Receive FIFO. This signal will remain active high as long as one byte of data remains in the Receive FIFO. When this condition no longer exists, RxRDY will be deasserted with respect to the leading edge of the $\overline{RxRD}$ strobe that removes the last byte of data from the Receive FIFO. $\overline{RxRD}$ should not be activated if RxRDY is low. Active HIGH and cleared by Reset.*

$\overline{RxRD}$ Receive Read Strobe (Input): *Enables transfer of received data from the EDLC Receive FIFO to the RxTxD Bus. Data is valid from the EDLC Receive FIFO at the RxTxD pins on the rising edge of this signal. This signal should not be activated unless RxRdy is high. Active LOW.*

RxDC Receive Discard (Output): *Asserted when one of the following conditions occurs, and the associated Interrupt Enable bit in the Receive Command Register is reset. (1) Receive FIFO overflow. (2) CRC Error. (3) Short Frame Error. (4) Receive frame address nonmatch or (5) current frame status lost because previous status was not read. RxDC does not activate on errors when the associated Interrupt Enable bit is set. In this case, EOF will be generated instead when the Receive FIFO is read out. This allows reception of frames with errors. RxDC acts internally to clear the Receive FIFO.*

TxRDY Transmit Ready (Output): *Indicates that the Transmit FIFO has space available for at least one data byte. This signal will remain active high as long as one byte of space exists for transmitted data to be written into. When this condition no longer exists, TxRDY will be deasserted with respect to the leading edge of the $\overline{TxWR}$ strobe that fills the Transmit FIFO. TxRDY is forced inactive during Reset, and when TxRET is active. Active HIGH. Goes high after Reset.*

$\overline{TxWR}$ Transmit Write (Input): *Synchronizes data transfer from the RxTxD Bus to the Transmit FIFO. Data is written to the FIFO on the rising edge of this signal. This signal should not be active unless TxRDY is high. Active LOW.*

TxRet Transmit Retransmit (Output): *Asserted whenever either transmit underflow or transmit collision conditions occur. It is nominally 800 ns in width. Active HIGH. Asserted by Reset. TxRET clears the internal Transmit FIFO.*

Command/Status Interface

CdSt (0-7) Command/Status Data Bus (I/O): *These lines carry commands and status as well as station address initialization information between the EDLC chip and CPU. These lines are nominally high impedance until activated by $\overline{CS}$ and $\overline{RD}$ being simultaneously active.*

A0-A2 Address (0-2) (Input): *Address lines to select the proper EDLC internal registers for reading or writing.*

$\overline{CS}$ Chip Select (Input): *Chip Select input, must be active in conjunction with $\overline{RD}$ or $\overline{WR}$ to successfully access the EDLC internal registers. Active LOW.*

$\overline{RD}$ Read (Input): *Enables reading of the EDLC internal registers in conjunction with $\overline{CS}$. Data from the internal registers is enabled via the falling edge of $\overline{RD}$ and is valid on the rising edge of the signal. Active LOW.*

$\overline{WR}$ Write (Input): *Enables writing of the EDLC internal registers in conjunction with $\overline{CS}$. Write data on the Cdst (0-7) data lines must be set up relative to the rising edge of the signal. Active LOW.*

INT Interrupt (Output): *Enabled as outlined above by a variety of transmit and receive conditions. Remains active until the status register containing the reason for the interrupt is read. Active HIGH.*

$\overline{RESET}$ (Input): *Initializes control logic, clears command registers, clears the Transmit Status Register, clears bits 0-5 of the Receive Status Register, sets the Old/New Status bit (bit 7 of the Receive Status Register), asserts RxDC and TxRET and clears the Receive and Transmit FIFOs. In addition, TxRDY is forced low during a reset. TxRDY goes high when $\overline{RESET}$ goes high, indicating the EDLC chip is ready to transmit. $\overline{RESET}$ is active LOW.*

Absolute Maximum Ratings

Ambient Temperature
Under Bias ..... –10°C to + 80°C
Storage Temperature ..... –65°C to +150°C
All Input or Output Voltages
with Respect to Ground ..... +6V to –0.3V
Package Maximum Power Dissipation ..... 1.5 Watts

Operating Conditions

Ambient Temperature Range ..... 0°C to 70°C
V_{CC} Power Supply ..... 4.50 V to 5.50 V

DC Characteristics T_A = 0° C to 70°C, V_{CC} = 5 V to 5%

Symbol	Parameter	Limits[1]			Units	Condition
		Min.	Typ.	Max.		
I_{IN}	Input Leakage Current			10	µA	V_{IN} = 0.45 V to 5.25 V
I_O	Output Leakage Current			10	µA	V_{OUT} = 0.45 V to 5.25 V
I_{CC}	V_{CC} Current		150	200	mA	
V_{CH}	Clock Input High Voltage	3.5		6	V	
V_{CL}	Clock Input Low Voltage			0.8	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH1}	Input High Voltage	2.0		6	V	Except $\overline{TxWR}$ and $\overline{RxRD}$
V_{IH2}	Input High Voltage	3.0		6	V	$\overline{TxWR}$ and $\overline{RxRD}$
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400 µA

NOTE:
1. Typical values are for T_A = 25°C and nominal supply voltages.

AC Test Conditions

Output Load: 1 Schottky TTL Gate + CL = 100 pF
(All pins except TxEN, TxD)
TxEN, TxD Load: 1 Schottky TTL Gate + CL = 35 pF
Input Pulse Level:0.4 V to 2.4 V
Timing Reference Level:1.5 V

Capacitance[6] T_A = 25°C, F_C = 1 MHz

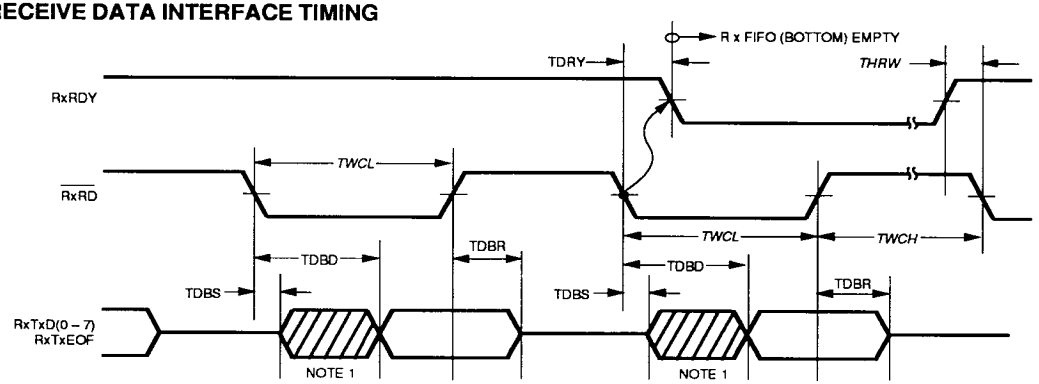
Symbol	Parameter	Maximum	Condition
C_{IN}	Input Capacitance	15 pF	V_{IN} = 0 V
$C_{I/O}$	I/O Capacitance	15 pF	$V_{I/O}$ = 0 V

AC Characteristics T_A = 0° C to 70°C, V_{CC} = 5 V ± 5%

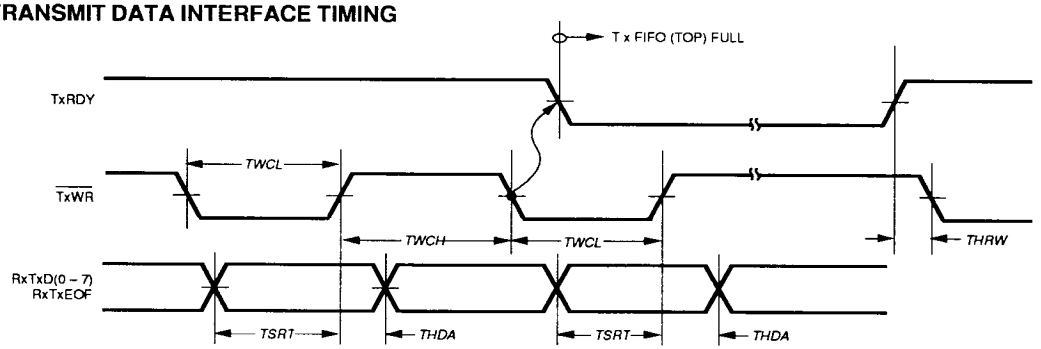
Symbol[5]	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units (ns)	Condition
DATA AND COMMAND/STATUS INTERFACE TIMING						
TDBD	RxTx/CdSt Bus Data Delay			150	ns	
TDBR	RxTx/CdSt Bus Release Delay	10			ns	
TDBS	RxTx/CdSt Bus Siezure Delay	10		150	ns	
TDRY	RxRDY/TxRDY Clear Delay			100	ns	
THAR	$A_{0-2}/\overline{CS}$ Hold	10			ns	
THDA	RxTx/CdSt Bus Hold	0			ns	
THRW	$\overline{RxRD}/\overline{TxWR}$ Hold	0			ns	
TSAR	$A_{0-2}/\overline{CS}$ Setup	0			ns	
TSCS	CdSt Bus Setup	90			ns	
TSRT	RxTx Bus Setup	90			ns	
TWCH	$\overline{RxRD}/\overline{TxWR}/\overline{RD}/\overline{WR}$ High Width	100			ns	
TWCL	$\overline{RxRD}/\overline{TWR}/\overline{RD}/\overline{WR}$ Low Width	200		10,000	ns	
SERIAL TRANSMIT AND RECEIVE INTEFACE TIMING						
TDDC	RxDC Set Delay	800			ns	NOTE 1
TDIC	INT Clear Delay			150	ns	
TDRE	TxRET Set Delay	2400		3400	ns	NOTE 3
TDRI	Receive INT Delay	1000			ns	NOTE 2
TDTD	TxD/TxEN Delay	20		60	ns	Cl = 35 pF
TDTI	Transmit INT Delay	1200			ns	NOTE 4
THRD	RxD Hold	20			ns	
TPCK	RxC/$\overline{TxC}$ Clock Period	95		1000	ns	
TSRD	RxD Setup	30			ns	
TWDC	RxDC High Width	600			ns	
TWRC	RxC High/Low Width	45			ns	
TWRE	TxRET High Width	600			ns	
TWRS	$\overline{RESET}$ Low Width	10,000			ns	
TWTC	$\overline{TxC}$ High/Low Width	45			ns	
TWCO	COLL Width	50			ns	

NOTES:
1. For frame reception with Shortframe or CRC Error. If frame reception is terminated due to Overflow, RxDC will be issued within 1.2 µs of Overflow. If frame reception is terminated due to non-match of address, RxDC wil be issued within 2.4 µs of the receipt of the last address bit.
2. Normal frame reception without Overflow. If frame reception is terminated due to Overflow, INT will be issued within 1.2µ of Overflow.
3. For TxRET caused by Collision or 16 Collision condition. If transmission is terminated due to UnderflowTxRET will be issued within 1.2 µs of the Underflow.
4. For INT caused by Collision or 16 Collision condition. If caused by Underflow, INT will be issued within 1.2 µs. If caused by normal termination, INT will be issued within 200 ns of TxEN going LOW.
5. Italics indicate input requirement, non-italics indicate output timing.
6 Characterized. Not tested.

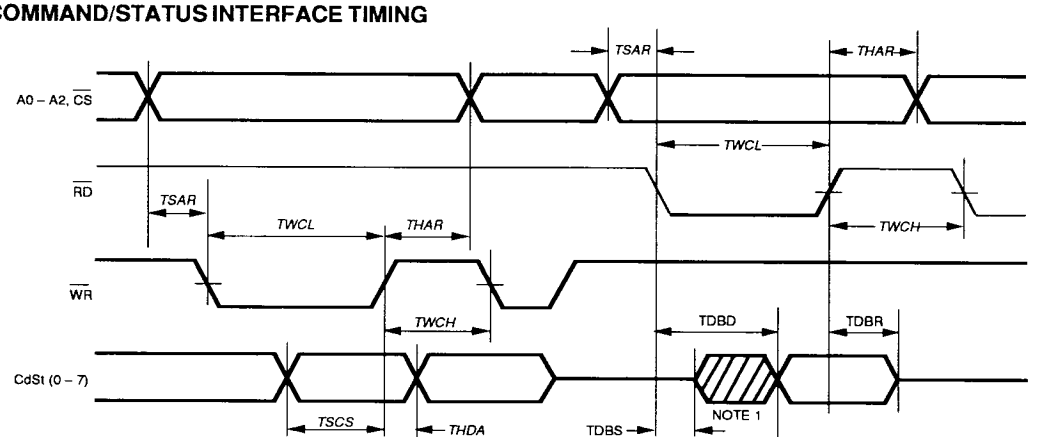
RECEIVE DATA INTERFACE TIMING



TRANSMIT DATA INTERFACE TIMING

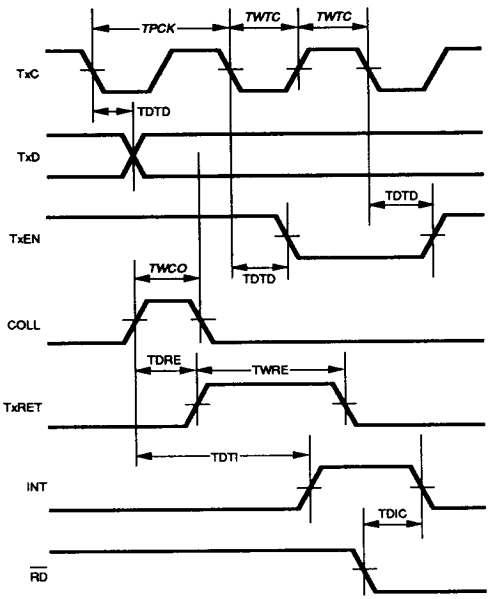


COMMAND/STATUS INTERFACE TIMING

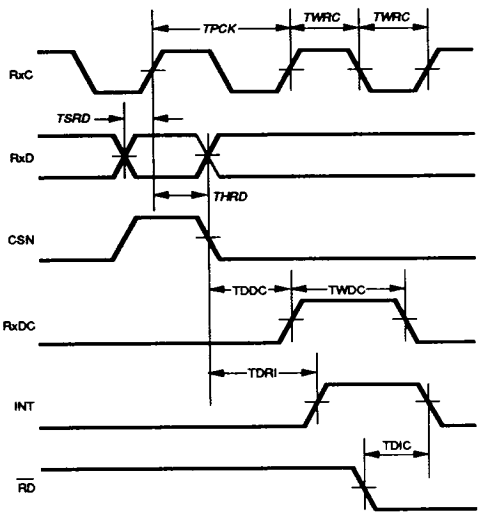


NOTE 1: Bus is driven at this time. However, no valid information present.

SERIAL TRANSMIT INTERFACE TIMING



SERIAL RECEIVE INTERFACE TIMING



Ordering Information