DDX® Multichannel Digital Audio Processor

FEATURES

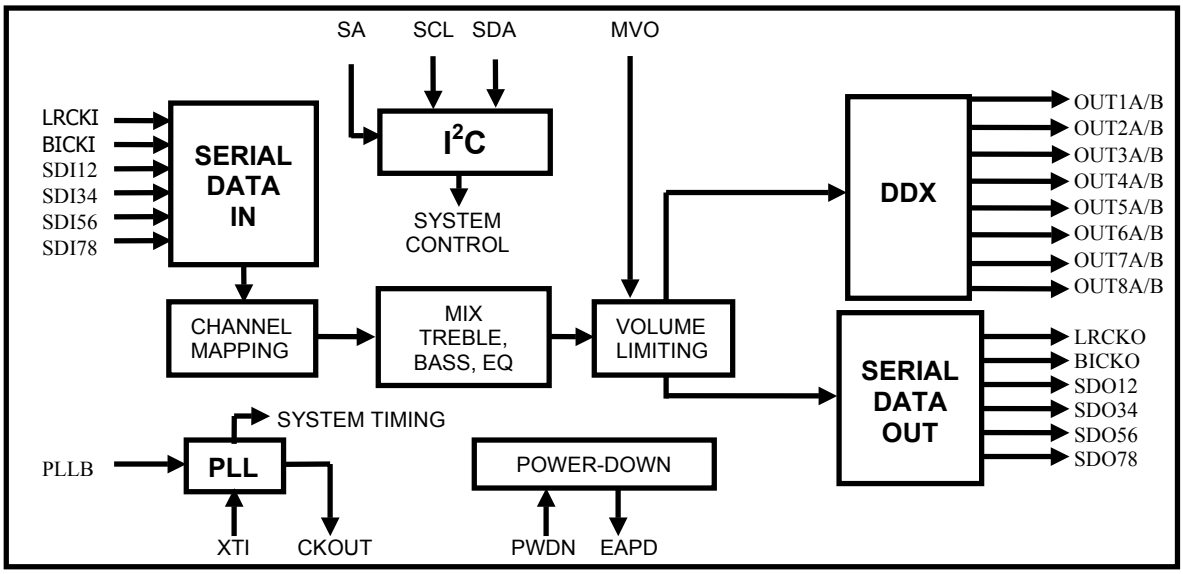
- 8 Channel, 24-Bit DDX® Processing
- I²C Control Bus
- 8 Channel Multi-format Serial Input/Output Interface
  - 32kHz - 192kHz Input Sample Rates
- Digital Gain/Attenuation +24dB to –100dB in 0.5dB steps
- Automatic/Selectable Channel Mute
- Complete Channel Mapping
- Adjacent Channel Mixing Capability
- Bass and Treble Control
- User Programmable 28-bit Parametric Filters
  - 5 Biquads in 8 Channel Mode
  - 10 Biquads in 4 Channel Mode
  - 20 Biquads in 2 Channel Mode
- Selectable High-Pass Filter
- Bass Management Function
- Variable Digital Limiter Function
- Dynamic Range Compression
- Selectable De-emphasis
- AM Interference Reduction Mode
- Companion evaluation board and development software

1.0 GENERAL DESCRIPTION

The DDX-8000 Controller includes eight channels of DDX® processing and a complete set of digital audio preamplifier functions. When combined with DDX power devices it provides a high-quality, high-efficiency, digital audio amplification solution for multi-channel audio applications such as surround sound amplifiers. The DDX-8000 may also be used as a stand-alone digital audio processor offering a low cost alternative to a DSP based solution.

The DDX-8000 includes four serial audio input and output data interfaces that can be configured for many different formats, including the popular I²S format. The design's 24-bit audio processing core includes volume control, digital filtering, bass management, gain compression/limiting and PCM and DDX® outputs. The design includes five user-programmable biquad filters per channel, as well as bass, treble and DC blocking. Each internal processing channel can receive any input channel, allowing flexibility including the ability to perform active digital crossover for powered loudspeaker systems. This high quality conversion from PCM audio to DDX's patented tri-state PWM switching waveform provides over 100dB SNR and dynamic range when used with the DDX-2060 or the DDX-2100 and over 120dB SNR and dynamic range at the digital output of the DDX-8000 processor.

Figure 1 – Block Diagram



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1.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}_3.3	3.3V I/O Power Supply	-0.5 to 4	V
V_{DD}_2.5	2.5V Logic Power Supply	-0.5 to 3.3	V
$V_{i2.5}$	Voltage on 2.5V inputs (pins 1, 16, 17)	-0.5 to V_{DD}_2.5+0.5	V
$V_{i3.3}$	Voltage on 3.3V inputs (pin 20)	-0.5 to V_{DD}_3.3+0.5	V
$V_{o3.3}$	Voltage on 3.3V outputs (pins 18,25,29-34, 38-43,47-51,55-58,62,63)	-0.5 to V_{DD}_3.3+0.5	V
V_{i5}	Voltage on 5V tolerant inputs (pins 6-11,15, 18,19,64)	-0.5 to 5.5 -0.8 to 6.3 (note 1)	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_a	Ambient operating temperature	-20 to +85	°C
T_j	Operating Junction Temperature	-20 to +125	°C

Note 1: -0.8V undershoots and 6.3V overshoots allowed for 4ns maximum.

1.2 THERMAL DATA

Symbol	Parameter	Value	Unit
$R\theta_{j-a}$	Thermal resistance Junction to Ambient	85	°C/W

1.3 RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}_3.3	I/O Power Supply Voltage (note 2)	3.0 to 3.6	V
V_{DD}_2.5	Logic Power Supply Voltage (note 2)	2.3 to 2.7	V
T_a	Operating Ambient Temperature	0 to 70	°C

Note 2: The +3.3V power pins are used to supply the I/O ring. It is NOT permissible to have the +2.5V internal core powered with the +3.3V I/O ring unpowered, when there is activity on the I/O. It is permissible to have the +3.3V I/O ring powered with the +2.5V internal core unpowered, but signals will not be received or transmitted. If both supplies are unpowered and there is external activity, the ESD protection circuit in the ring will clamp external signals at 2.8V maximum by sinking current provided by the interface.

1.4 ELECTRICAL CHARACTERISTICS (V_{DD}_3.3= 3.3±0.3V, V_{DD}_2.5= 2.5±0.2V, T_a=0 to 70°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ESD}	Electrostatic Protection	Leakage< 1uA (note 3)	1000			V

Note 3: Human Body Model. Pins 34, 43, 47 withstand only 500V.

1.4.1 DC ELECTRICAL CHARACTERISTICS: 3.3V CAPABLE BUFFERS(pins 18,20,25,29-34, 38-43,47-51,55-58,62,63)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILhyst}	Low Level Threshold	Input Falling	0.8		1.35	V
V_{IHhyst}	High Level Threshold	Input Rising	1.3		2.0	V
V_{hyst}	Schmitt Trigger Hysteresis		0.3		0.8	V
V_{ol}	Low Level Output	Iol = 100uA			0.2	V
V_{oh}	High Level Output	Ioh = -100uA	Vdd_3.3 -0.2			V
V_{OL}	Low Level Output	Iol = 2mA (note 4)			0.4	V
V_{OH}	High Level Output	Ioh = -2mA (note 4)	2.4			V

Note 4: Pin 20 Iol=4mA, Ioh= -4mA

1.4.2 DC ELECTRICAL CHARACTERISTICS: 2.5V CMOS INPUT BUFFERS(pins 1, 16, 17)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Threshold	Input Falling		0.5* VDD_2.5		V
V_{IH}	High Level Threshold	Input Rising		0.5* VDD_2.5		V
Ipd	Pull down Current	Vi = VDD_2.5		50		uA

1.4.3 DC ELECTRICAL CHARACTERISTICS: 5V TOLERANT BUFFERS(pins 6-11,15,18,19, 64)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILhyst}	Low Level Threshold	Input Falling	0.8		1.35	V
V_{IHhyst}	High Level Threshold	Input Rising	1.3		2.0	V
V_{hyst}	Schmitt Trigger Hysteresis		0.3		0.8	V
I_{IL}	Low Level Input Current	Vi = 0V			1	uA
$I_{IH\_3.3}$	High Level Input Current	Vi = VDD_3.3			2	uA

Note 5: RESET, Pin 15, must be held low for a minimum of 100 nsec.

1.4.4. OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{VDD\_3.3}$	Operating Current 3.3V	All 8-channels operating		5		mA
$I_{VDD\_2.5}$	Operating Current 2.5V			60		mA
I_{VDD_PLL}	Operating Current PLL					mA
$I_{VDD\_3.3}$	PowerDown Current 3.3V	PowerDown Asserted		3.5		mA
$I_{VDD\_2.5}$	PowerDown Current 2.5V			0.7		mA
I_{VDD_PLL}	PowerDown Current PLL					mA

1.5 PIN DESCRIPTION

Table 1: Audio Inputs

Pin #	Pin Name	I/O	Description	Type
10	LRCKI	I	I^2S Left/Right Clock	5V Tolerant TTL Input
11	BICKI	I	I^2S Bit Clock	5V Tolerant TTL Input
9	SDI12	I	I^2S Data Channels 1 & 2	5V Tolerant TTL Input
8	SDI34	I	I^2S Data Channels 3 & 4	5V Tolerant TTL Input
7	SDI56	I	I^2S Data Channels 5 & 6	5V Tolerant TTL Input
6	SDI78	I	I^2S Data Channels 7 & 8	5V Tolerant TTL Input

Table 2: Clocking

Pin #	Pin Name	I/O	Description	Type
16	PLLB	I	Phase Locked Loop Bypass	2.5V CMOS Input with Pull-Down
20	XTI	I	Clock Input	3.3V Capable TTL Schmitt Trigger Input
21	PLLF	I	PLL Filter	Analog Pad
25	CKOUT	O	Clock Output	3.3V Capable TTL 4mA Output

Table 3: Control/Miscellaneous

Pin #	Pin Name	I/O	Description	Type
17	SA	I	I^2C Select Address	2.5V CMOS Input with Pull-Down
18	SDA	I/O	I^2C Serial Data	5V Tolerant Input / 3.3V Capable 2mA Output
19	SCL	I	I^2C Serial Clock	5V Tolerant TTL Schmitt Trigger Input
1	MVO	I	Master Volume Override	2.5V CMOS Input with Pull-Down
15	RESET	I	Global Reset Input	5V Tolerant TTL Schmitt Trigger Input
64	PWDN	I	Device PowerDown	5V Tolerant TTL Schmitt Trigger Input
51	EAPD	O	External Amp Power Down	3.3V Capable TTL 2mA Output

Table 4: Audio Outputs

Pin #	Pin Name	I/O	Description	Type
50	OUT1A	O	PWM Channel 1 Output A	3.3V Capable TTL 2mA Output
49	OUT1B	O	PWM Channel 1 Output B	3.3V Capable TTL 2mA Output
48	OUT2A	O	PWM Channel 2 Output A	3.3V Capable TTL 2mA Output
47	OUT2B	O	PWM Channel 2 Output B	3.3V Capable TTL 2mA Output
43	OUT3A	O	PWM Channel 3 Output A	3.3V Capable TTL 2mA Output
42	OUT3B	O	PWM Channel 3 Output B	3.3V Capable TTL 2mA Output
41	OUT4A	O	PWM Channel 4 Output A	3.3V Capable TTL 2mA Output
40	OUT4B	O	PWM Channel 4 Output B	3.3V Capable TTL 2mA Output
39	OUT5A	O	PWM Channel 5 Output A	3.3V Capable TTL 2mA Output
38	OUT5B	O	PWM Channel 5 Output B	3.3V Capable TTL 2mA Output
34	OUT6A	O	PWM Channel 6 Output A	3.3V Capable TTL 2mA Output
33	OUT6B	O	PWM Channel 6 Output B	3.3V Capable TTL 2mA Output
32	OUT7A	O	PWM Channel 7 Output A	3.3V Capable TTL 2mA Output
31	OUT7B	O	PWM Channel 7 Output B	3.3V Capable TTL 2mA Output
30	OUT8A	O	PWM Channel 8 Output A	3.3V Capable TTL 2mA Output
29	OUT8B	O	PWM Channel 8 Output B	3.3V Capable TTL 2mA Output
56	LRCKO	O	I^2S Left/Right Clock Output	3.3V Capable TTL 2mA Output
55	BICKO	O	I^2S Serial Clock Output	3.3V Capable TTL 2mA Output
57	SDO12	O	I^2S Data Channels 1&2 Output	3.3V Capable TTL 2mA Output
58	SDO34	O	I^2S Data Channels 3&4 Output	3.3V Capable TTL 2mA Output
62	SDO56	O	I^2S Data Channels 5&6 Output	3.3V Capable TTL 2mA Output
63	SDO78	O	I^2S Data Channels 7&8 Output	3.3V Capable TTL 2mA Output

Table 5: Power Supplies

Pin #	Pin Name	I/O	Description	Type
22	VDD_PLL		PLL Supply	2.5V PLL Power Supply Voltage
23	GND_PLL		PLL Ground	PLL Ground
3,12,24,28, 35,44,52,59	VDD_3.3		3.3V I/O Supply	3.3V Digital Power Supply Voltage
2,4,13,27, 36,45,53,60	GND		Ground	Digital Ground
5,14,26,37, 46,54,61	VDD_2.5		2.5V Logic Supply	2.5V Digital Power Supply Voltage

1.5.1 LRCKI: Left/Right Clock In (pin 10)

The Left/Right clock input is for the purpose of data word framing. The clock frequency will be at the input sample rate Fs. Refer to Figure 9.

1.5.2 BICKI: Bit Clock In (pin 11)

The serial or bit clock input is for the purpose of framing each data bit. The bit clock frequency is typically 64*Fs, for example using I^2S serial format at a 48 kHz sample rate. Refer to Figure 9.

1.5.3 SDI12 through 78: Serial Data In (pins 6-9)

PCM Serial Digital Audio data inputs consist of four left/right pairs. Six format choices are available including I^2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits. Refer to section 3.1 for more information.

1.5.4 PLLB: PLL Bypass (pin 16)

This pin is used to steer the XTI input bypassing the internal PLL circuit. With PLLB set high, the master clock applied to the XTI pin will be used as the internal master clock. It is recommended to use the internal PLL circuit leaving this pin at ground.

1.5.5 XTI: Master clock In (pin 20)

This pin is the master clock input. The master clock must be an integer multiple of the LR clock frequency. Typically, the master clock frequency is 12.288 MHz (256*Fs) for a 48kHz sample rate, which is the default at power-up. Care must be taken not to exceed an internal clock frequency of 98.304MHz; otherwise the device may not properly operate or be able to communicate. See section 4.1 for more information.

1.5.6 PLLF: PLL Filter (pin 21)

This pin connects to external filter components for PLL loop compensation. Refer to the schematic diagram Figure 18 for the recommended circuit.

1.5.7 CKOUT: Clock Out (pin 25)

CKOUT provides a divided clock output derived from the internal PLL. This output may be used as a clock source for other devices in the system. For details, refer to section 4.3.

1.5.8 I^2C (pins 17, 18, 19)

The SA (Select Address), SDA (I^2C Data) and SCL (I^2C Clock) pins operate per the I^2C specification. See Section 2 for communication details.

1.5.9 MVO: Master Volume Override (pin 1)

This pin enables the user to bypass the Volume Control on all channels. When MVO is pulled High, the Master Volume Register is set to 00h, which corresponds to its Full Scale 0dB setting. The individual Channel Volume Settings default to 30h or 0dB and therefore when MVO is set the total gain in the DDX-8000 is 0dB for every channel. This is intended for simple applications without I2C control and for testing purposes.

1.5.10 RESET (pin 15)

Driving this pin (low) sets the DDX-8000 into a reset state turning off the outputs and returning all settings to their defaults. The reset is asynchronous to the internal clock.

1.5.11 PWDN: Device Power-Down in (pin 64)

This puts the DDX-8000 into a low-power state via appropriate power-down sequence. Pulling PWDN low begins power-down sequence, a soft mute is performed on all outputs and EAPD goes low ~30ms later.

1.5.12 EAPD: External Amplifier Power-Down out (pin 51)

This output is used to control the operation of DDX® Power Devices and for Power-on and Power-off sequencing.

1.5.13 OUT1A,B through OUT8A,B: DDX PWM outputs (pins 29-50)

The PWM outputs provide the patented DDX® PWM signal to the power devices. See section 8.1.

1.5.14 BICKO and LRCKO: Bit Clock Out and LR Clock Out (pins 55, 56)

These clock signals are used to frame the I^2S output audio data. See section 8.3

1.5.15 SDO12 through 78: Serial Data Out (pins 57,58,62,63)

PCM Serial Digital Audio information is output here. Six different format choices are available including I^2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits. When configuring the device for serial data loop-thru, all that is required are connections from SDO to SDI. For example to implement up to twenty biquad filters on two channels, connect SDO12 to SDI34 … SDO56 to SDI78. See section 8.2. When not configuring for serial loop-thru, the I^2S output format specified can be different than the I^2S input format specified.

1.5.16 VDD_PLL and GND_PLL: Phase Locked Loop Power (pins 22, 23)

The phase locked loop power is applied here. This +2.5V supply must be well bypassed for noise immunity. The audio performance of the device is critically dependent upon the PLL circuit.

1.5.17 VDD_3.3: +3.3VDC (pins 3, 12, 24, 28, 35, 44, 52, 59)

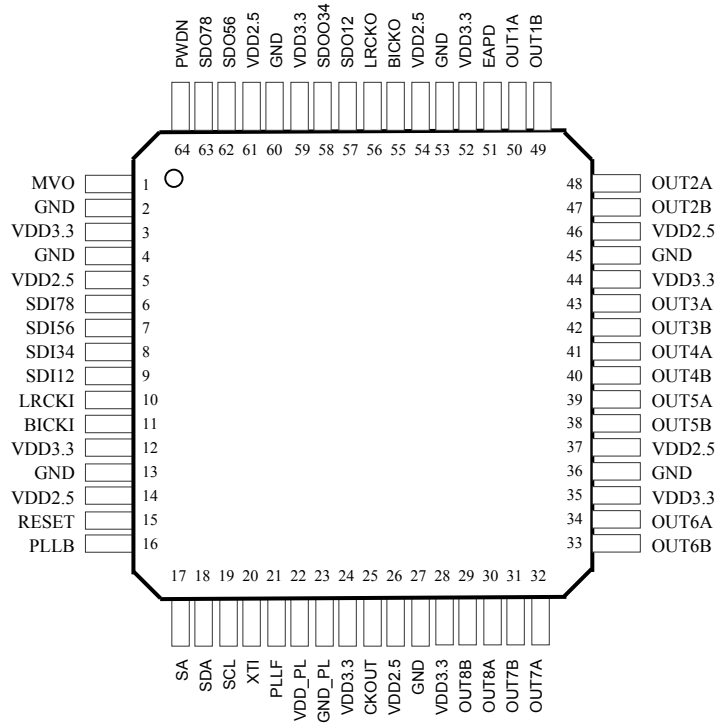
The +3.3V power pins are used to supply the I/O ring. It is NOT permissible to have the +2.5V internal core powered with the +3.3V I/O ring unpowered, when there is activity on the I/O. It is permissible to have the +3.3V I/O ring powered with the +2.5V internal core unpowered, but signals will not be received or transmitted. If both supplies are unpowered and there is external activity, the ESD protection circuit in the ring will clamp external signals at 2.8V maximum by sinking current provided by the interface.

1.5.18 GND: Digital Ground (pins 2, 4, 13, 27, 36, 45, 53, 60)

1.5.19 VDD_2.5: +2.5VDC (pins 5, 14, 26, 37, 46, 54, 61)

The +2.5V power pins are used to supply the digital logic core.

1.6. PIN CONNECTION (Top View)



1.7. AUDIO PERFORMANCE

Parameter	From DDX-2060 Output	From I2S Output
SNR (Typical)	-100dB	-124dB
Dynamic Range (Typical)	-100dB	-124dB
THD vs. Output Power	.04% (1W, 1KHz, 28V Vcc)	.0003% (-10dBFS, 1KHz)

1.7.1. Test conditions

The EB-8000 test platform was used to produce the measurements shown in the following sections. This platform was designed with the interest of testing and demonstrating the DDX-8000 device in concert with the DDX-2060 power device. See the corresponding application note for more detailed information including schematics concerning this evaluation board.

1.7.2. Performance characteristics using DDX-2060 Power Device at Vcc = 28V, 8 Ohm load

Figure 2: FFT, -60dB, 1kHz Output

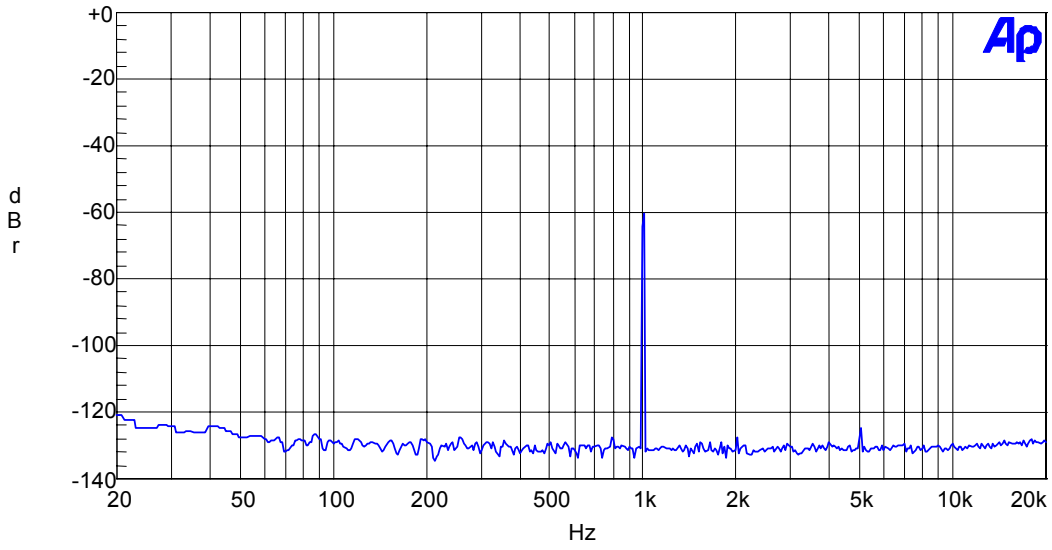


Figure 3: Inter-Modulation Distortion, 19kHz and 20kHz

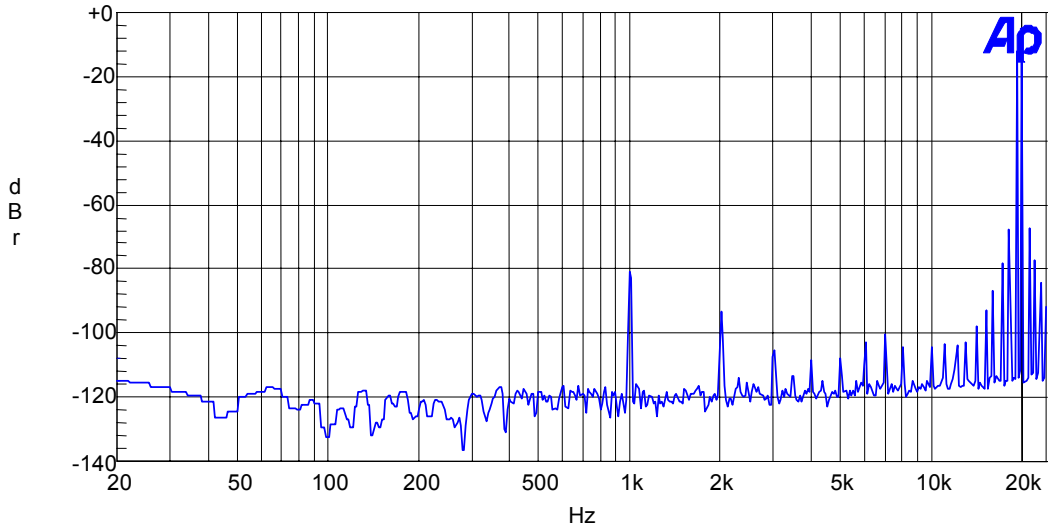
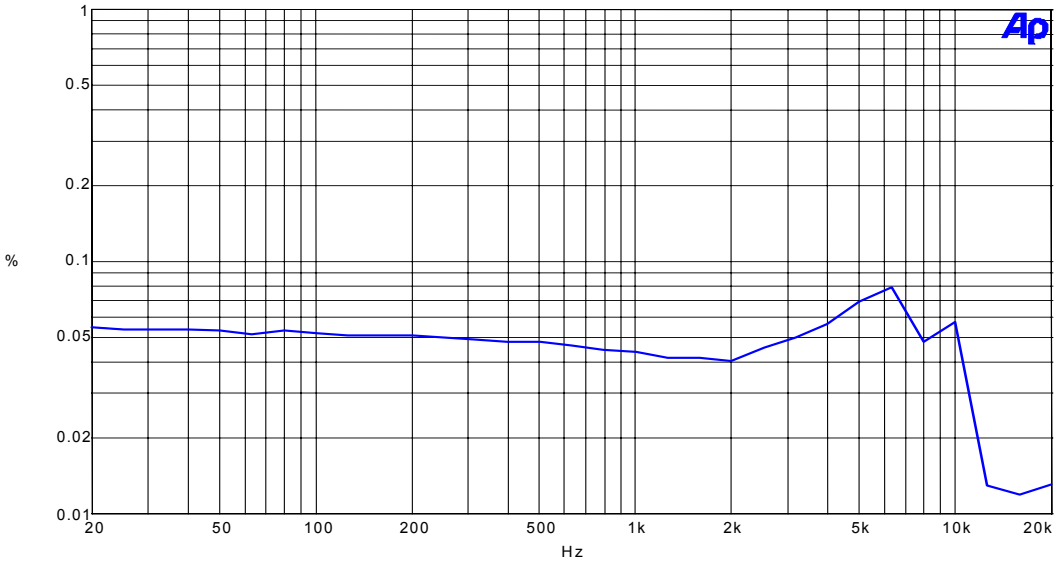


Figure 4: THD+N vs. Frequency, 1kHz, 1W



1.7.3. Measurements from I²S Output

Figure 5: FFT, -60dB, 1kHz Output

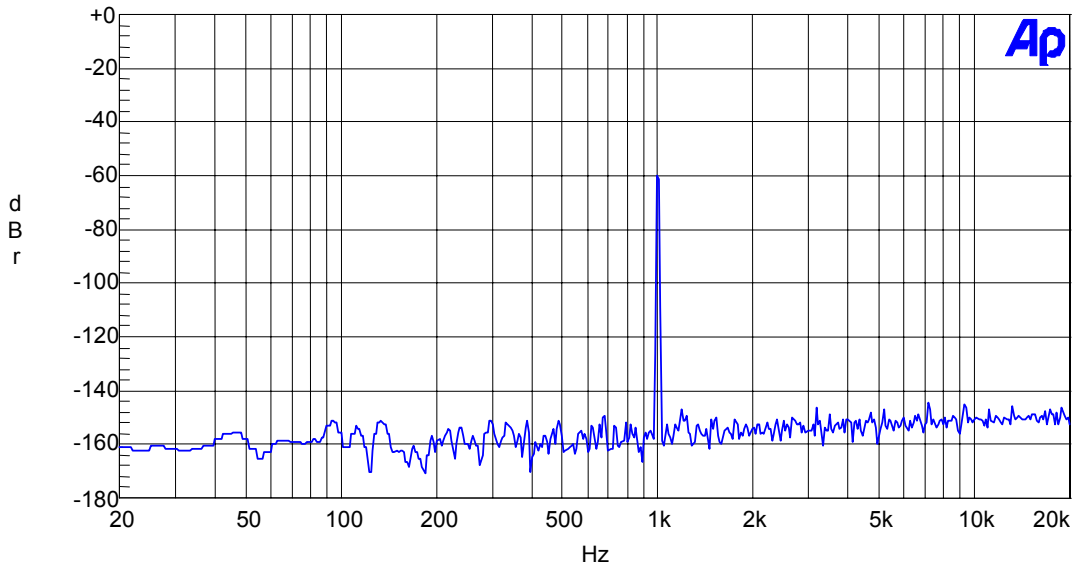
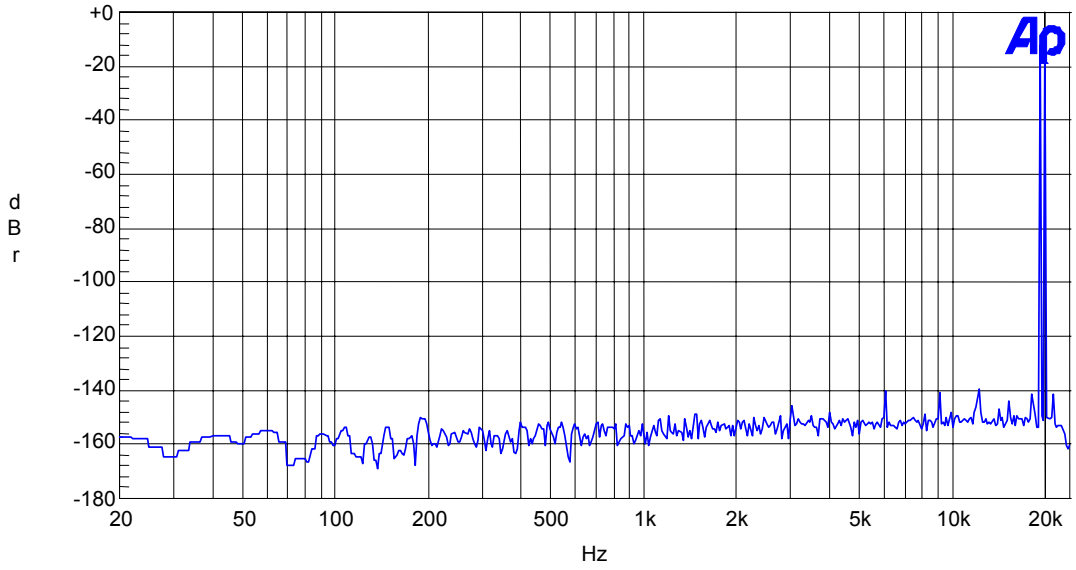


Figure 6: Inter-Modulation Distortion, 19kHz and 20kHz



1.8 How this document is organized

This document is organized into three main areas:

Section 1	Device overview information and highlights
Sections 2-9	Functional detail
Sections 10-11	Register summary and reference information

Sections 2-9 provide a conceptual approach as to how the various features in the device can be used and what the specific settings are for a given feature and their effect. In these sections, frequent references are made to the DDX-8000 registers used to control a particular feature. These references have a form consistent with the following: <Register Name> - <Register Address in hex>, <Bit Numbers within register>. For example, "Configuration Register B – 01h, Bits D4-D2". A given feature may be controlled by many different registers.

Section 10 provides a register summary to be used as a quick reference. In this section, the default value for each register and setting is noted and frequent references are made to the functional section(s) that provides the detail corresponding to the register and bit(s) in question and what other settings are available.

2. I^2C BUS SPECIFICATION

The DDX-8000 provides a number of registers that are used to control its behavior. The I^2C protocol is used to set and query these registers. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The DDX-8000 is always a slave device in all of its communications.

2.1 COMMUNICATION PROTOCOL

2.1.1 Data Transition or change

Data changes on the SDA line must only occur when the SCL clock is low. An SDA transition while the clock is high is used to identify a START or STOP condition.

2.1.2 Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

2.1.3 Stop Condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between DDX-8000 and the bus master.

2.1.4 Data Input

During the data input the DDX-8000 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL clock signal is low.

2.2 DEVICE ADDRESSING

To start communication between the master and the DDX-8000, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I^2C bus definition. In the DDX-8000 the I^2C interface has two device addresses depending on the SA pin configuration, 0x30 or 0011000x when SA = 0, and 0x32 or 0011001x when SA = 1.

The 8th bit (LSB) identifies read or write operation R/W. This bit is set to 1 in read mode and 0 for write mode. After a START condition the DDX-8000 identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

2.3 WRITE OPERATION

Following the START condition the master sends a device select code with the RW bit set to 0. The DDX-8000 acknowledges this and then the master writes the byte of internal address. After receiving the internal byte address the DDX-8000 again responds with an acknowledgement. See figure 7.

2.3.1 Byte Write

In the byte write mode the master sends one data byte, this is acknowledged by the DDX-8000. The master then terminates the transfer by generating a STOP condition.

2.3.2 Multi-byte Write

The multi-byte write modes can start from any internal address. Sequential data byte writes will be written to sequential addresses within the DDX-8000. The master generating a STOP condition terminates the transfer.

Write Mode Sequence

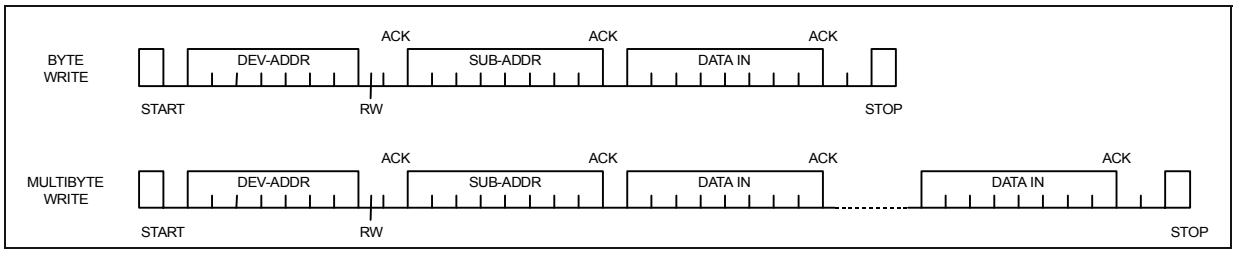


Figure 7: I²C Write Mode Sequence

Read Mode Sequence

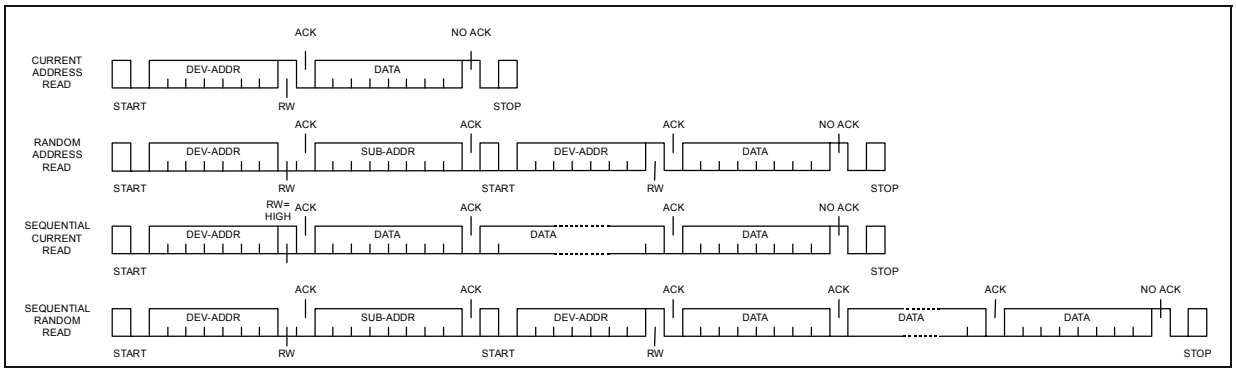


Figure 8: I²C Read Mode Sequence

3. Input Interface

3.1. Serial Data Interface

The DDX-8000 audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. DDX-8000 always acts a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI (pin 10), serial clock BICKI (pin 11), serial data 1 & 2 SDI12 (pin 9), serial data 3 & 4 SDI34 (pin 8), serial data 5 & 6 SDI56 (pin 7), and serial data 7 & 8 SDI78 (pin 6).
The SAI register (Configuration Register B – 01h, Bits D4-D2) and the SAIFB register (Configuration Register B – 01h, Bit D5) are used to specify the serial data format. The default serial data format is I^2S, MSB-First. Available formats are shown in the tables and figure that follow.

Table 6: Serial Data First Bit

SAIFB	Format
0	MSB-First
1	LSB-First

Note: Serial input and output formats (see section 8.2) are specified distinctly.

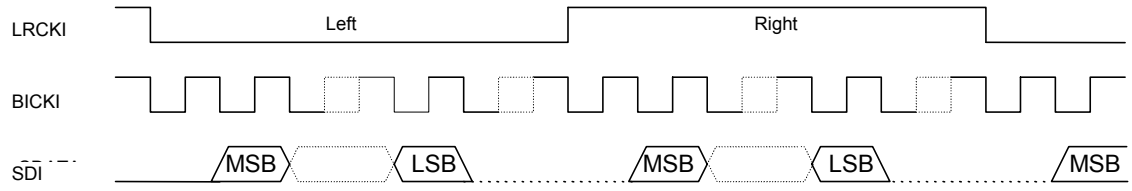
For example, SAI=010 and SAIFB=1 would specify Right-Justified 16-bit data, LSB-First.
Table 7 below lists the serial audio input formats supported by DDX-8000 as related to BICKI = 32/48/64fs, where sampling rate fs = 32/44.1/48/88.2/96/176.4/192 kHz.

Table 7: Supported Serial Audio Input Formats

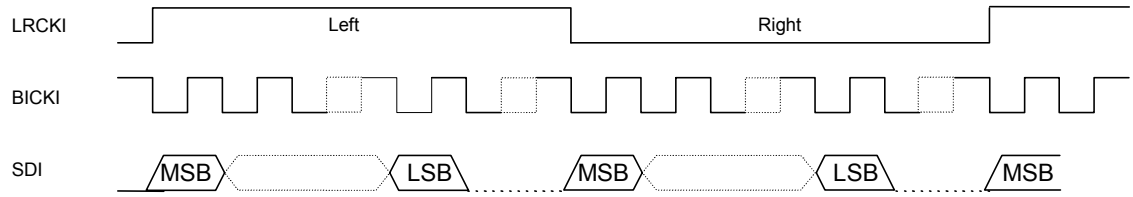
BICKI	SAI (2...0)	SAIFB	Interface Format
32fs	010	X	MSB First Right/Left-Justified 16-bit data
48fs	001	0	MSB First Left-Justified Data
		1	LSB First Left-Justified 24-bit Data
	010	X	Right-Justified 16-bit Data
	011	X	Right-Justified 18-bit Data
	100	X	Right-Justified 20-bit Data
	101	X	Right-Justified 24-bit Data
64fs	000	0	I^2S 16 to 24-bit Data
	001	0	MSB First Left-Justified Data
		1	LSB First Left-Justified 24-bit Data
	010	X	Right-Justified 16-bit Data
	011	X	Right-Justified 18-bit Data
	100	X	Right-Justified 20-bit Data
	101	X	Right-Justified 24-bit Data

Note: 'X' represents Don't Care. Shading denotes default setting of DDX-8000

SAI=000 I^2S



SAI=001 Left Justified



SAI=010 to 101 Right Justified

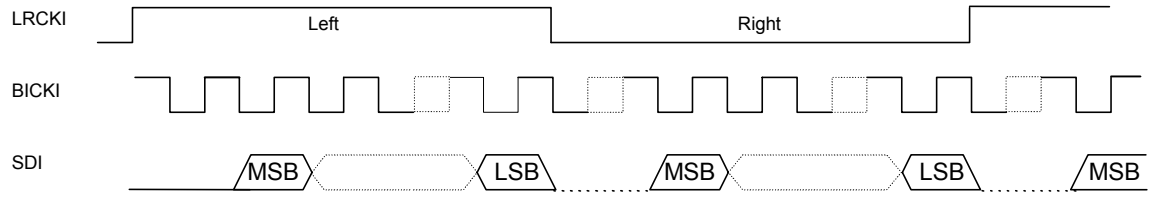


Figure 9: Audio Serial Interface Formats

3.2. Serial Input Data Timing characteristics (Fs = 32 to 192kHz)

BICKI FREQUENCY (slave mode)	12.5MHz max.
BICKI pulse width low (T0) (slave mode)	40ns min.
BICKI pulse width high (T1) (slave mode)	40ns min.
BICKI active to LRCKI edge delay (T2)	20ns min.
BICKI active to LRCKI edge delay (T3)	20ns min.
SDI valid to BICKI active setup (T4)	20ns min.
BICKI active to SDI hold time (T5)	20ns min.

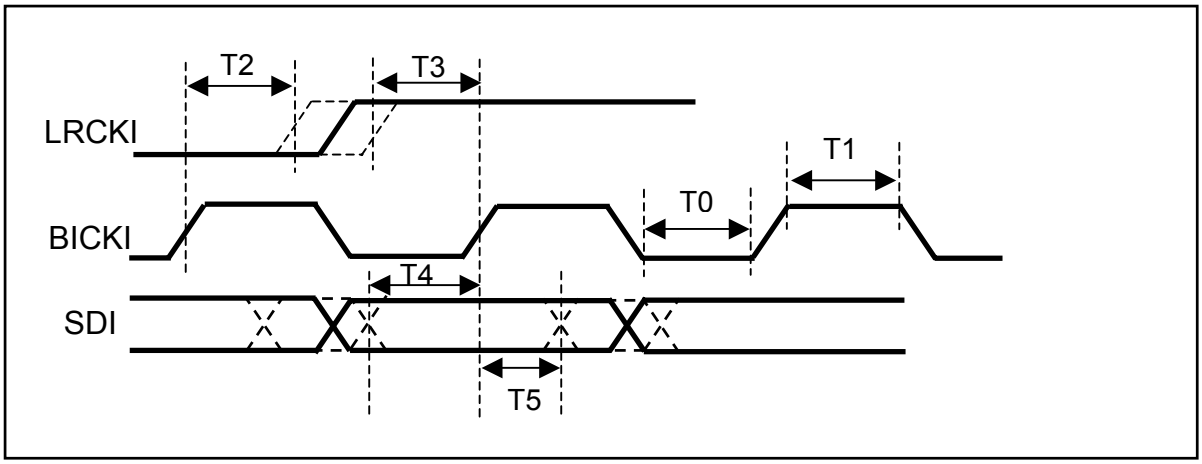


Figure 10: Serial Input Data Timing characteristics

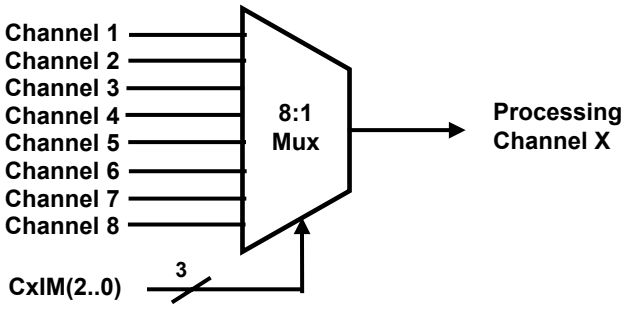
3.3. Channel Mapping

Each internal processing channel can receive data from any serial input channel using the Channel Input Mapping registers: C1IM (011h, Bits D2-D0), C2IM (011h, Bits D6-D4), C3IM (012h, Bits D2-D0), C4IM (012h, Bits D6-D4), C5IM (013h, Bits D2-D0), C6IM (013h, Bits D6-D4), C7IM (014h, Bits D2-D0), C8IM (014h, Bits D6-D4). This allows for flexibility in processing, simplifies output stage designs, and enables the ability to perform crossovers. By default, each serial input channel is mapped to its corresponding processing channel. Table 8 shows available settings for the input mapping registers.

For example, to take data for internal processing channel 6 from serial input channel 2 (SDI12 – pin 9, right channel), set the C6IM register (address 13h, bits D6, D5, D4) to 001. Now, input 2 is routed to Channel 6.

Table 8: Processing Channel Input Mapping (where x is the Processing channel)

CxIM(2..0)	Serial Input From:
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8



4. System Clocking

4.1. Input Sample Rate and Input Clock

The DDX-8000 will support a number of data input sample rates (32kHz, 44.1kHz, 48Khz, 88.2kHz, 96kHz, 176.4kHz, 192kHz) and was designed to accept a number of input clock frequencies that are integer multiples of the input sample rate (*fs*). In order to generate the internal clock from the input clock provided to the XTI pin (pin 20), a low-jitter PLL has been included in the device.

The IR register (Configuration Register A – 00h, Bits D4-D3) is used to specify the sample rate, and the MCS register (Configuration Register A – 00h, Bits D2-D0) is used to specify the input clock frequency as a multiple of the sample rate. The default is a sample rate of 48kHz and an input clock rate of 256*fs (12.288 MHz). Depending on the design, settings other than these defaults may need to be specified. Accepted settings are specified in the table that follows.

Input Sample Rate *Fs* (kHz)	**IR(1..0)**	**MCS(2..0)**				
		1xx	**011**	**010**	**001**	**000**
32,44.1,48	00	128fs	256fs	384fs	512fs	768fs
88.2,96	01	64fs	128fs	192fs	256fs	384fs
176.4,192	10	64fs	128fs	192fs	256fs	384fs
Reserved	11	NA	NA	NA	NA	NA

When the incoming sample rate changes from 44.1kHz or 48kHz to 96kHz or vice-versa, the IR bit settings must change. If the incoming master clock to the XTI pin changes, then the MCS bits must also change. Depending on the timing of this change, the mute bits may have to be set before the change occurs and unset afterwards. Care must be taken when changing the MCS bits such that the internal clock generated by the PLL does not exceed 98.304Mhz.

4.2. PLL Bypass

Using the PLLB pin (pin 16) the PLL can be bypassed. With PLLB set high, the clock source applied to XTI (pin 20) provides a direct connection to the internal system clock. When this option is selected, an external frequency as shown below should be provided to the device.

External frequency required when bypassing the PLL (differs according to sample rate):

- 65.536Mhz for 32kHz
- 90.3168Mhz for 44.1khz, 88.2kHz, and 176.4kHz
- 98.304Mhz for 48kHz, 96kHz, and 192kHz

4.3. Output Clock

The DDX-8000 can provide a clock output CKOUT (pin 25) derived from the internal PLL. The COS register (Configuration Register D – 03h, Bits D5-D4) is used to specify the frequency of this clock. The COD register (Configuration Register F – 05h, Bit D2) can be used to disable clock output on this pin. By default, clock output is enabled and the frequency is the PLL output (internal system clock) divided by 8. It is recommended that this output be disabled if not used by the system.

The available CKOUT frequencies in MHz are shown in the table that follows.

COS(1,0)	**Input Sample Rate (kHz)**		
	32	**44.1,88.2,176.4**	**48,96,192**
00	65.536	90.3168	98.304
01	16.384	22.5792	24.576
10	8.192	11.2896	12.288
11	4.096	5.6448	6.144

5. Bass Management and Scale/Mix

5.1. Bass Management

To implement bass management, the DDX-8000 provides the ability to scale and mix all channels to processing channel 6 where filters can then be applied. This allows for information from any channel to be taken from that channel and scaled to processing channel 6 and then filtered appropriately for a subwoofer application. The BME register (Configuration Register A – 00h, bit D5) is used to select this feature. By default, bass management is not selected. (Note that if both BME and MIXE are set to 1, BME – Bass Management takes precedence and would be enabled.)

When the bass management feature is selected eight 24-bit coefficients (one per channel referred to as CxBMS where x represents the channel) stored in a RAM block within the device are used to specify a scaling factor. The scale factor should be in the range of 0 (no mixing, full attenuation) to 1 (full mixing, no attenuation – 7FFFFFh). Each input channel is multiplied by its corresponding scale factor and summed. The resulting summation is then provided as the input to the filter for channel 6. The source channels (1,2,3,4,5,7,8) will pass through to their respective filters unchanged. See Figure 11.

Section 6.1.5 describes the technique for writing the scale coefficients to RAM.

5.2. Adjacent Channel Mixing

The scale and mix functionality can alternatively be used to mix adjacent channels. In this mode, odd channels will be mixed with their adjacent even channels and the result is output in place of the even processing channel where it can then be filtered. Combined with the channel-mapping feature a large number of possibilities exist for two channel mixing to provide up to four mixed channels. The MIXE register (Configuration Register E – 04h, Bit D0) is used to select this feature. (Note that in this case, BME register must be set to 0). By default, adjacent channel mixing is not selected.

The scaling coefficients are the same as those used for bass management (described above) and are used to specify the amount of scaling to the even channel, 0 (no mixing, full attenuation) to 1 (full mixing, no attenuation – 7FFFFFh). The odd channels will pass through to their respective filters unchanged. How the scaling and summing occurs and how the output is produced is shown in Figure 12 below.

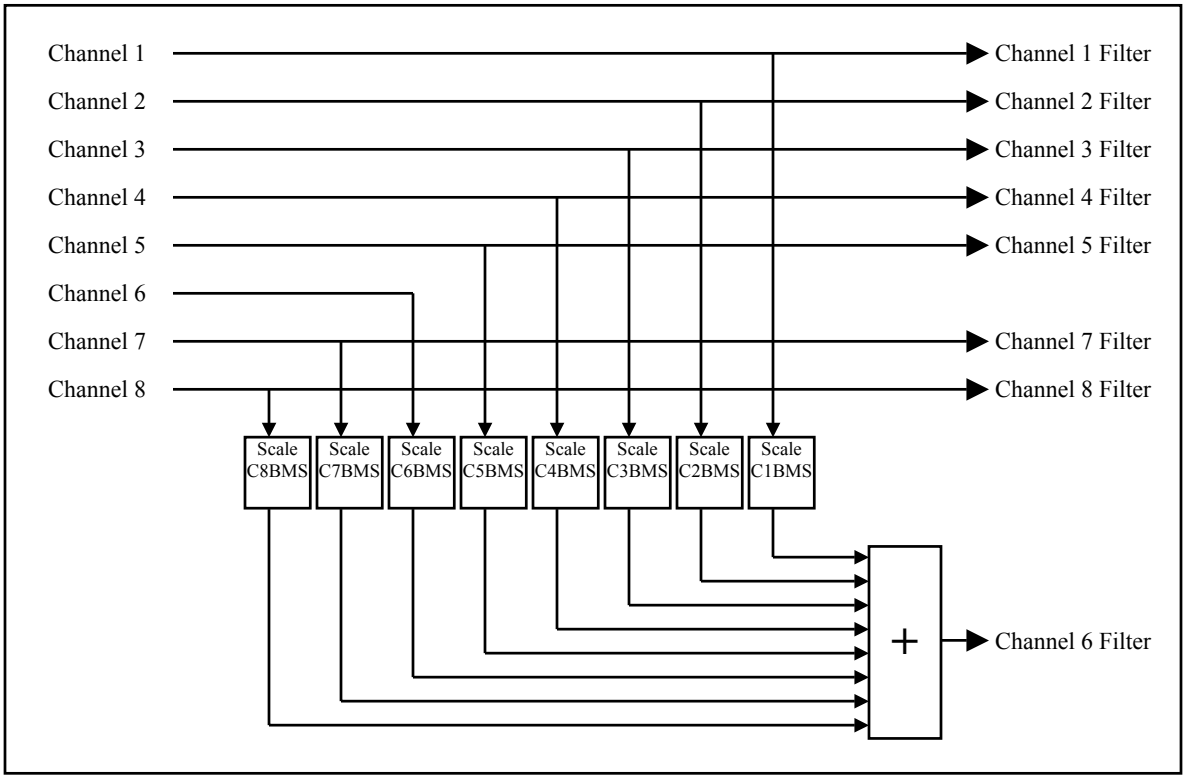


Figure 11: Bass Management (BME=1, MIXE=x)

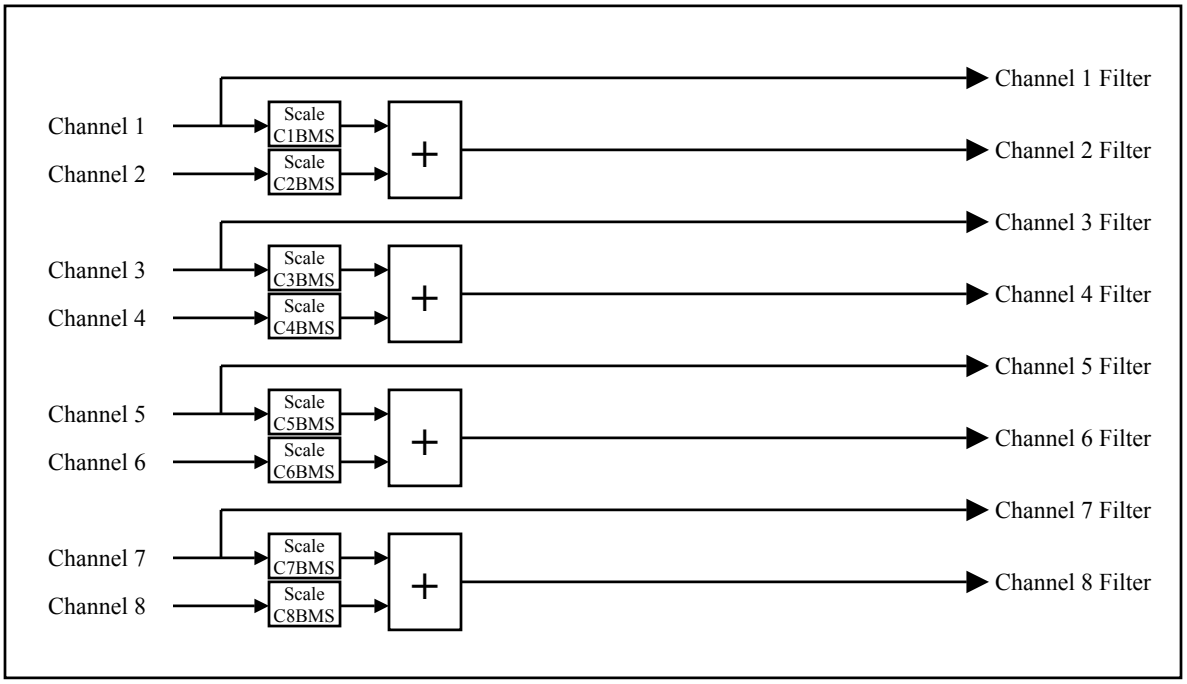


Figure 12: Adjacent Channel Mixing (BME=0, MIXE=1)

6. EQ and Tone Control

The DDX-8000 has the ability to pass each processing channel through a 5 stage cascaded 2nd order IIR filter (biquad). In addition, the device also contains bass and treble tone control adjustments. The digital audio data flow is shown in the diagram below.

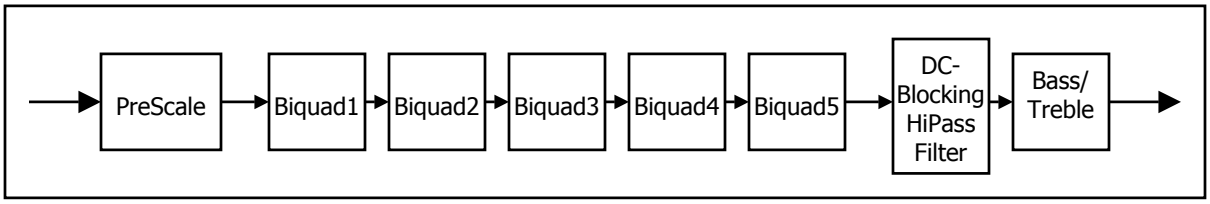


Figure 13: Data flow for single channel Biquad / Bass / Treble

6.1. Equalization

To implement equalization, the DDX-8000 provides five user-programmable 28-bit biquads per channel. The DSPB register (Configuration Register B – 01h, Bit D0) is used to bypass both pre-scale and equalization. By default, pre-scale and equalization are enabled and the default scale factors and filters cause the data to be passed through unchanged.

When equalization is enabled, five 24-bit filter coefficients for each channel for each biquad (stored in a RAM block within the device) are used to define the filter. These biquads run at 192kHz for the 48kHz, 96kHz, or 192kHz input rates and at 176.4kHz for the 44.1kHz, 88.2kHz, and 176.4kHz input rates. The sample rate the biquads run at should be considered when designing the filters. Section 6.1.6 below describes the technique for writing these coefficients to RAM.

6.1.1. Biquad Equation

The biquads use the equation that follows. This is diagrammed in figure 14 below.

$$Y[n] = 2(b_0/2)X[n] + 2(b_1/2)X[n-1] + b_2X[n-2] – 2(a_1/2)Y[n-1] – a_2Y[n-2]$$

$$= b_0X[n] + b_1X[n-1] + b_2X[n-2] – a_1Y[n-1] – a_2Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multiplies are 28-bit signed fractional multiplies, with coefficient values in the range of 800000h (-1) to 7FFFFFh (0.9999998808).

Coefficients stored in RAM are referenced in the following manner:

CxHy0 = b_2
CxHy1 = $b_0/2$
CxHy2 = $-a_2$
CxHy3 = $-a_1/2$
CxHy4 = $b_1/2$

The x represents the channel and the y the biquad number. For example C3H41 is the $b_0/2$ coefficient in the fourth biquad for channel 3

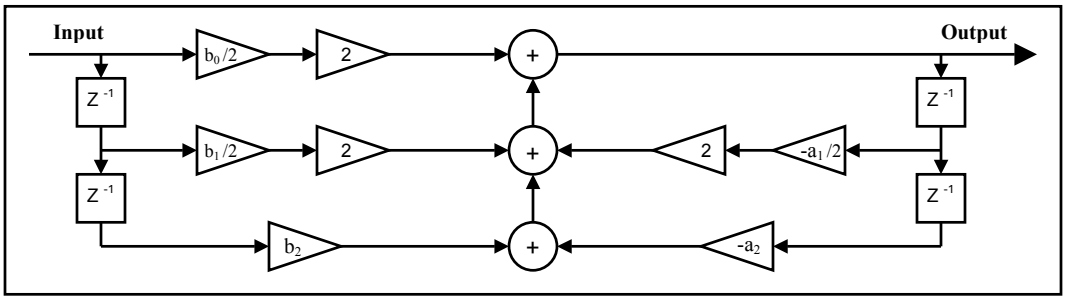


Figure 14: Biquad Filter

6.1.2. De-emphasis

The DEMP register (Configuration Register E – 04h, Bit D2) is used to control the DDX-8000 de-emphasis feature. Setting this bit will place de-emphasis on all channels. When this is used it takes the place of biquad1 on each channel and any coefficients specified for biquad1 will be ignored. By default, de-emphasis is not active. DSPB(DSP Bypass) register must be set to 0 for de-emphasis to function.

6.1.3. Pre-Scale

The Pre-Scale block which precedes the first biquad is used for attenuation when filters are designed that boost frequencies above 0dBFS. This is a single 28-bit signed multiply, with 800000h = -1 and 7FFFFFh = 0.9999998808. By default, all pre-scale factors are set to 800000h.

Note that the default pre-scale value inverts the signal phase. This should be understood when the output is taken from the I^2S output interface.

6.1.4. Reading a Coefficient Value

The following sequence of steps should be followed to read any coefficient, pre-scale, post-scale, or bass management value from RAM:

- write 8-bit address to I^2C register 1Ch
- read top 8-bits of coefficient in I^2C address 1Dh
- read middle 8-bits of coefficient in I^2C address 1Eh
- read bottom 8-bits of coefficient in I^2C address 1Fh

6.1.5. Writing a single Coefficient Value

The following sequence of steps should be followed to write any pre-scale, post-scale, or bass management value to RAM:

- write 8-bit address to I^2C register 1Ch
- write top 8-bits of coefficient in I^2C address 1Dh
- write middle 8-bits of coefficient in I^2C address 1Eh
- write bottom 8-bits of coefficient in I^2C address 1Fh
- write 1 to W1 bit in I^2C address 2Ch

6.1.6. Writing a set of Coefficient Values

Use the following sequence of to write a set of filter coefficient values to RAM. This mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side effects. When using this technique, the 8-bit starting address would specify the address of the biquad b2 coefficient (e.g. RAM address 0, 5, 10, 15, …, 50, … 195 decimal), and the DDX 8000 will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

- write 8-bit starting address to I^2C register 1Ch
- write top 8-bits of coefficient b2 in I^2C address 1Dh
- write middle 8-bits of coefficient b2 in I^2C address 1Eh
- write bottom 8-bits of coefficient b2 in I^2C address 1Fh
- write top 8-bits of coefficient b0 in I^2C address 20h
- write middle 8-bits of coefficient b0 in I^2C address 21h
- write bottom 8-bits of coefficient b0 in I^2C address 22h
- write top 8-bits of coefficient a2 in I^2C address 23h
- write middle 8-bits of coefficient a2 in I^2C address 24h
- write bottom 8-bits of coefficient a2 in I^2C address 25h
- write top 8-bits of coefficient a1 in I^2C address 26h
- write middle 8-bits of coefficient a1 in I^2C address 27h
- write bottom 8-bits of coefficient a1 in I^2C address 28h
- write top 8-bits of coefficient b1 in I^2C address 29h
- write middle 8-bits of coefficient b1 in I^2C address 2Ah
- write bottom 8-bits of coefficient b1 in I^2C address 2Bh
- write 1 to WA bit in I^2C address 2Ch

6.1.7. Coefficient/Scaling Factor Map

Table 9: RAM Block for Biquad Coefficients and Bass Management, Pre-Scale, and Post-Scale Scaling Factors

Index (Decimal)	Index (Hex)		Coefficient	Default
0	00h	Channel 1 - Biquad 1	C1H10($b_{2)}$	000000h
1	01h		C1H11(b0/2)	3FFFFFh
2	02h		C1H12(a2)	000000h
3	03h		C1H13(a1/2)	000000h
4	04h		C1H14(b1/2)	000000h
5	05h	Channel 1 - Biquad 2	C1H20	000000h
…	…	…	…	…
24	18h	Channel 1 - Biquad 5	C1H54	000000h
25	19h	Channel 2 - Biquad 1	C2H10	000000h
26	1Ah		C2H11	3FFFFFh
…	…	…	…	…
49	31h	Channel 2 - Biquad 5	C2H54	000000h
50	32h	Channel 3 - Biquad 1	C3H10	000000h
…	…	…	…	…
199	C7h	Channel 8 - Biquad 5	C8H54	000000h
200	C8h	Channel 1 - Pre-Scale	C1PS	800000h
201	C9h	Channel 2 – Pre-Scale	C2PS	800000h
202	CAh	Channel 3 – Pre-Scale	C3PS	800000h
…	…	…	…	…
207	CFh	Channel 8 –Pre-Scale	C8PS	800000h
208	D0h	Channel 1 – BassM Scale	C1BMS	000000h
209	D1h	Channel 2 – BassM Scale	C2BMS	000000h
…	…	…	…	…
215	D7h	Channel 8 – BassM Scale	C8BMS	000000h
216	D8h	Channel 1 – Post-Scale	C1PS	800000h
217	D9h	Channel 2 – Post-Scale	C2PS	800000h
…	…	…	…	…
223	DFh	Channel 8 – Post-Scale	C8PS	800000h
224	F0h	Not Used		
…	…	…	…	…
255	FFh	Not Used		

Setting the BQL register (Configuration Register D – 03h, Bit D7) to 1 will cause all channels to use the biquad coefficient values for channel 1. This option should only be used if every channel uses the same EQ settings. By default, every channel will use its own set of coefficient values for filtering.

In a similar manner, setting the PSL register (Configuration Register D – 03h, Bit D6) to 1 will cause all channels use the post-scale values for channel 1.

6.2. High Pass Filter

The DDX-8000 features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a DDX amplifier, which can cause speaker damage. This filter will not affect the 20 – 20kHz frequency response. The HPB register (Configuration Register C – 02h, Bit D7) can be set to 1 to disable this feature. By default, the AC coupling digital high-pass filter feature is enabled.

6.3. Tone Control

The DDX-8000 contains bass and treble tone control adjustments. These are selectable from +12dB to –12dB of boost or cut in 2dB steps. These are 1st order shelving filters with a corner frequency of 150Hz for bass and 3kHz for treble. Any gain introduced in the tone controls will carry through to the volume and limiting block without saturation.

The TTC register (address 1Bh, Bits D7-D4) is used to adjust the treble boost or cut. The BTC register (address 1Bh, Bits D3-D0) is used to adjust the bass boost or cut. By default a 0dB boost/cut is specified for each. The table that follows details the boost or cut corresponding to all available settings.

Table 10: Tone Control Boost/Cut

BTC(3..0)/TTC(3..0)	Boost/Cut
0000	-12dB
0001	-12dB
…	…
0111	-4dB
0110	-2dB
0111	0dB
1000	+2dB
1001	+4dB
…	…
1101	+12dB
1110	+12dB
1111	+12dB

For example, setting TTC=1001 would specify a +4dB treble boost and setting BTC=0000 would specify a –12dB bass cut.

7. Volume and Dynamics Control

7.1. Volume Control

The DDX-8000 provides individual volume registers for each channel and a master volume register that provides an offset to each channel's volume setting. The individual channel volumes are adjustable in 0.5dB steps from +24dB to –103dB. The master volume is adjustable in 0.5dB steps from 0dB to –127dB. Note that the maximum possible gain is +24dB.

In a multi-channel application, the channel volume registers should be used to set the maximum volume setting or digital gain and the volume offsets between channels. The master volume register can then be used to control the overall system volume.

Individual 8-bit channel volume registers (referenced as CxV where x is the channel number ranging from 1 to 8) are located at I^2C addresses 09h through 10h. The default channel volume setting is 0dB (30h). The 8-bit Master Volume MV register is located at I^2C address 07h, and the default setting is "hard mute" (FFh). Tables 11 and 12 below show the volume level as a function of the register values.

Table 11: Channel Volume Settings

CxV(7..0)	Volume
00000000(00h)	+24dB
00000001(01h)	+23.5dB
00000010(02h)	+23dB
…	…
00101111(2Fh)	+0.5dB
00110000(30h)	0dB
00110001(31h)	-0.5dB
…	…
11111110(FEh)	-103dB
11111111(FFh)	Hard Channel Mute

Table12: Master Volume Settings

MV(7..0)	Volume Offset from Channel Value
00000000(00h)	0dB
00000001(01h)	-0.5dB
00000010(02h)	-1dB
…	…
01001100(4Ch)	-38dB
…	…
11111110(FEh)	-127dB
11111111(FFh)	Hard Master Mute

As an example, understanding that the channel volume register is used to set the maximum volume for that channel and the master volume register provides an offset, if C5V = 0Bh or +18.5dB and MV = 21h or –16.5dB, then the total gain for channel 5 = +2dB.

By default, all changes in volume take place at digital zero-crossings as this creates the smoothest possible volume transition. The ZCE register (Configuration Register B – 01h, Bit D6) can be set to 0 to cause volume updates to occur immediately, however, it is recommended to operate in the default mode.

7.1.1 Pin-Commanded Master Volume Override

The MVO pin (pin 1) is used to bypass the Master Volume Control on all channels. When MVO is pulled High, the master volume setting used is 00h, which corresponds to its Full Scale 0dB setting. With the individual Channel Volume Settings at a default of 30h or 0dB, this results in a total gain of 0dB for every channel. This is intended for simple applications without I^2C control and for testing purposes.

7.1.2 Output Mute Control

The master mute register (address 06h, Bit D0) is used to command a mute on all channels simultaneously by setting the register to 1. The channel mute registers (referenced as CxM where x is the channel number ranging from 8 down to 1, located at I^2C address 08h, Bits D7-D0) are used to command a mute on channels individually by setting the appropriate bit to 1.

Both the Master Mute and the Channel Mutes provide a "soft mute" with the volume ramping down to mute in approximately 43ms. A "hard mute" can be obtained by commanding a value of all 1's(FFh) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel that whose total volume is less than –103dB will be muted.

7.2. Dynamics Control

In combination with the gain/volume control features noted above, the DDX-8000 also provides features for controlling the dynamic range of the sound output. The device has the ability to compress the output when a certain threshold is exceeded by an input signal (with volume/gain applied) and to apply the compression at a particular rate. Once the input signal falls below a certain threshold, a release (or uncompression) of the output will occur.

Various parameters are used to specify these thresholds and rates. The compression threshold is the level which when exceeded will cause compression to begin. The release threshold is the level at which uncompression will begin. Compression will occur according to the compression rate setting and uncompression will occur according to the release rate setting. In general, default settings are optimized for musicality such that it should not be necessary to change defaults except for tailored applications.

Dynamics control is implemented in the device by a "limiter". The purpose of the limiter is to automatically reduce the dynamic range of the input signal to prevent the outputs from clipping (anti-clipping mode) or to actively reduce the dynamic range for a better listening environment (Dynamic Range Compression - DRC).

7.2.1 Dual Independent Limiters

The DDX-8000 features two independent limiters (limiter 1 and limiter 2). Having two limiters provides several advantages:

- A phenomenon known as "pumping" occurs when musical content with large amounts of low frequency information is run through one compressor. The mids and highs seem to vary in amplitude or "pump" to the low frequency beat. This phenomenon can be avoided by having two limiters such that the low frequency information is processed on a separate limiter than the rest of the source (for example associating channel 6 with limiter 1 and all other channels with limiter 2).
- Distortion is less noticeable in the lower frequency band than in the mid to high band. With two limiters, separate limiter parameters allows for the threshold to be set higher for the limiter associated with the channel that has the lower frequency content.

Each channel can be mapped to either limiter or not mapped. Non-mapped channels will not use a limiter and will clip when a 0dBFS output is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then, if needed, adjust the gain of the mapped channels in unison.

The 2-bit Channel Limiter Select registers (CxLS where x is the channel number, located at I^2C addresses 15h and 16h) are used to define the mapping of each channel to a limiter. By default, all channels have limiting disabled. The following table shows the settings used to associate a channel with either limiter 1 or limiter 2.

Table 13: Channel Limiter Selection
(where x indicates the channel number)

CxLS(1,0)	Channel Limiter Mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2
11	Reserved. Don't use this setting.

All channels mapped to limiter 1 are affected by the compression and release rates and thresholds specified for limiter 1. Similarly, all channels mapped to limiter 2 are affected by the compression and release rates and thresholds specified for limiter 2.

7.2.2 Compression and Release Rates

The 4-bit limiter attack rate registers (L1A and L2A, located a I2C addresses 17h and 19h, bits D3-D0 respectively) are used to specify the compression rate. By default, the compression rate for each limiter is 0.4512 dB/ms. Available compression rates are shown in table 14.

The 4-bit limiter release rate registers (L1R and L2R, located a I2C addresses 17h and 19h, bits D7-D4 respectively) are used to specify the release rate. By default, the release rate for each limiter is 0.0147 dB/ms. Available release rates are shown in table 15.

Table 14: Limiter Compression Rates (where x indicates the limiter number)

LxA(3..0)	Compression Rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	
1111	0.0451	Slow

Table 15: Limiter Release Rates (where x indicates the limiter number)

LxR(3..0)	Release Rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	
1111	0.0104	Slow

Note: Shaded areas show the default settings.

The compression and release settings apply the same way whether in Anti-Clipping or Dynamic Range Compression mode.

7.2.3 Anti-Clipping Mode

This mode provides a way of avoiding clipping of the audio signal which when it occurs can introduce a great deal of harmonic distortion and sounds very rough and harsh. By default, the limiters operate in this mode.

The DRC register (Configuration Register B – 01h, Bit D7) specifies anti-clipping mode when set to 0. In this mode compression and release threshold values are constant and dependent on the volume (gain/attenuation) settings applied to the input signal. See figure 15.

A number of compression threshold setting scenarios exist:

- Set to 0dB: Prevent any clipping from taking place. This is the default setting.
- Higher than 0dB: Allow a limited amount of clipping to take place. % THD may increase.
- Below 0dB: Limit the maximum overall output.

Since gain can be added digitally within the DDX-8000 (see section 7.1, Volume Control) it is possible to exceed 0dB Full-Scale. When this occurs, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the compression threshold is exceeded is determined by the compression rate setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The 4-bit limiter attack threshold registers (L1AT and L2AT, located a I2C addresses 18h and 1Ah, bits D7-D4 respectively) are used to specify the compression threshold. By default, the compression threshold for each limiter is 0dB relative to Full-Scale (FS). Available compression thresholds are shown in table 16.

The 4-bit limiter release threshold registers (L1RT and L2RT, located a I2C addresses 18h and 1Ah, bits D3-D0 respectively) are used to specify the release threshold. By default, the release threshold for each limiter is -6dB relative to Full-Scale (FS). Available release thresholds are shown in table 17.

Table 16: Limiter Compression Threshold (where x indicates the limiter number)

LxAT(3..0)	AC(dB relative to FS)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 17: Limiter Release Threshold (where x indicates the limiter number)

LxRT(3..0)	AC(dB relative to FS)
0000	–∞
0001	-23dB
0010	-16.9dB
0011	-13.4dB
0100	-10.9dB
0101	-9.0dB
0110	-7.4dB
0111	-6.0dB
1000	-4.9dB
1001	-3.8dB
1010	-2.9dB
1011	-2.1dB
1100	-1.3dB
1101	-0.65dB
1110	0dB
1111	+0.6dB

Note: Shaded areas show the default settings.

Note that the release threshold value can be used to set what is effectively a minimum dynamic range. This is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound "lifeless".

7.2.4 Dynamic Range Compression Mode

Dynamic Range Compression (DRC) mode provides a useful solution in the following situations:

- If a user wishes to listen at low volume levels, simply reducing the volume would cause the quietest passages to become inaudible. In this mode, materials can be played at moderate levels without missing any of the audio content.
- If the audio content contains periods of louder than average data (e.g. TV commercials have a greater than average level than standard TV content), this mode can be used to help limit the louder than average signal content to the desired level. This can be thought of as a "Nighttime Listening" Mode.

The DRC register (Configuration Register B – 01h, Bit D7) specifies dynamic range compression (DRC) mode when set to 1. In this mode compression and release threshold values vary with the volume settings allowing for limiting to occur independent of the gain/attenuation but dependent on the input signal. See figure 16.

In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold. In essence, these settings are used to specify the difference between the loudest and softest sounds in dB. See tables 18 and 19.

Table 18: Limiter Compression Threshold (where x indicates the limiter number)

LxAT(3..0)	DRC(dB relative to Volume)
0000	-22
0001	-20
0010	-18
0011	-16
0100	-14
0101	-12
0110	-10
0111	-8
1000	-7
1001	-6
1010	-5
1011	-4
1100	-3
1101	-2
1110	-1
1111	0

Table 19: Limiter Release Threshold (where x indicates the limiter number)

LxRT(3..0)	DRC(db relative to Volume + LxAT)
0000	∞
0001	-33dB
0010	-26.9dB
0011	-23.4dB
0100	-20.9dB
0101	-19.0dB
0110	-17.4dB
0111	-16.0dB
1000	-14.9dB
1001	-13.8dB
1010	-12.9dB
1011	-12.1dB
1100	-11.3dB
1101	-10.65dB
1110	-10dB
1111	-9.4dBdB

Note: Shaded areas show the default settings.

7.3. Volume and Dynamics Control Bypass

By default, the volume and dynamics controls are enabled. The VOLEN register (Configuration Register E – 04h, Bit D1) can be set to 0 to cause the volume and dynamics control mechanisms to be bypassed.

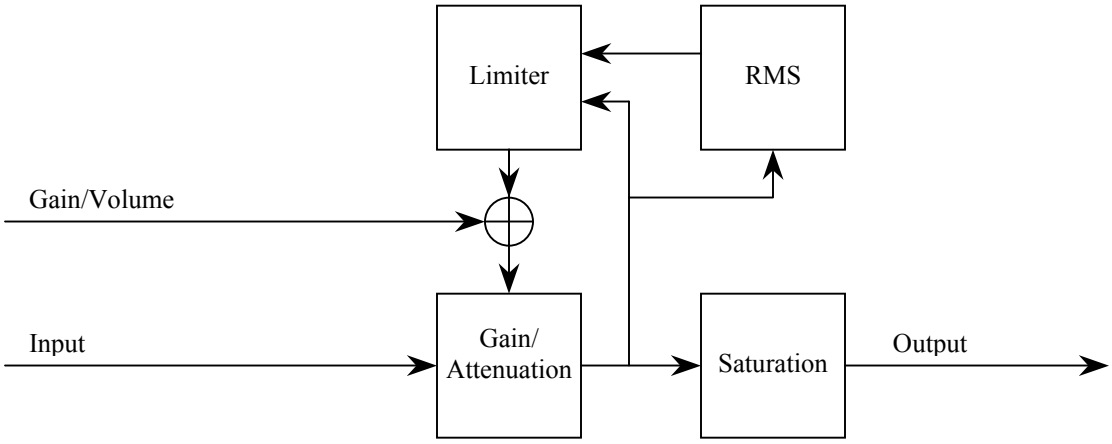


Figure 15: Limiter Conceptual Flow Diagram: Anti-Clipping Mode

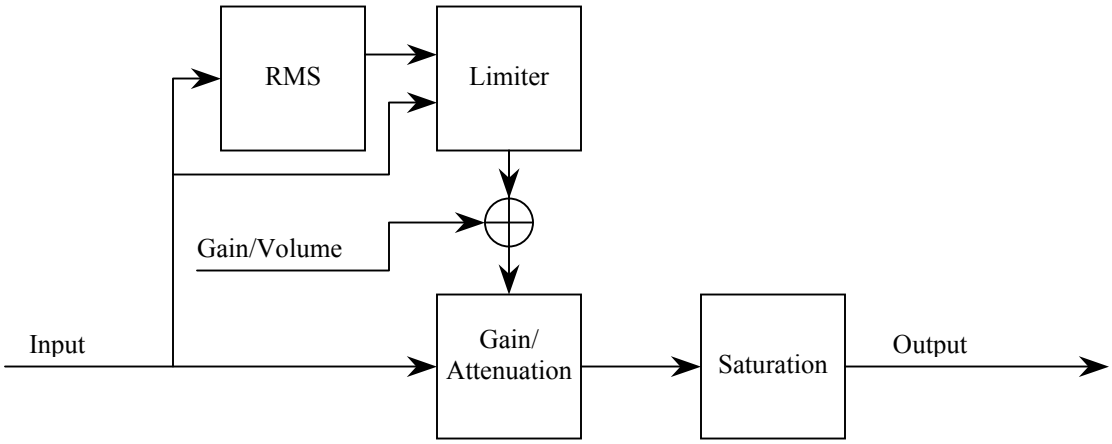


Figure 16: Limiter Conceptual Flow Diagram: Dynamic Range Compression Mode

8. Output Interface

8.1. PWM Output

The DDX-8000 provides PWM output to drive a DDX Power device. The PWM output for eight channels is provided using 16 output pins: OUT1A/B through OUT8A/B. (See table 4 for pin numbers.) The PWMD register (Configuration Register F – 05h, Bit D0) is used to disable PWM output. In this case, the A and B outputs for each channel are held in the damp state. By default, PWM output is enabled.

By default, the device includes a channel-specific zero-detect mute function which is activated upon receipt of 2048 consecutive zero value input samples. Automatic transition from mute with no "pops" or "clicks" will occur on the first non-zero input value. The ZDE register (Configuration Register B – 01, Bit D1) is used to enable or disable this feature. Setting this register to zero will disable the feature, but in general, when using a digital source, this register should always be set.

The relative timing of the PWM output pulses has been designed to minimize crosstalk when adjacent channel outputs are connected to a single DDX power device. It is recommended to pair channels 1 and 2 to one power device, channels 3 and 4 to the second power device, channels 5 and 6 to the third power device, and channels 7 and 8 to the fourth power device.

8.2. Serial Data Output Interface

The audio serial output was designed to interface with standard digital audio components and to provide a number of serial data formats. DDX-8000 does not generate the serial clocks when transmitting audio output; instead it recycles the serial input clocks received at the input interface. Serial data for eight channels is provided using 6 output pins: left/right clock LRCKO (pin 56, same as LRCKI), serial clock BICKO (pin 55, same as BICKI), serial data 1 & 2 SDO12 (pin 57), serial data 3 & 4 SDO34 (pin 58), serial data 5 & 6 SDO56 (pin 62), and serial data 7 & 8 SDO78 (pin 63).

The SAO register (Configuration Register E – 04h, Bits D5-D3) and the SAOFB register (Configuration Register E – 04h, Bit D6) are used to specify the serial data output format. The default serial data output format is I^2S, MSB-First. Available formats are shown in the tables and figure that follow. See figure 9 for a diagram of these formats.

Table 20: Serial Data Output First Bit

SAOFB	Format
0	MSB-First
1	LSB-First

Note: Serial output and input formats (see section 3.1) are specified distinctly.

Table 21: Serial Audio Output Data Formats

BICKO = BICKI	SAO (2...0)	Output Interface Format
48fs	001	Right-Justified 24-bit Data
64fs	000	I^2S 24-bit Data
	001	Left-Justified Data
	010	Right-Justified 16-bit Data
	011	Right-Justified 18-bit Data
	100	Right-Justified 20-bit Data
	101	Right-Justified 24-bit Data

8.3. Serial Output Data Timing characteristics (Fs = 32 to 192kHz)

BICKO Frequency	BICKI
BICKO pulse width low (T0)	40ns min.
BICKO pulse width high (T0)	40ns min.
BICKO active to LRCKO edge delay (T2)	20ns min.
BICKO active to LRCKO edge delay (T3)	20ns min.
SDO valid to BICKO active setup (T4)	20ns min.
BICKO active to SDO hold time (T5)	20ns min.
BICKO falling to SDO edge (T6)	<1ns min.
BICKO falling to SDO edge (T6)	10ns max.

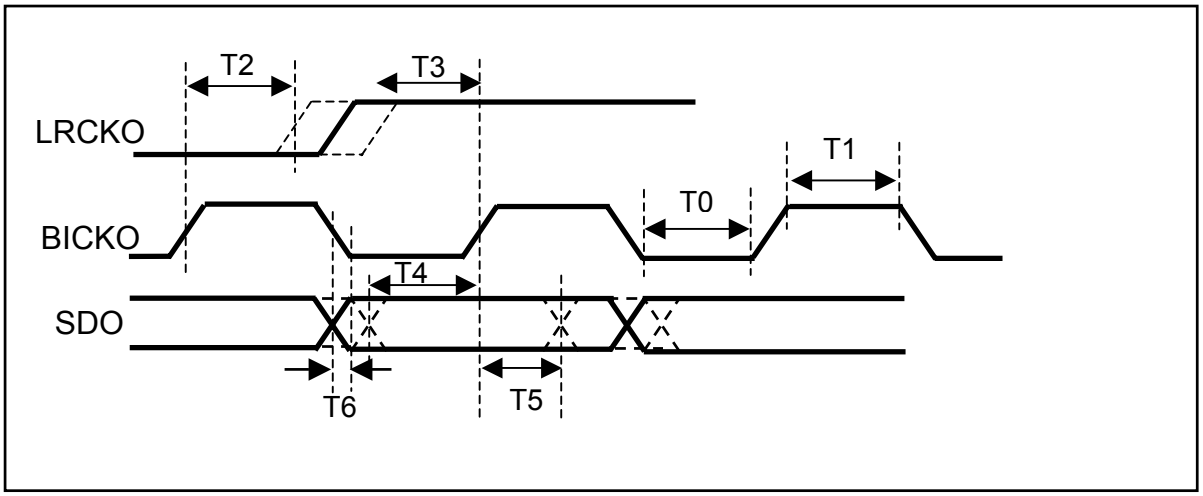


Figure 17: Serial Output Data Timing characteristics

9. PowerDown Management

9.1. Entering the PowerDown state

A PowerDown request of the DDX-8000 device is initiated by a High-to-Low transition of the PWDN pin. When this occurs, the device will perform a graceful shutdown by soft-muting the PWM outputs. After approximately 30ms, the device will enter a PowerDown state (all the device clocks are stopped) and the EAPD pin (used to switch off the external power device) will be brought Low.

9.2. Exiting the PowerDown state

The device will exit the PowerDown state immediately as soon as the PWDN pin is reasserted (brought back to High). When this occurs, the device will perform a graceful resume of activity by resuming all device clocks, soft-unmuting PWM output, and immediately bringing EAPD High (See EAPD comments below).

9.3. EAPD Control

The DDX-8000 EAPD output pin is used to switch off the external power chip (Active Low). While it is controlled indirectly by the PowerDown processes noted above, it could also be controlled directly using the EAPD bit (I2C register 5, bit 7). Unless the PowerDown state has been initiated using the PWDN pin (as noted above), the EAPD output pin will reflect the value in the EAPD bit. At reset, this bit (and hence the EAPD pin) is Low, which indicates an external power device off state. After reset, this bit must be made High by issuing I2C commands.

Note that using the EAPD bit to directly control the EAPD output pin does not cause any DDX-8000 device PowerDown activities to occur.

10. Register Summary

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	ConfA	MPC	HPE	BME	IR1	IR0	MCS2	MCS1	MCS0
01h	ConfB	DRC	ZCE	SAIFB	SAI2	SAI1	SAI0	ZDE	DSPB
02h	ConfC	HPB	RES	RES	RES	RES	RES	RES	RES
03h	ConfD	BQL	PSL	COS1	COS0	C78BO	C56BO	C34BO	C12BO
04h	ConfE	RES	SAOFB	SAO2	SAO1	SAO0	DEMP	VOLEN	MIXE
05h	ConfF	EAPD				AME	COD	I2SD	PWMD
06h	Mmute								MMute
07h	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
08h	Cmute	C8M	C7M	C6M	C5M	C4M	C3M	C2M	C1M
09h	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0Ah	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0Bh	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0Ch	C4Vol	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0Dh	C5Vol	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0Eh	C6Vol	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0Fh	C7Vol	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
10h	C8Vol	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
11h	C12im		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
12h	C34im		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
13h	C56im		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
14h	C78im		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
15h	C1234ls	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
16h	C5678ls	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
17h	L1ar	L1R3	L1R2	L1R1	L1R0	L1A3	L1A2	L1A1	L1A0
18h	L1atrt	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
19h	L2ar	L2R3	L2R2	L2R1	L2R0	L2A3	L2A2	L2A1	L2A0
1Ah	L2atrt	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
1Bh	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
1Ch	Cfaddr	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
1Dh	B2cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
1Eh	B2cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
1Fh	B2cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
20h	B0cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
21h	B0cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
22h	B0cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
23h	A2cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
24h	A2cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
25h	A2cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
26h	A1cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
27h	A1cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
28h	A1cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
29h	B1cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
2Ah	B1cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
2Bh	B1cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
2Ch	Cfud							WA	W1
2Dh	RES1	RES	RES	RES	RES	RES	RES	RES	RES
2Eh	RES2	RES	RES	RES	RES	RES	RES	RES	RES
2Fh	RES3	RES	RES	RES	RES	RES	RES	RES	RES
30h	RES4	RES	RES	RES	RES	RES	RES	RES	RES

Register Organization

- 00h-05h: Configuration Registers
- 06h-07h: Master Mute and Volume
- 08h-10h: Channel Mute and Volumes
- 11h-14h: Channel Input Mapping
- 15h-1Ah: Limiter Selection and Parameters
- 1Bh: Tone Control
- 1Ch-2Ch: Coefficient Control Registers
- 2Dh-30h: Reserved (RES)
- Blank Items are “Don’t Care”

10.1. Configuration Register A (address: 00h, default value: 83h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	MPC	HPE	BME	IR1	IR0	MCS2	MCS1	MCS0
RST	1	0	0	0	0	0	1	1

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	1	MCS0	Master Clock Select: By default, the input clock rate is specified as 256*fs. See section 4 for other available settings.
D1	R/W	1	MCS1	
D2	R/W	0	MCS2	
D3	R/W	0	IR0	Input Sample Rate: By default, the sample rate is 32/44.1/48kHz. See section 4.1 for other available settings.
D4	R/W	0	IR1	
D5	R/W	0	BME	Bass Management Enable: 0 – No Bass Management (default) 1 – Bass Management on Channel 6 See section 5.
D6	R/W	0	HPE	DDX Headphone Enable : 0 – Channels 7,8 normal DDX operation. 1 – Channels 7,8 DDX Headphone operation.
D7	R/W	1	MPC	Max Power Correction: By default, MPC is enabled.

Max Power Correction
Setting the MPC bit turns on special processing that corrects the DDX power device at high power. This mode reduces the THD+N of a full DDX system at maximum power output and slightly below. By default, Max Power Correction is enabled. In general, if using the DDX2060 or DDX2100 IC Power Devices this bit should always be set.

Head Phone Enable
Channels 7 and 8 of the DDX-8000 have the option to be processed for headphones. The headphone output must use an appropriate power device to drive headphones. This signal is a fully differential 3-wire drive called DDX Headphone (Patent Applied for). For more information about DDX headphone, contact Apogee Applications.

10.2. Configuration Register B (address: 01h, default value: 42h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	DRC	ZCE	SAIFB	SAI2	SAI1	SAI0	ZDE	DSPB
RST	0	1	0	0	0	0	1	0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	DSPB	DSP Bypass: 0 – DSP Active (default) 1 – DSP Bypassed See section 6.
D1	R/W	1	ZDE	Zero Detect Enable: 0 – Zero-Detect Mute Disabled 1 – Zero-Detect Mute Enabled (default) See section 8.1.
D2	R/W	0	SAI0	Serial Audio Input Interface Format: By default, the serial input format is I^2S, MSB-First. See section 3 for other serial input format options.
D3	R/W	0	SAI1	
D4	R/W	0	SAI2	
D5	R/W	0	SAIFB	
D6	R/W	1	ZCE	Zero Crossing Enable: 0 – Disabled See section 7 for details. 1 – Enabled (default)
D7	R/W	0	DRC	Dynamic Range Compression: 0 – Anti-Clipping Mode (default) 1 – Dynamic Range Compression Mode Defaults to Anti-Clipping. See sections 7.2.3 and 7.2.4.

10.3. Configuration Register C (address: 02h, default value: 7Ch)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	HPB	RES	RES	RES	RES	RES	OM1	OM0
RST	0	1	1	1	1	1	0	0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	OM0	DDX Power Output Mode: The default setting is 00, Drop Compensation.
D1	R/W	0	OM1	See description below.
D2	R/W	1	RES	Reserved: Do not change from default setting.
D3	R/W	1	RES	
D4	R/W	1	RES	
D5	R/W	1	RES	
D6	R/W	1	RES	
D7	R/W	0	HPB	High Pass Bypass: 0 - "Not bypassed" (default.) 1 - Bypass internal AC coupling digital high-pass filter See section 6.2 for details.

DDX Power Output Mode

Two DDX power output mode settings are available: Drop Compensation Mode is intended for use with DDX Power Devices and uses a modulation limit of 93.75%; Full-Power Mode can also be used with all DDX Power Devices and increases the modulation limit to near 100%. This mode will enable a slightly higher power output when clipping begins and can be used for an increase in output power. The table that follows shows the values used to select the desired power output mode.

OM (1...0)	Output Stage Mode
00	DDX-2060 / DDX-2100 – Drop Compensation
01	Reserved
10	DDX-2060 / DDX-2100 – Full Power Mode
11	Reserved

10.4. Configuration Register D (address: 03h, default value: 20h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	BQL	PSL	COS1	COS0	C78BO	C56BO	C34BO	C12BO
RST	0	0	1	0	0	0	0	0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	C12BO	Channels 1&2, 3&4, 5&6, 7&8 Binary Output Mode Enable Bits. A setting of 0 indicates ordinary DDX tri-state output. A setting of 1 indicates binary output mode.
D1	R/W	0	C34BO	
D2	R/W	0	C56BO	
D3	R/W	0	C78BO	
D4	R/W	0	COS0	Clock Output Select: The default clock output frequency is PLL/8. See section 4.3 for other options.
D5	R/W	1	COS1	
D6	R/W	0	PSL	Post Scale Link: 0 - Each channel uses its own post-scale value (default) 1 – Each channel uses channel 1 post-scale value
D7	R/W	0	BQL	Biquad Link: 0 - Each channel uses its own coefficient values (default) 1 – Each channel uses channel 1 coefficient values See section 6.1.7.

Binary Output
Each two-channel pair of outputs can be set to output a binary PWM stream. In this mode, output A of a channel will be considered the positive output and output B is negative inverse. For example, setting C34BO = 1 sets channels 3&4 to Binary Output (PWM) Mode.

In general, for best performance, leave the CxBO register bits at 0, DDX Ternary Output, unless using a special output stage configuration.

Post-Scale
The DDX-8000 provides an additional scaling capability post volume and dynamics control. This is a 24-bit signed fractional multiply where 800000h = -1 and 7FFFFFh = .9999998808. One scaling factor per channel referred to as CxPS where x represents the channel number is stored in a RAM block within the device (see table 8). Each post-volume/dynamics sample is multiplied by its corresponding scaling factor. By default, all post-scale factors are set to 800000h. Section 6.1.5 describes the technique for writing the scale coefficients to RAM.

For multi-channel applications, by setting the PSL register (Configuration Register D – 03h, Bit D6) to 1, the post-scale value can be taken from C1PS (channel 1 post-scale) for all channels. By default, all channels use individual post-scale factors.

10.5. Configuration Register E (address: 04h, default value: 02h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	RES	SAOFB	SAO2	SAO1	SAO0	DEMP	VOLEN	MIXE
RST	0	0	0	0	0	0	1	0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	MIXE	Mix Enable: 0 - Adjacent channel mixing is disabled (default) (Adjacent Channels) 1 - Adjacent channel-mixing mode. See section 5.2
D1	R/W	1	VOLEN	Volume Enable: 0 – Volume and dynamics control is bypassed 1 - Volume and dynamics control is enabled. (default) See section 7.3.
D2	R/W	0	DEMP	De-emphasis Enable: 0 - De-emphasis is disabled (default) 1 – De-emphasis is enabled See section 6.1.2.
D3	R/W	0	SAO0	Serial Audio Output Interface Format: By default, the serial output format is I^2S, MSB-First. See section 8 for other serial output format options.
D4	R/W	0	SAO1	
D5	R/W	0	SAO2	
D6	R/W	0	SAOFB	
D7	R/W	0	RES	Reserved: Do not change from default setting.

10.6. Configuration Register F (address: 05h, default value: 00h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	EAPD				AME	COD	SID	PWMD
RST	0				0	0	0	0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	PWMD	PWM Output Disable: 0 – PWM Output Normal (default) 1- No PWM Output
D1	R/W	0	SID	Serial Interface(I^2S Out) Disable: 0 – I^2S Output Normal (default) 1- No I^2S Output
D2	R/W	0	COD	Clock Output Disable: 0 – Clock Output Normal (default) 1- No Clock Output
D3	R/W	0	AME	AM Mode Enable : 0 – Normal DDX operation. (default) 1 – AM reduction mode DDX operation.
D4	R/W	0		Unused: Changes have no effect.
D5	R/W	0		
D6	R/W	0		
D7	R/W	0	EAPD	External Amplifier: 0 – External Power Stage PowerDown Active (default) Power Down 1 – Normal Operation See section 9.

AM Mode Enable

The DDX-8000 features a DDX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when DDX is operating in a device with an AM tuner active. The SNR of the DDX processing is reduced to >75dB in this mode, which is still greater than the SNR of AM radio.

10.7. Master Mute (address: 06h, default value: 00h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME								MMUTE
RST								0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	MMUTE	Master Mute: 0 – "Not Muted" (default) 1 – Soft mute of all channels See section 7.1.2 for details. Note that even though "Not Muted" is the default setting, at power-on-reset, the master volume setting (see below) is set to "hard mute" by default and EAPD is set to "power down" by default.
D1	R/W	0		Unused: Changes have no effect.
D2	R/W	0		
D3	R/W	0		
D4	R/W	0		
D5	R/W	0		
D6	R/W	0		
D7	R/W	0		

10.8. Master Volume (address: 07h, default value: FFh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
RST	1	1	1	1	1	1	1	1

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	1	MV0	Master Volume: The power-on-reset default value of FFh specifies a "hard mute". See section 7.1 for details on other settings.
D1	R/W	1	MV1	
D2	R/W	1	MV2	
D3	R/W	1	MV3	
D4	R/W	1	MV4	
D5	R/W	1	MV5	
D6	R/W	1	MV6	
D7	R/W	1	MV7	

10.9. Channel 1,2,3,4,5,6,7,8 Mute (address: 08h, default value: 00h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C8M	C7M	C6M	C5M	C4M	C3M	C2M	C1M
RST	0	0	0	0	0	0	0	0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	C1M	Channel 1 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.
D1	R/W	0	C2M	Channel 2 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.
D2	R/W	0	C3M	Channel 3 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.
D3	R/W	0	C4M	Channel 4 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.
D4	R/W	0	C5M	Channel 5 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.
D5	R/W	0	C6M	Channel 6 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.
D6	R/W	0	C7M	Channel 7 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.
D7	R/W	0	C8M	Channel 8 Mute: 0 - Not muted (default), 1 – Muted See section 7.1.2.

10.10. Channel 1,2,3,4,5,6,7,8 Volume (addresses: 09h – 10h, default values: 30h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	CxV7	CxV6	CxV5	CxV4	CxV3	CxV2	CxV1	CxV0
RST	0	0	1	1	0	0	0	0

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	CxV0	Channel Volume (where x is the channel number): The default value of 30h in each channel volume register at power-on-reset specifies a volume/gain setting of 0 dB. See section 7.1 for details on other settings.
D1	R/W	0	CxV1	
D2	R/W	0	CxV2	
D3	R/W	0	CxV3	
D4	R/W	1	CxV4	
D5	R/W	1	CxV5	
D6	R/W	0	CxV6	
D7	R/W	0	CxV7	

10.11. Channel Input Mapping (address 11h - 14h)

Channels 1 & 2 (address: 11h, default value: 10h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
RST		0	0	1		0	0	0

Channels 3 & 4 (address: 12h, default value: 32h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
RST		0	1	1		0	1	0

Channels 5 & 6 (address: 13h, default value: 54h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
RST		1	0	1		1	0	0

Channels 7 & 8 (address: 14h, default value: 76h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
RST		1	1	1		1	1	0

Bits D7 and D3 of these registers are unused and any changes have no effect.

On power-on-reset, each serial input channel is mapped to its corresponding processing channel. See section 3.3 for more detail.

10.12. Limiter Selection (addresses 15h – 16h)

Channels 1, 2, 3, 4 (address: 15h, default value: 00h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
RST	0	0	0	0	0	0	0	0

Channels 5,6,7,8 (address: 16h, default value: 00h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
RST	0	0	0	0	0	0	0	0

For channels 1-8, these 2-bit registers determine to which limiter each channel is mapped (or not mapped at all). By default, all channels are not mapped to any limiter. See section 7.2.1 for usage details.

10.13. Limiter 1 & 2 Rates and Thresholds (addresses 17h - 1Ah)

Limiter 1 Release and Attack Rate (address: 17h, default value: A6h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L1R3	L1R2	L1R1	L1R0	L1A3	L1A2	L1A1	L1A0
RST	1	0	1	0	0	1	1	0

Limiter 1 Attack and Release Threshold (address: 18h, default value: 67h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
RST	0	1	1	0	0	1	1	1

Limiter 2 Release and Attack Rate (address: 19h, default value: A6h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L2R3	L2R2	L2R1	L2R0	L2A3	L2A2	L2A1	L2A0
RST	1	0	1	0	0	1	1	0

Limiter 2 Attack and Release Threshold (address: 1Ah, default value: 67h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
RST	0	1	1	0	0	1	1	1

By default, an attack (compression) rate of 0.4512 dB/ms and a release rate of 0.0147 dB/ms are specified for each limiter. See section 7.2.2. for other available settings and usage specifics.

By default, the compression threshold for each limiter is set to 0 dB relative to full scale and the release setting is set to –6 dB relative to full scale. See sections 7.2.3 and 7.2.4 for other specifics regarding other compression and release threshold settings and usage specifics.

In general, default settings are optimized for musicality. It should not be necessary to change defaults except for tailored applications.

10.14. Tone Control (address: 1Bh, default value: 77h)

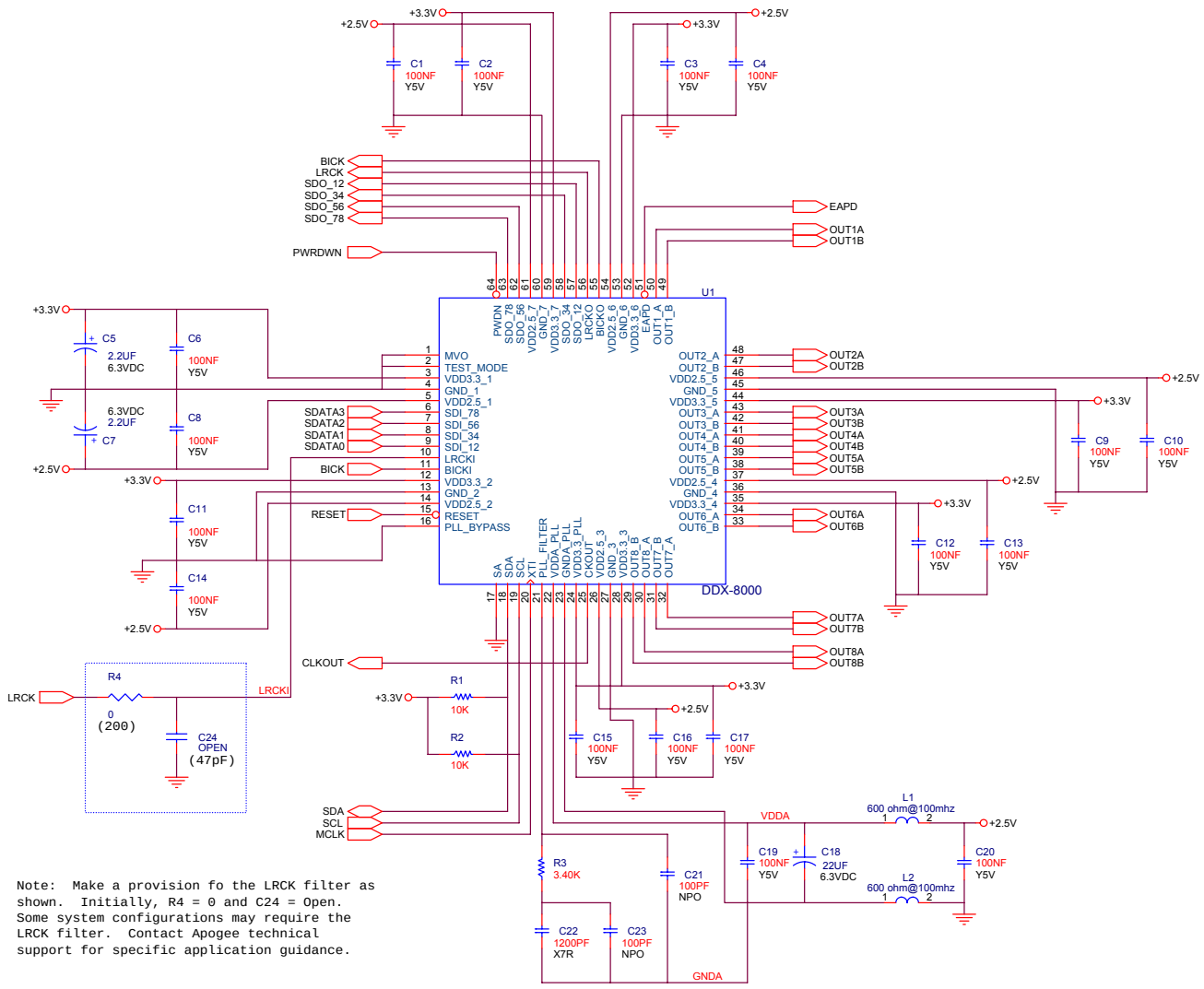
BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
RST	0	1	1	1	0	1	1	1

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	1	BTC0	Bass Tone Control: By default, a 0dB boost/cut is specified. See section 6.3 other boost/cut settings.
D1	R/W	1	BTC1	
D2	R/W	1	BTC2	
D3	R/W	0	BTC3	
D4	R/W	1	TTC0	Treble Tone Control: By default, a 0dB boost/cut is specified. See section 6.3 other boost/cut settings.
D5	R/W	1	TTC1	
D6	R/W	1	TTC2	
D7	R/W	0	TTC3	

10.15. Coefficient Control Registers (addressed 1C – 2Ch)

All values are 0 on reset. Bits D7 and D2 in register address 2Ch are unused and any changes have no effect. See sections 6.1.4 – 6.1.6 for details regarding use of these registers to read and write coefficient values.

11. Reference Schematic

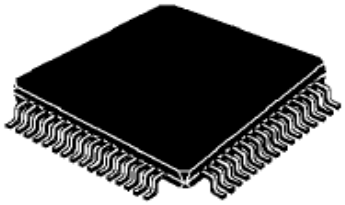


Note: Make a provision fo the LRCK filter as shown. Initially, R4 = 0 and C24 = Open. Some system configurations may require the LRCK filter. Contact Apogee technical support for specific application guidance.

Figure 18: Reference Schematic

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



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