Transition-mode PFC controller enhances performance

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Active power factor correction is a common feature in today's switch-mode power supply (SMPS), especially in those applications falling within the scope of regulations that limit harmonic currents injected into the public supply system.

A power-factor-corrected (PFC) SMPS is typically composed of two series-connected stages. First is a PFC pre-regulator (i.e. a boost converter running off the rectified main voltage), which generates a regulated intermediate DC bus. The next stage is a cascaded DC/DC converter that is powered by the intermediate bus, which generates the SMPS output rails, providing the isolation required by safety regulations. **Figure 1** shows a specific case typical of AC/DC adapters, where the cascaded DC/DC stage is a single-output flyback converter.

Each stage is governed by a controller IC that incorporates the functions needed to properly handle power flow under the specified operating conditions, as well as some of the protection features needed to safely control abnormal conditions. However, the two stages do not simply process power sequentially, but somehow "talk to one another" as well. This two-way communication between the two controller ICs is an important feature. Power on/off sequencing, as well as no-load conditions and fault handling, require a coordinated operation of the two stages.

Hence, in most SMPS designs, it is possible to see additional circuitry comprising voltage references, op amps and comparators (or just zener diodes and small-signal BJTs, depending on the requirements and value of the specific application) to establish this communication, and allow the two control chips to be coordinated.

In this respect, the PFC controller ICs available in the market offer few means to ease the task. Since they are conceived for the pre-regulator, they function as a standalone stage.

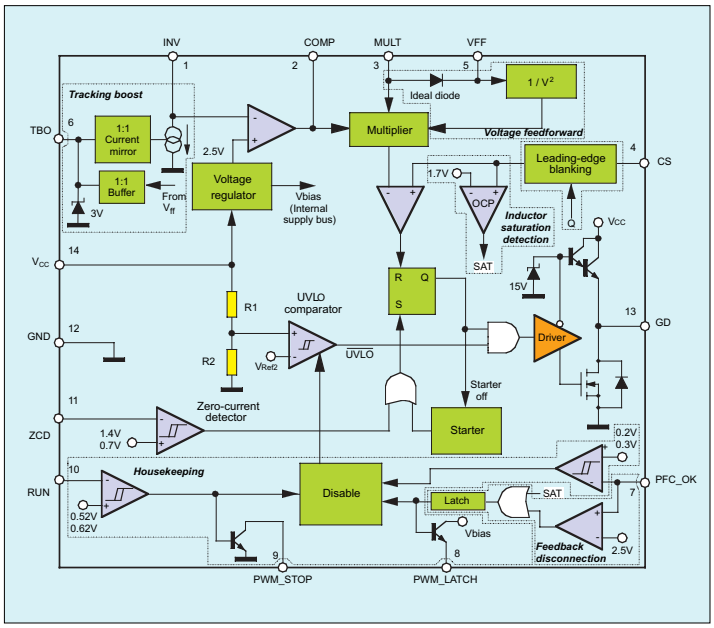

Figure 2: Transition-mode pre-regulators carry standard functions such as multiplier, voltage reference, zero-current detector and other glue logic.

Also, even in the lower power range, there are applications with demanding requirements on the SMPS in terms of static and dynamic performance. Consider high-end AC/DC adapters for laptops, where efficiency needs to be maximized to alleviate heat removal issues, which are subject to zero-to-maximum and vice versa step-load changes.

With these considerations in mind, STMicroelectronics has developed the L6563, a 14-pin controller chip for transition-mode operated PFC pre-regulators, designed for use in SMPS. Based on the control core of a standard device, it includes typical functional blocks such as multiplier, voltage reference, error amplifier and zero-current detector. Also, there are many functions aimed at improving the performance and safety of the pre-regulator, as well as simplifying the above-mentioned "glue logic" circuitry that coordinates the operation of the pre-regulator to that of the cascaded DC/DC converter.

As a transition-mode controller, the L6563 is suitable for systems handling about 250-300W (this limit is always controversial due to the high degree of subjectivity in its assessment). The device can be operated with fixed-off-time control to get continuous inductor current, thus extending its use to applications with higher power levels (500W and above). It targets applications such as high-end AC/DC adapters, ATX silver boxes, entry-level servers, PDPs and high-end LCD TVs.

Device functionality

The L6563 has additional functions that can be divided into three groups (**Figure 2**):

1. Functions that improve PFC pre-regulator performance (voltage feedforward, tracking boost and leading-edge blanking on current sense);
2. Functions that improve PFC pre-regulator safety (feed-

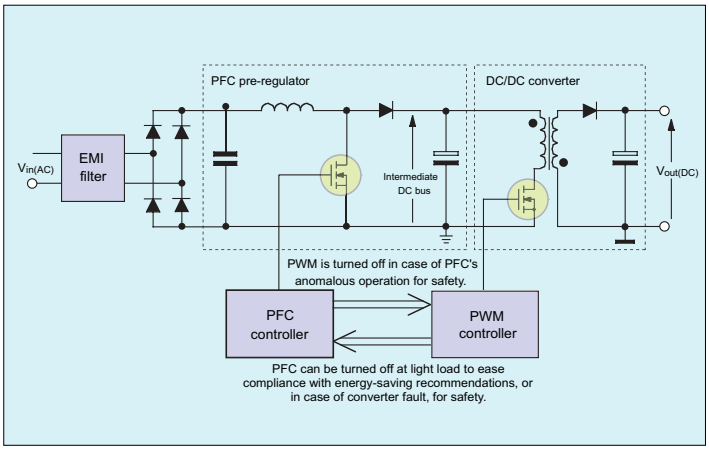

Figure 1: Each DC/DC stage is governed by a controller IC that handles power flow under the specified operating conditions.

On-board function	L6563	L6562	L6561
Tracking boost	**Yes**	No	No
Feedback failure detection	**Yes**	No	No
Input (Line) voltage feedforward	**Yes**	No	No
AC brownout detection	**Yes**	No	No
Housekeeping (Interface with PWM controller)	**Yes**	No	No
Inductor saturation detection	**Yes**	No	No
Leading-edge blanking on current sense	**Yes**	No	No
Easy-to-drive on/off control pin	**Yes**	No	No
Gate drive internal clamp	**Yes**	Yes	No
THD optimizer	**Yes**	Yes	No

Table 1: Functional differences between the L6563, the L6562 and the L6561.

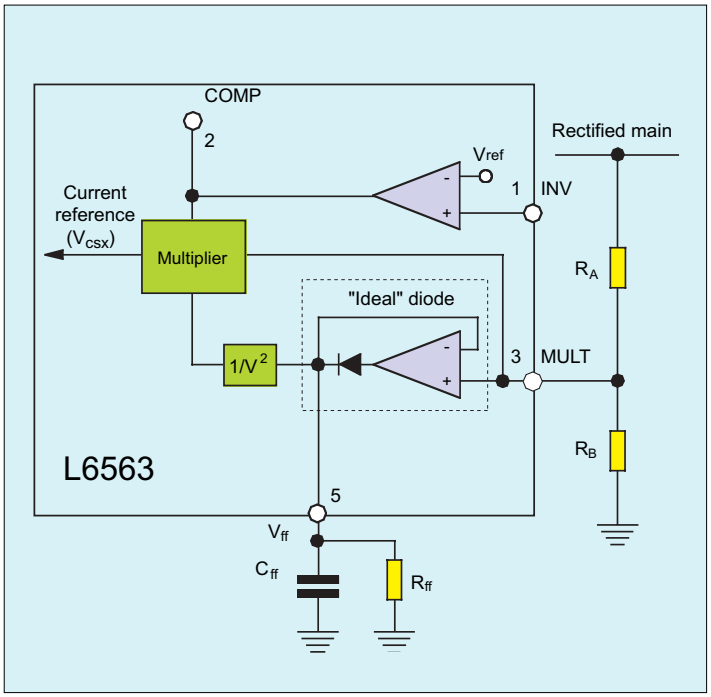

Figure 3: Capacitor R_{ff} and resistor R_{ff}, both connected to the V_{ff} pin to ground, complete an internal peak-holding circuit.

dummy loss due to resistors connected to high-voltage lines must be minimized.

Differences between this new IC and its predecessors, the L6561 and L6562, are summarized in **Table 1**.

Input voltage feedforward function

This function, available on some PFC control chips for higher-power applications (where the boost inductor is operated in continuous conduction mode at a fixed frequency), is implemented in a chip for transition-mode-operated PFC stages. Eliminating the dependence of the system gain on the input voltage by properly injecting the information on the rms input voltage in the loop brings better dynamic behavior in wide-range main applications, lower line current distortion and, most noticeably, constant maximum power capability vs. line voltage.

The L6563 realizes this function with just two external parts, using a technique that provides rejection of line voltage surges. In **Figure 3**, a capacitor C_{ff} and a resistor R_{ff}, both connected from the V_{ff} pin to ground, complete an internal peak-holding circuit. This provides a DC voltage on the V_{ff} pin that equals the peak of the rectified sine wave applied to the multiplier input MULT (no additional input voltage sensing is needed) and thus represents the mains rms voltage.

In case of sudden line voltage rise, C_{ff} will be rapidly charged through the low impedance of the internal diode and no appreciable overshoot will be visible at the pre-regulator's output. In case of line voltage drop, C_{ff} will be discharged with the time constant R_{ff}*C_{ff}, which will take some tens of ms to achieve an acceptable steady-state ripple and have low current distortion. Consequently, the output voltage can experience undershoots such as in systems with no feedforward compensation.

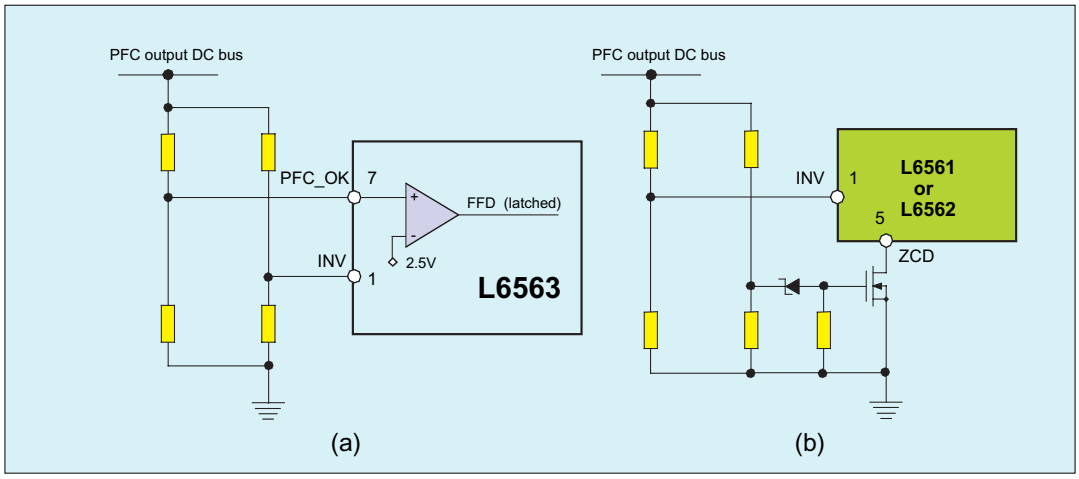

Figure 4: (a) The pin internally connects a comparator referred to a voltage reference; (b) Additional margin is required because precision is not as good as tolerance of the zener and the MOSFET's threshold.

Tracking boost function

The L6563 can either work conventionally, where the output voltage is fixed at a given value, or with the so-called "tracking boost" or "boost follower" approach, where the regulated output voltage is automatically changed, tracking the rms line voltage. This technique helps improve the boost stage efficiency at low main voltage and may also bring the additional benefit of a smaller inductor.

This function works in conjunction with the input voltage feedforward function and, compared with existing solutions in the market, offers independence of the output load, tighter tolerance and higher flexibility, with just one external resistor R_{ff} (**Figure 4**).

Only the information of the input voltage, available at the V_{ff} pin, is used to change the output voltage setpoint. The precision is good, since the tolerance of the internal temperature-compensated 1:1 mirrors is naturally tight and, then, only resistors are involved. There is maximum flexibility; it is possible to obtain a linear relationship between the main voltage and the PFC output voltage $V_{out} = p+q\ (Vin_{rms})$, where the constants p and q can be fully programmed by the user with an appropriate selection of R_t and the output divider ratio.

To avoid undesired output voltage rise in case the main voltage exceeds the maximum specified value, the voltage on

back failure detection, inductor saturation detection and brownout protection);

3. Housekeeping functions, which improve the interaction between the pre-regulator and the cascaded DC/DC converter (remote on/off control and latched/non-latched inhibit of PWM controller).

Condition	Caused by	PWM_STOP	PWM_LATCH
Feedback failure	PFC_OK > 2.5V	Open	Active (high)
Saturating inductor	CS > 1.7V	Open	Active (high)
Brownout or off	RUN < 0.52V	Active (low)	Open
Standby	PFC_OK < 0.2V	Open	Open

Table 2: L6563 facilitates the implementation of housekeeping functions.

Also, some electrical parameters have improved:

- In view of the larger power levels to handle, the dynamics available on the current sense pin has been reduced by about 36 percent. This allows the use of lower-value sense resistors and a reduction of the associated power dissipation.
- The overvoltage protection tripping current has been halved, so that the resistance values of the divider that sets the output voltage can be doubled for the same overvoltage level. This reduction halves the consumption of the divider, which is critical in applications like AC/DC adapters, where there are severe requirements on the no-load input consumption and where, as a consequence, any

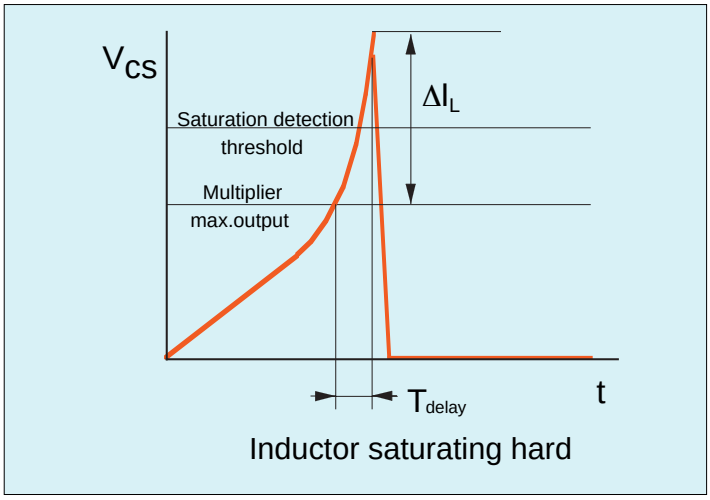

Figure 5: The boost inductor's hard saturation may be a fatal event for a PFC pre-regulator. The inductor current upslope becomes very large.

the TBO pin is clamped internally. By properly selecting the multiplier bias, it is possible to set the maximum input voltage above which input-to-output tracking ends and the output voltage becomes constant.

Blanking on current sense

Digitally blanking the current sense input of the PWM comparator for a fixed time makes it blind to the leading-edge spike due to circuit parasitics and offers improved performance compared to the RC smoothing filter used in the L6561/2. A clean operation of the boost converter is ensured even at light load without the additional time delay caused by the RC time constant, which adversely affects the maximum deliverable power at high mains voltage in case of overload.

In addition to the standard protection function that handles overvoltage conditions resulting from an abrupt load/line change or occurring at startup, the L6563 includes an output voltage monitoring system that provides protection against feedback loop failures, long-term degradations and erroneous settings.

In **Figure 4a**, there is a pin (PFC_OK) dedicated to providing additional monitoring of the output voltage. The pin internally connects a comparator referred to a voltage reference, tracking the reference used for setting the output voltage. The monitoring divider will be selected so that the voltage at the pin reaches the reference when the output voltage exceeds a preset value, which also includes worst-case tolerances and load/line transients.

When this function is triggered, the device is latched off as long as the supply voltage V_{cc} of the IC is above the UVLO threshold. If required, it is possible to stop the PWM controller IC of the cascaded DC/DC converter, so that the entire unit is latched off. To restart the L6563, it is necessary to recycle the input power, so that its V_{cc} voltage goes below the UVLO thresholds.

The external implementation shown in **Figure 4b** is probably the simplest one. The precision is not as good because of the tolerance of the zener and the MOSFET's threshold, and there is no correlation with the output voltage setpoint, hence, additional margin is required. Finally, there is no latch-off or hysteresis, thus the unit continuously turns on and off and the output voltage may stay at a dangerously high level at light load.

The boost inductor's hard saturation may be a fatal event for a PFC pre-regulator: The inductor current upslope becomes so large (50-100 times steeper) that the internal propagation delays prevent any control (**Figure 5**). The current may reach abnormally high values; the MOSFET may work in the active region and dissipate a huge amount of power, which leads to a catastrophic failure after a few switching cycles. This condition–which may occur if the boost inductor is not well-designed, or during overload when the output-to-input voltage difference becomes so small as to prevent boost inductor demagnetization–is detected through a second comparator on the current sense pin.

Parameter	Value
Input voltage range	88-264Vac
Regulated output voltage range	220-390Vdc
Maximum output voltage	400Vdc
Maximum output power	80W
Maximum output overvoltage	40Vdc
Minimum switching frequency	40kHz
Minimum expected efficiency	90%

Table 3: 80W wide-range main PFC pre-regulator with tracking boost function: basic electrical specification.

Brownout protection function

Brownout, a mains undervoltage, may cause overheating of the primary power section due to excess rms current. It can also cause the PFC pre-regulator to work open-loop. This could be dangerous, considering its poor dynamic response, should the input voltage return abruptly to its rated value. This is why it is usually preferable to shut down the unit during brownout.

The L6563 easily allows this (**Figure 6**). The RUN pin internally connects a comparator referred to a voltage reference; an external voltage lower than the internal reference keeps the IC off. This function is quite flexible and can also be used for other purposes. In applications where the PFC stage is the master (i.e. it starts before the DC/DC converter does), it is possible to stop the PWM controller IC of the cascaded DC/DC converter, so that the entire unit is turned off.

Figure 6a is of general use while **Figure 6b** can be used if the bias levels of the multiplier and the R_{ff}*C_{ff} time constant are compatible with the specified brownout level and with the specified holdup time, respectively.

Housekeeping functions

A special feature of the L6563 is that it facilitates the implementation of the "housekeeping" circuitry needed to coordinate the operation of the PFC stage with that of the cascaded DC/DC converter. The L6563 provides some input and output pins to do that: RUN, PFC_OK (inputs), PWM_STOP and PWM_ LATCH (outputs).

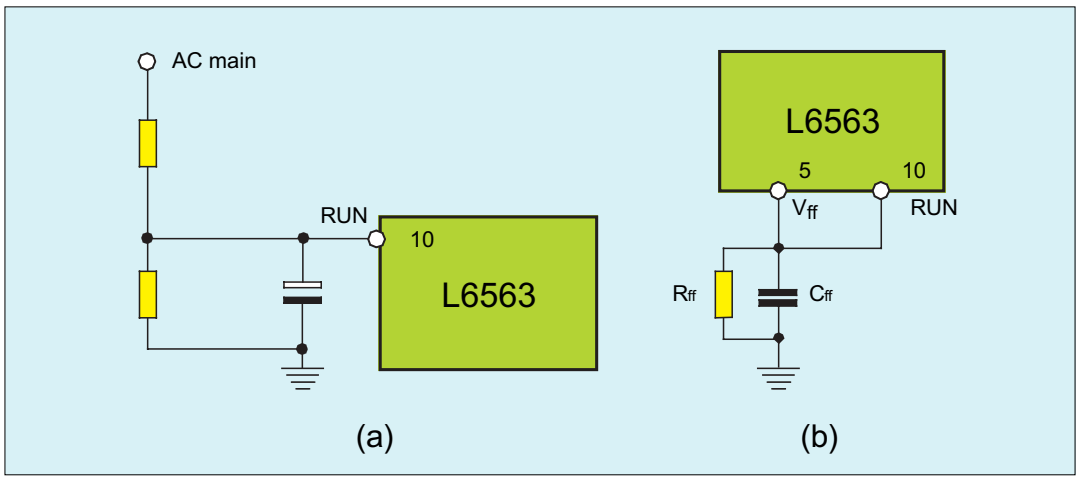

Figure 6: The RUN pin internally connects a comparator referred to a voltage reference; an external voltage lower than the internal reference keeps the IC off.

The operation of the RUN pin has already been described in the previous section. Pulling it low causes the output pin PWM_STOP to be forced low (it is open, otherwise); this is meant to turn off the PWM chip of the cascaded DC/DC converter and can be used as brownout protection or as a remote on/off control from some logic signal.

The PFC_OK pin, already seen as part of the FDD function, turns off the L6563 if pulled low. Aside from protecting the IC in case of a shorted PFC_OK pin to ground that would cause the protection to be ineffective, this feature is also a second remote on/off input that can be used as an alternative to RUN. The designer can choose either one, depending on which is more convenient in their application. Note, however, that unlike the RUN pin, the PFC_OK pin does not affect the status of the PWM_STOP output when pulled low.

Finally, the PWM_LATCH pin is an open-emitter output. It is normally open when the PFC works properly and goes high if either the FFD function or the inductor saturation detection function is tripped with the aim of latching off the PWM controller of the cascaded DC/DC converter (**Table 2**). □