

**SANYO**

No. 5169

**STK391-020****2-Channel Convergence Correction Circuit**  
( $I_C$  max = 6A)**Overview**

The STK391-020 is a convergence correction circuit IC for video projectors. It incorporates two output amplifiers in a single package, making possible the construction of CRT horizontal and vertical convergence correction output circuits for each of the RGB colors using just three hybrid ICs.

**Applications**

- Video projectors

**Features**

- 2 output amplifier circuits in a single package
- High maximum supply voltage ( $V_{CC}$  max =  $\pm 44V$ )
- Low thermal resistance ( $\theta_{j-c}$  =  $2.7^{\circ}C/W$ )
- High temperature stability (good idling current temperature compensation)
- Low correction coil inductance for improved oscillator stability (up to  $f_H$  = 64kHz)
- Pin compatible with the STK4274 for easy replacement

**Specifications**

**Maximum Ratings** at  $T_a = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		$\pm 44$	V
Maximum collector current	$I_C$	Tr9, 11, 20, 22	6.0	A
Thermal resistance	$\theta_{j-c}$	Tr9, 11, 20, 22 (per transistor)	2.7	$^{\circ}C/W$
Junction temperature	$T_j$		150	$^{\circ}C$
Operating substrate temperature	$T_c$		105	$^{\circ}C$
Storage temperature	$T_{slg}$		-30 to +105	$^{\circ}C$

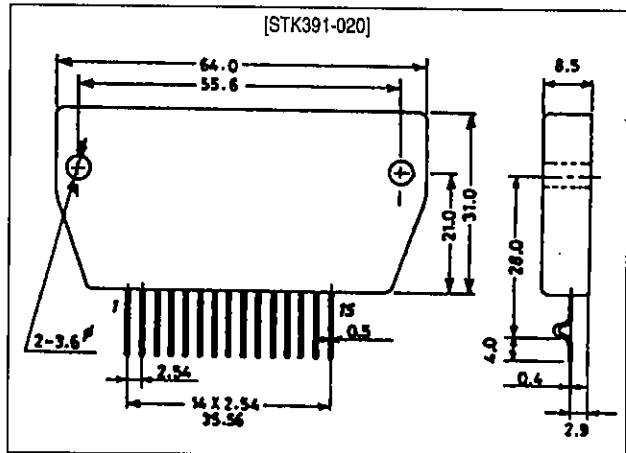
**Operating Characteristics** at  $T_a = 25^{\circ}C$ ,  $R_g = 50\Omega$ ,  $V_{CC} = \pm 24V$

Parameter	Symbol	Conditions	min	typ	max	Unit
Output noise voltage	$V_{NO}$		-	-	0.2	mVrms
Quiescent current	$I_{CCO}$		-	20	40	mA
Neutral voltage	$V_N$		-50	0	+50	mV
Output delay time	$t_D$	$f = 15.75kHz$ , triangular wave input, $V_{OUT} = 1.5V_{p-p}$	-	-	1	$\mu s$

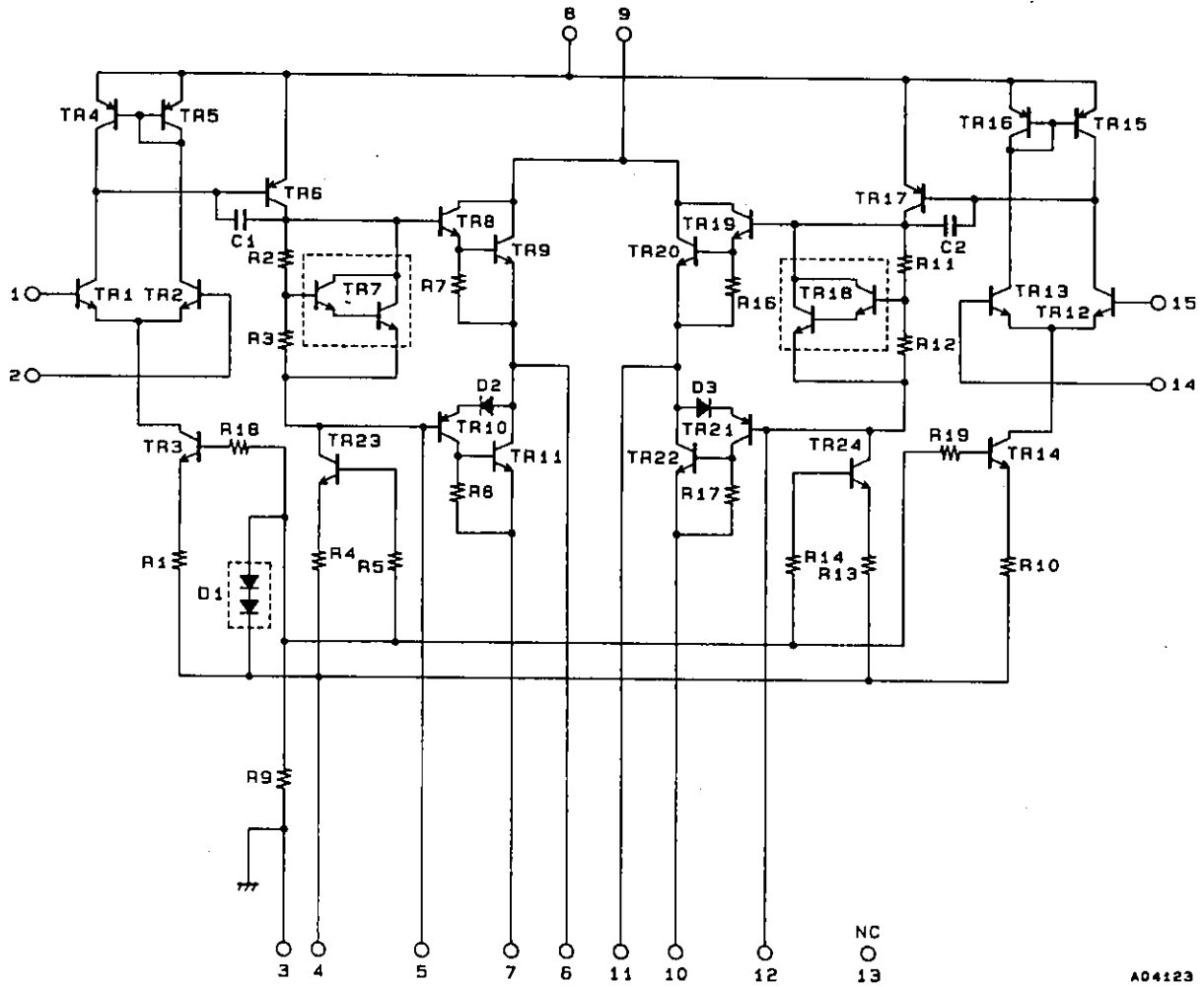
**Package Dimensions**

unit: mm

4062

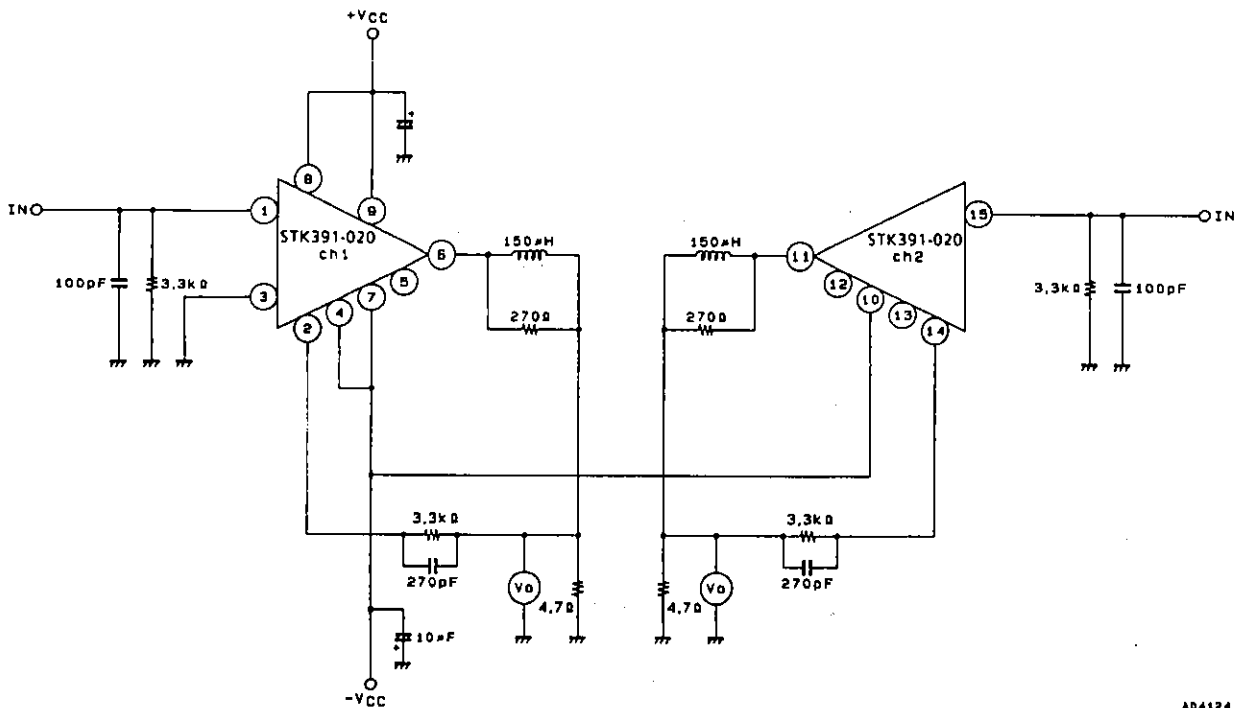


Equivalent Circuit



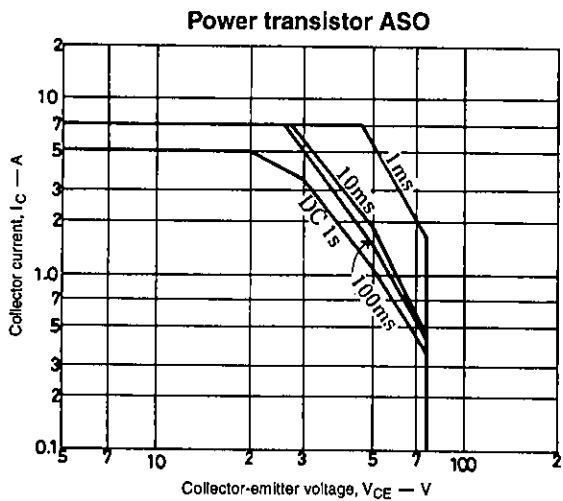
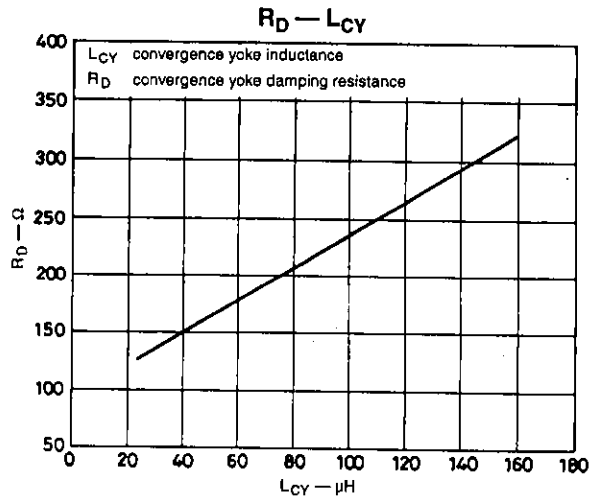
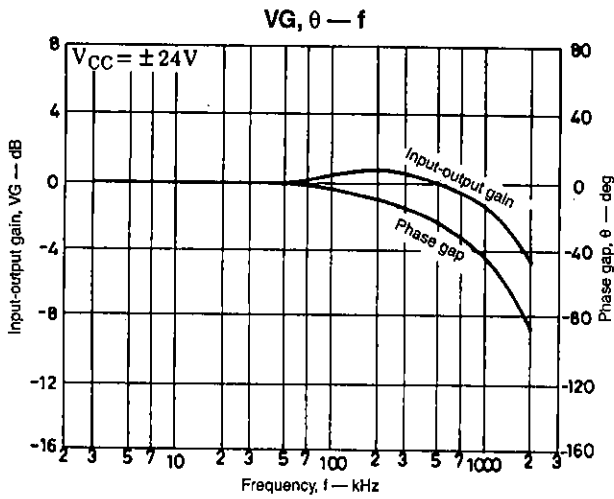
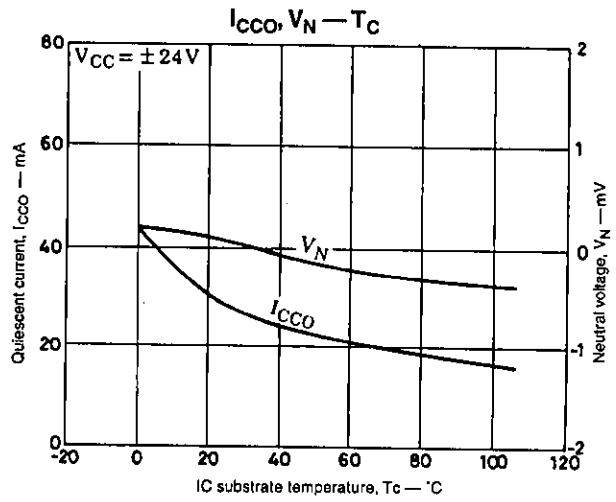
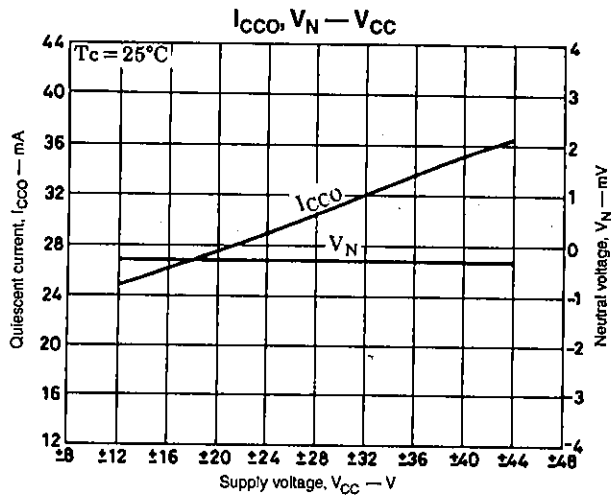
AD4123

Test Circuit



AD4124

Vo:  $V_{NO}$  is measured by connecting a VTVM.  
 $V_N$  is measured by connecting a DC voltmeter.  
 $I_D$  is measured by connecting an oscilloscope.



## Heatsink Design

### Tj max, Tc max, θj-c

The heatsink design is determined by the maximum ratings of several key parameters—Tj max, Tc max and θj-c.

- Tj max (junction temperature)  
Tj max is dependent on the physical structure of each functional element. A junction temperature exceeding this rating can lead to device deterioration and breakdown, so the design must not exceed this rating.
- Tc max (operating substrate temperature)  
Tc max is dependent on the materials used within an element and on the circuit design, and should be selected on the basis of reliability. Operation exceeding this value is not guaranteed.
- θj-c (thermal resistance)  
θj-c is dependent on the heatsink design, which can vary greatly. The heatsink necessary is determined by calculation using the maximum rating for Tj.

As Tj and Tc operating conditions are independent, the heatsink must be designed to satisfy the maximum ratings for both parameters.

### Heatsink Design Considerations

In the expressions below Pd represents the operating IC substrate internal power dissipation and Pc represents the power dissipation per transistor. The heatsink thermal resistance, θc-a, required to dissipate the total power dissipation, Pd, is determined as follows:

Condition 1: IC substrate temperature not to exceed 105°C.

$$Pd \times \theta_{c-a} + T_a < 105^\circ\text{C} \text{ (Tc max)} \dots\dots\dots (1)$$

where Ta is the guaranteed maximum ambient temperature.

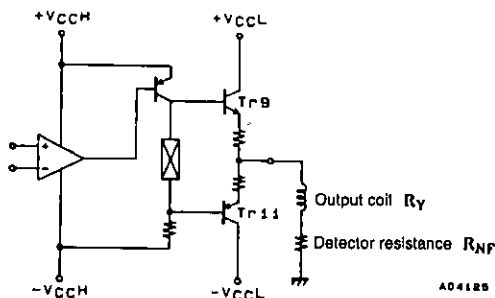
Condition 2: Power transistor junction temperature, Tj, not to exceed 150°C.

$$Pd \times \theta_{c-a} + Pc \times \theta_{j-c} + T_a < 150^\circ\text{C} \text{ (Tj max)} \dots\dots (2)$$

where θj-c is the power transistor thermal resistance per transistor. Therefore, the heatsink design must satisfy both these expressions.

### Design Process

A model circuit for a single channel in the STK391-020 is shown below.



The power dissipation, Pd, is the sum of channel 1, Pd1, and channel 2, Pd2, power dissipations:

$$Pd \text{ max} = Pd1 \text{ max} + Pd2 \text{ max}$$

Therefore, from equation (1),

$$\theta_{c-a} < \frac{T_c \text{ max} - T_a \text{ max}}{Pd \text{ max}} \dots\dots\dots (3)$$

the necessary heatsink resistance is determined (note that Tc max = 105°C).

The power dissipation per power transistor per channel, Pc, is related to the transistor junction temperature by the following equation.

$$T_j = Pd \text{ max} \times \theta_{c-a} + T_a + Pc \times \theta_{j-c} \dots\dots\dots (4)$$

where Tj cannot exceed Tj max = 150°C. Therefore, in order to maintain Tj below 150°C, a lower heatsink thermal resistance, θc-a, is necessary to lower Tc.

### Heatsink Design Example

This example assumes the following worst-case conditions—VccH = ±35V, VccL = ±25V, output coil LY = 80µH and Ry = 0Ω, current detector resistance RNF = 4.7Ω, Ip-o max = 0.6Ap-o (Ip-p = 1.2A) sawtooth wave input, Io (DC) max = 0.6A DC input, both channels operating, Ta max = 60°C (guaranteed maximum).

The channel 1 power dissipation, Pd1, is given from Figures 1 and 2.

- Pd1 max = 7.0W (AC) with sawtooth wave input
- Pd1 max = 13.2W (DC) with DC input

As Pd1 max (AC) < Pd1 max (DC), the power dissipation is greater with DC input. Also, looking at the output transistor dissipation, Pc,

- Pc = 0.5Pd1 with sawtooth wave input
- Pc = Pd1 with DC input (one side transistor continuously ON)

the power dissipation is also higher with DC input. Accordingly, the heatsink design example below assumes DC input. The power dissipation in the predriver stage is ignored.

As Pd1 max = Pd2 max = 13.2W, Pd max (both channels) is given by

$$Pd \text{ max} = Pd1 \text{ max} + Pd2 \text{ max} = 26.4\text{W}$$

From equation (3) with Ta = 60°C,

$$\theta_{c-a} = \frac{T_c \text{ max} - T_a}{Pd \text{ max}} = \frac{105 - 60}{26.4} = 1.70^\circ\text{C/W}$$

For a 2mm aluminum heatsink with no surface coating, the necessary surface area, S, is given from Figure 3.

$$S = 780\text{cm}^2 \text{ (28cm} \times \text{28cm)}$$

Also, from equation (4), the output stage power transistor junction temperature is given by

$$\begin{aligned}
 T_j &= P_{d \max} \times \theta_{c-a} + T_a + P_{c \max} \times \theta_{j-c} \\
 &= 26.4 \times 1.7 + 60 + 13.2 \times 2.7 \\
 &= 140.5^\circ\text{C}
 \end{aligned}$$

which provides a 9.5°C derating below  $T_j \max = 150^\circ\text{C}$ . However, an allowance for the predriver stage power dissipation (transistors, resistors, etc.) should also be included in the substrate internal power dissipation,  $P_d$ .

Figure 1.  $P_d - I_{p-o}$

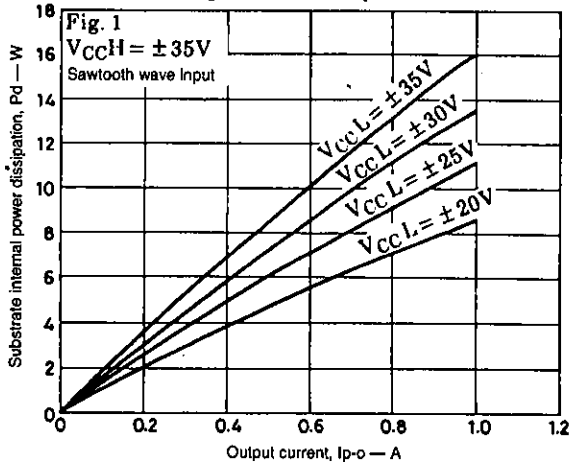


Figure 2.  $P_d - I_o$

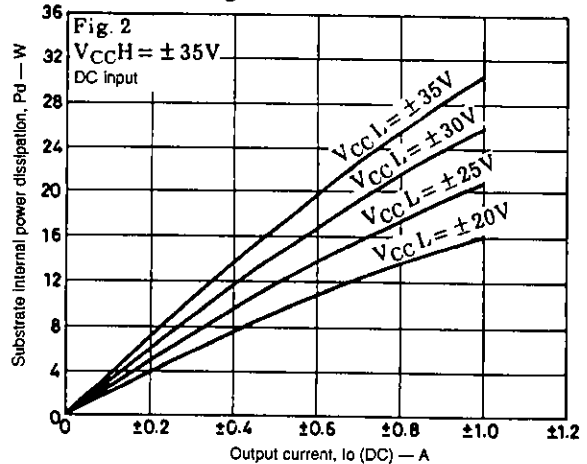
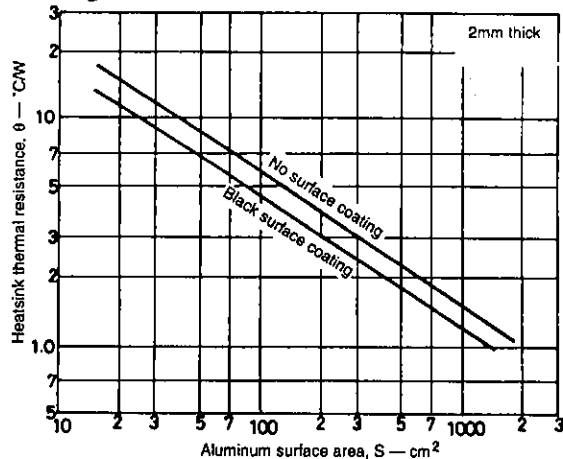


Figure 3. Al heatsink thermal resistance



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