DATA SHEET

TDA9321H
I²C-bus controlled TV input processor

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

I²C-bus controlled TV input processor TDA9321H

FEATURES

- Multistandard Vision IF (VIF) circuit with Phase-Locked Loop (PLL) demodulator
- Sound IF (SIF) amplifier with separate input for single reference Quasi Split Sound (QSS) mode and separate Automatic Gain Control (AGC) circuit
- AM demodulator without extra reference circuit
- Switchable group delay correction circuit which can be used to compensate the group delay pre-correction of the B/G TV standard in multistandard TV receivers
- Several (I²C-bus controlled) switch outputs which can be used to switch external circuits such as sound traps, etc.
- Flexible source selection circuit with 2 external CVBS inputs, 2 Luminance (Y) and Chrominance (C) (or additional CVBS) inputs and 2 independently switchable outputs
- Comb filter interface with CVBS output and Y/C input
- Integrated chrominance trap circuit
- Integrated luminance delay line with adjustable delay time
- Integrated chrominance band-pass filter with switchable centre frequency
- Multistandard colour decoder with 4 separate pins for crystal connection and automatic search system
- PALplus helper demodulator
- Possible blanking of the helper signals for PALplus and EDTV-2
- Internal baseband delay line
- Two linear RGB inputs with fast blanking; the RGB signals are converted to YUV signals before they are supplied to the outputs; one of the RGB inputs can also be used as YUV input
- Horizontal synchronization circuit with switchable time constant for the PLL and Macrovision/subtitle gating
- Horizontal synchronization pulse output or clamping pulse input/output
- Vertical count-down circuit
- Vertical synchronization pulse output
- Two-level sandcastle pulse output
- I²C-bus control of various functions
- Low dissipation.

GENERAL DESCRIPTION

The TDA9321H (see Fig.1) is an input processor for ‘High-end’ television receivers. It contains the following functions:

- Multistandard IF amplifier with PLL demodulator
- QSS-IF amplifier and AM sound demodulator
- CVBS and Y/C switch with various inputs and outputs
- Multistandard colour decoder which can also decode the PALplus helper signal
- Integrated baseband delay line (64 μs)
- Sync processor which generates the horizontal and vertical drive pulses for the feature box (100 Hz applications) or display processor (50 Hz applications).

The supply voltage for the TDA9321H is 8 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9321H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage (pins V_{P1} and V_{P2})	7.2	8.0	8.8	V
I_P	supply current (pins V_{P1} and V_{P2})	–	120	–	mA
Input signals					
$V_{i(VIF)(rms)}$	VIF amplifier sensitivity (RMS value)	–	35	–	μV
$V_{i(SIF)(rms)}$	SIF amplifier sensitivity (RMS value)	–	30	–	μV
$V_{i(CVBS/Y)(p-p)}$	CVBS or Y input signal (peak-to-peak value)	–	1.0	–	V
$V_{i(C)(p-p)}$	chrominance input signal (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{i(RGB)(p-p)}$	RGB input signal (peak-to-peak value)	–	0.7	–	V
Output signals					
$V_{o(VIFO)(p-p)}$	demodulated CVBS output signal (peak-to-peak value)	–	2.5	–	V
$V_{o(CVBSPIP)(p-p)}$	CVBS output signal for Picture-In-Picture (peak-to-peak value)	–	1.0	–	V
$V_{o(CVBSTXT)(p-p)}$	CVBS output signal for teletext (peak-to-peak value)	–	2.0	–	V
$I_{o(TAGC)}$	tuner AGC output current	0	–	5	mA
$V_{o(QSS)(rms)}$	QSS output signal (RMS value)	–	100	–	mV
$V_{o(AM)(rms)}$	demodulated AM sound output signal (RMS value)	–	500	–	mV
$V_{o(V)(p-p)}$	−V output signal (peak-to-peak value)	–	1.05	–	V
$V_{o(U)(p-p)}$	−U output signal (peak-to-peak value)	–	1.33	–	V
$V_{o(Y)(b-w)}$	Y output signal (black-to-white value)	–	1.0	–	V
$V_{o(hor)}$	horizontal pulse output	–	5	–	V
$V_{o(ver)}$	vertical pulse output	–	5	–	V
$V_{o(sc)(p-p)}$	subcarrier output signal (peak-to-peak value)	–	250	–	mV

BLOCK DIAGRAM

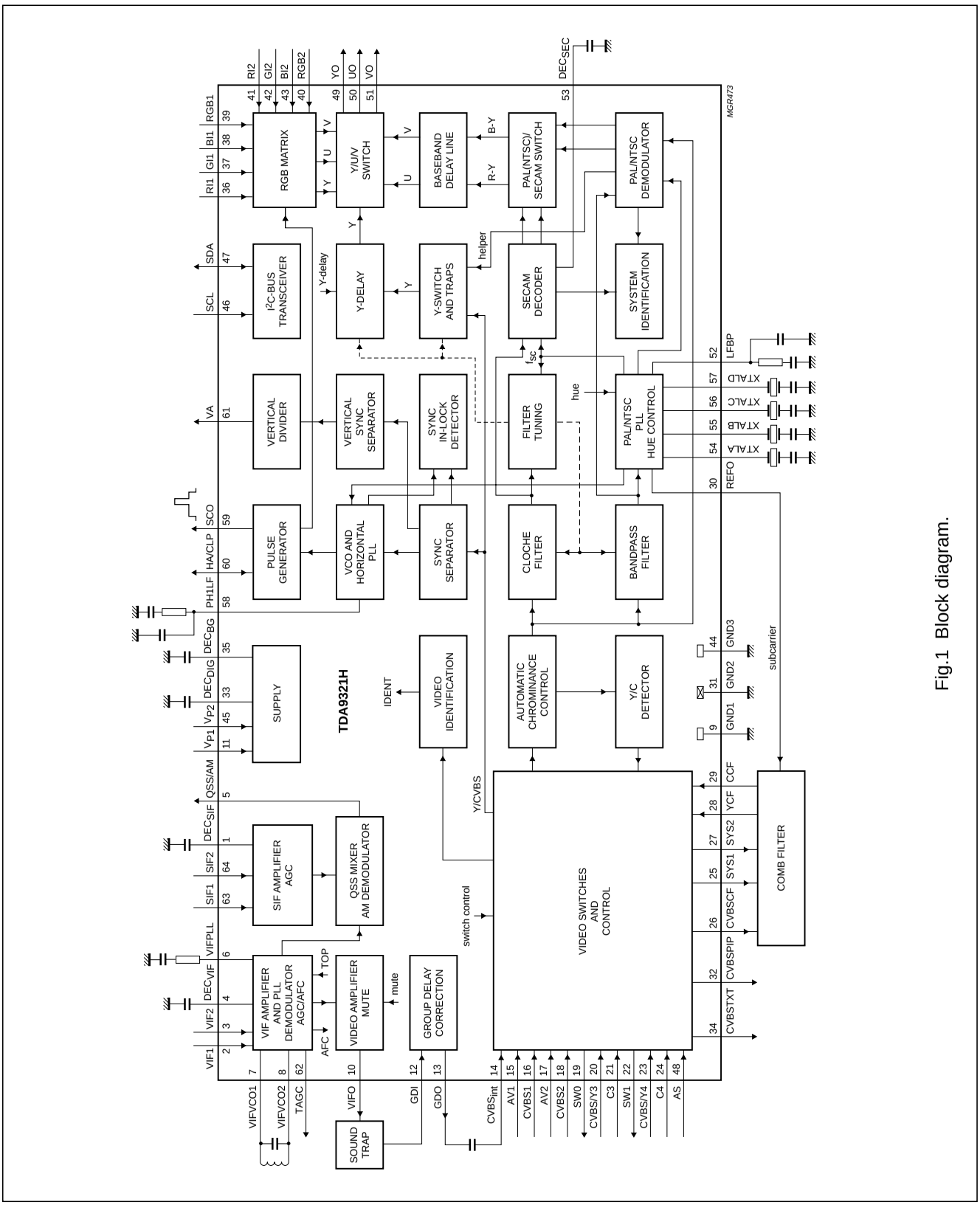


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DEC_{SIF}	1	SIF AGC decoupling
VIF1	2	VIF input 1
VIF2	3	VIF input 2
DEC_{VIF}	4	VIF AGC decoupling
QSS/AM	5	combined QSS and AM sound output
VIFPLL	6	VIF PLL filter
VIFVCO1	7	VIF VCO tuned circuit 1
VIFVCO2	8	VIF VCO tuned circuit 2
GND1	9	main supply ground
VIFO	10	VIF output
V_{P1}	11	positive supply 1 (+8 V)
GDI	12	group delay correction input
GDO	13	group delay correction output
$CVBS_{int}$	14	internal CVBS input
AV1	15	AV input 1
CVBS1	16	CVBS input 1
AV2	17	AV input 2
CVBS2	18	CVBS input 2
SW0	19	switch output bit 0 (I²C-bus)
CVBS/Y3	20	CVBS or luminance input 3
C3	21	chrominance input 3
SW1	22	switch output bit 1 (I²C-bus)
CVBS/Y4	23	CVBS or luminance input 4
C4	24	chrominance input 4
SYS1	25	system output 1 for comb filter
CVBSCF	26	CVBS output for comb filter
SYS2	27	system output 2 for comb filter
YCF	28	luminance input from comb filter
CCF	29	chrominance input from comb filter
REFO	30	reference output (subcarrier)
GND2	31	digital supply ground
CVBSPIP	32	CVBS output for Picture-In-Picture

SYMBOL	PIN	DESCRIPTION
DEC_{DIG}	33	digital supply decoupling
CVBSTXT	34	CVBS output for teletext
DEC_{BG}	35	band gap decoupling
RI1	36	red input 1
GI1	37	green input 1
BI1	38	blue input 1
RGB1	39	RGB insertion input 1
RGB2	40	RGB insertion input 2
RI2	41	red input 2
GI2	42	green input 2
BI2	43	blue input 2
GND3	44	ground 3
V_{P2}	45	positive supply 2 (+8 V)
SCL	46	serial clock input (I²C-bus)
SDA	47	serial data input/output (I²C-bus)
AS	48	address select input (I²C-bus)
YO	49	luminance output
UO	50	U-signal output
VO	51	V-signal output
LFBP	52	loop filter burst phase detector
DEC_{SEC}	53	SECAM PLL decoupling
XTALA	54	crystal A (4.433619 MHz)
XTALB	55	crystal B (3.582056 MHz)
XTALC	56	crystal C (3.575611 MHz)
XTALD	57	crystal D (3.579545 MHz)
PH1LF	58	phase 1 loop filter
SCO	59	sandcastle pulse output
HA/CLP	60	horizontal pulse output or clamp pulse input/output
VA	61	vertical pulse output
TAGC	62	tuner AGC output
SIF1	63	SIF input 1
SIF2	64	SIF input 2

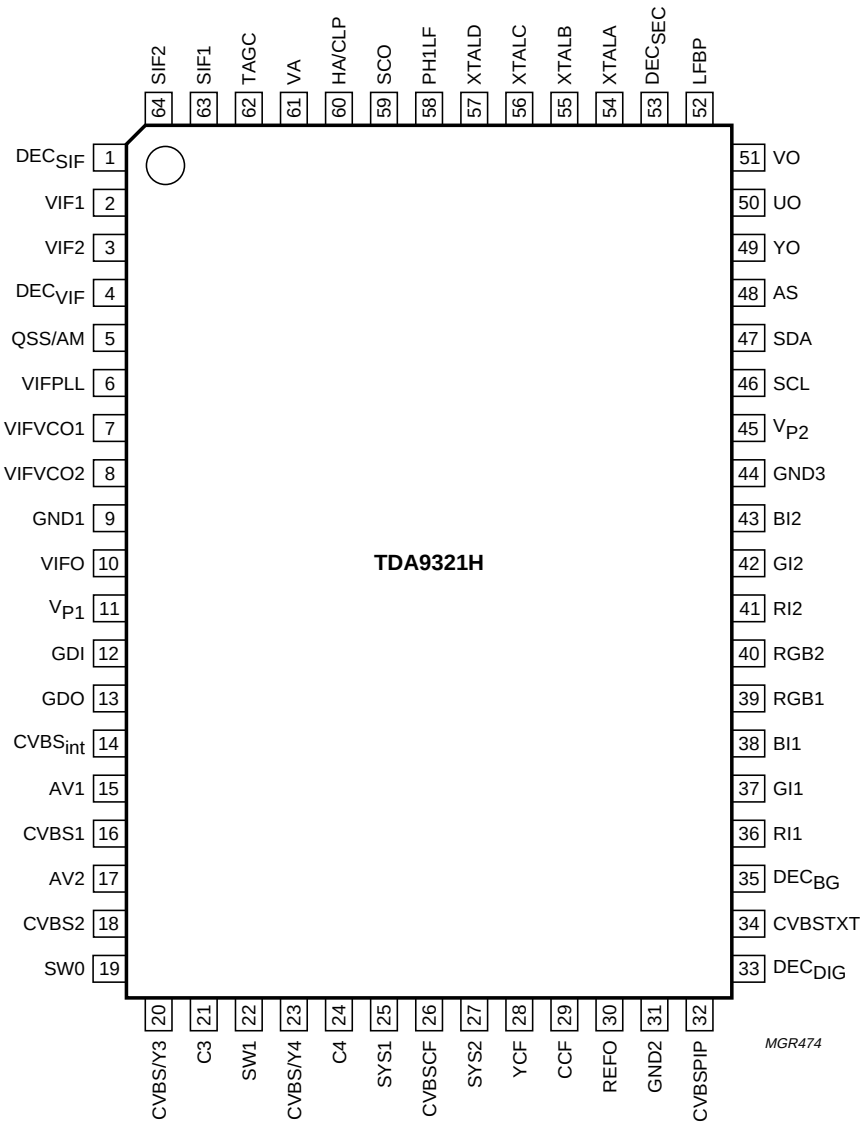


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The VIF amplifier contains 3 AC-coupled control stages with a total gain control range which is higher than 66 dB. The sensitivity of the circuit is comparable with that of modern IF-ICs.

The video signal is demodulated by a PLL carrier regenerator. This circuit contains a frequency detector and a phase detector. During acquisition the frequency detector will tune the VCO to the correct frequency. The initial adjustment of the oscillator is realized via the I²C-bus. The switching between SECAM L and L' can also be realized via the I²C-bus. After lock-in the phase detector controls the VCO so that a stable phase relationship between the VCO and the input signal is achieved. The VCO operates at twice the IF frequency. The reference signal for the demodulator is obtained by means of a frequency divider circuit. To get a good performance for phase modulated carrier signals the control speed of the PLL can be increased by bit FFI.

The AFC output is obtained by using the VCO control voltage of the PLL and can be read via the I²C-bus. For fast search tuning systems the window of the AFC can be increased with a factor 3. The setting is realized with bit AFW.

The AGC detector operates on top-sync and top-white-level. The demodulation polarity is switched via the I²C-bus. The AGC detector time constant capacitor is connected externally; this is mainly because of the flexibility of the application. The time constant of the AGC system during positive modulation is rather long, this is to avoid visible variations of the signal amplitude. To improve the speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When, during 3 field periods, no action is detected the speed of the system is increased. For signals without peak white information the system switches automatically to a gated black level AGC. Because a black level clamp pulse is required for this mode of operation the circuit will only switch to black level AGC in the internal mode.

The circuits contain a video identification (ident) circuit which is independent of the synchronization circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor. However, this ident circuit cannot be made as sensitive as the slower sync ident circuit (bit SL). It is recommended to use both ident outputs to obtain a reliable search system. The ident output is supplied to the tuning system via the I²C-bus.

The input of the ident circuit is connected to pin 14 (see Fig.3). This has the advantage that the ident circuit can also be made operative when a scrambled signal is received (descrambler connected between pins 10 and 14). A second advantage is that the ident circuit can be used when the VIF amplifier is not used (e.g. with built-in satellite tuners). The video ident circuit can also be used to identify the selected CBVS or Y/C signal. The switching between the 2 modes can be realized with bit VIM.

The TDA9321H contains a group delay correction circuit which can be switched between the BG and a flat group delay response characteristic. This has the advantage that in multistandard receivers no compromise has to be made for the choice of the SAW filter. Both the input and output of the group delay correction circuit are externally available so that the sound trap can be connected between the VIF output and the group delay correction input. The output signal of the correction circuit can be supplied to the internal video processing circuit and to the external SCART plug.

The IC has several (I²C-bus controlled) output ports which can be used to switch sound traps or other external components.

When the VIF amplifier is not used the complete VIF amplifier can be switched off with bit IFO.

Sound circuit

The SIF amplifier is similar to the VIF amplifier and has a gain control range of approximately 66 dB. The AGC circuit is related to the SIF carrier levels (average level of AM or FM carriers) and ensures a constant signal amplitude to the AM demodulator and the QSS mixer.

The single reference QSS mixer is realized by a multiplier. In this multiplier the SIF signal is converted to the intercarrier frequency by mixing it with the regenerated picture carrier from the VCO. The mixer output signal is supplied to the output via a high-pass filter for attenuation of the residual video signals. With this system a high performance hi-fi stereo sound processing can be achieved.

The AM sound demodulator is realized by a multiplier. The modulated SIF signal is multiplied in phase with the limited SIF signal. The demodulator output signal is supplied to the output via a low-pass filter for attenuation of the carrier harmonics.

Video switches

The circuit has 3 CVBS inputs (1 internal and 2 externals) and 2 Y/C inputs. The Y/C inputs can also be used as additional CVBS inputs. The switch configuration is given in Fig.3. The various sources can be selected via the I²C-bus.

The circuit can be set in a mode in which it automatically detects whether a CVBS or a Y/C signal is supplied to the Y/C inputs. In this mode the TV-standard identification first takes place on the added Y/CVBS and the C input signal. Then both chrominance input signal amplitudes are checked once and the input signal with the highest burst signal amplitude is selected. The result of the detection can be read via the I²C-bus.

The IC has 2 inputs (AV1 and AV2) which can be used to read the status levels of pin 8 of the SCART plug. The information is available in the output status byte 02 in bits D0 to D3.

The 3 outputs of the video switches (CVBSCF, CVBSTXT and CVBSPIP) can be independently switched to the various input signals. The names are just arbitrary and it is, for instance, possible to use the CVBSCF signal to drive the comb filter and the teletext decoder in parallel and to supply the CVBSTXT signal to the SCART plug (via an emitter follower).

For comb filter interfacing the circuit has the CVBSCF output, a 3rd Y/C input, a reference signal output REFO and 2 control pins (SYS1 and SYS2) which switch the comb filter to the standard of the incoming signal (as detected by the ident circuit of the colour decoder). When a signal is recognized which can be combed and the comb filter is enabled by bit ECMB the Y/C signals coming from the comb filter are automatically selected. This is indicated via bit CMB in output status byte 02 (D5). For signals which cannot be combed (such as SECAM or black-to-white signals) the Y/C signals coming from the comb filter are not selected.

Chrominance and luminance processing

The circuits contain a chrominance band-pass, a SECAM cloche filter and a chrominance trap circuit. The filters are realized by means of gyrator circuits and they are automatically calibrated by comparing the tuning frequency with the crystal frequency of the decoder. The luminance delay line is also realized by means of gyrator circuits. The centre frequency of the chrominance band-pass filter is switchable via the I²C-bus so that the performance can be optimized for ‘front-end’ signals and external CVBS signals.

The luminance output signal which is derived from the incoming CVBS or Y/C signal can be varied in amplitude by means of a separate gain setting control via the I²C-bus control bits GAI1 and GAI0. The gain variation which can be realized with these bits is –1 to +2 dB.

Colour decoder

The colour decoder can decode PAL, NTSC and SECAM signals. The PAL/NTSC decoder contains an alignment-free crystal oscillator with 4 separate pins for crystal connection, a killer circuit and two colour difference demodulators. The 90° phase shift for the reference signal is produced internally.

Because it is possible to connect 4 different crystals to the colour decoder, all colour standards can be decoded without external switching circuits. Which crystals are connected to the decoder must be indicated via the I²C-bus. The crystal connection pins which are not used must be left open-circuit.

The horizontal oscillator is calibrated by means of the crystal frequency of the colour PLL. For a reliable calibration it is very important that the crystal indication bits XA to XD are not corrupted. For this reason bits XA to XD can be read in the output bytes so that the software can check the I²C-bus transmission.

The IC contains an Automatic Colour Limiting (ACL) circuit which is switchable via the I²C-bus and prevents oversaturation occuring when signals with a high chrominance-to-burst ratio are received. The ACL circuit is designed such that it only reduces the chrominance signal and not the burst signal. This has the advantage that the colour sensitivity is not affected by this function. The ACL function is mainly intended for NTSC signals but it can also be used for PAL signals. For SECAM signals the ACL function should be switched off.

The SECAM decoder contains an auto-calibrating PLL demodulator which has two references: the 4.43 MHz subcarrier frequency which is obtained from the crystal oscillator which is used to tune the PLL to the desired free-running frequency and the band gap reference to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search or SECAM mode.

The circuit can also decode the PALplus helper signal and can insert the various reference signals: set-ups and timing signals which are required for the PALplus decoder ICs.

The baseband delay line (TDA4665 function) is integrated.

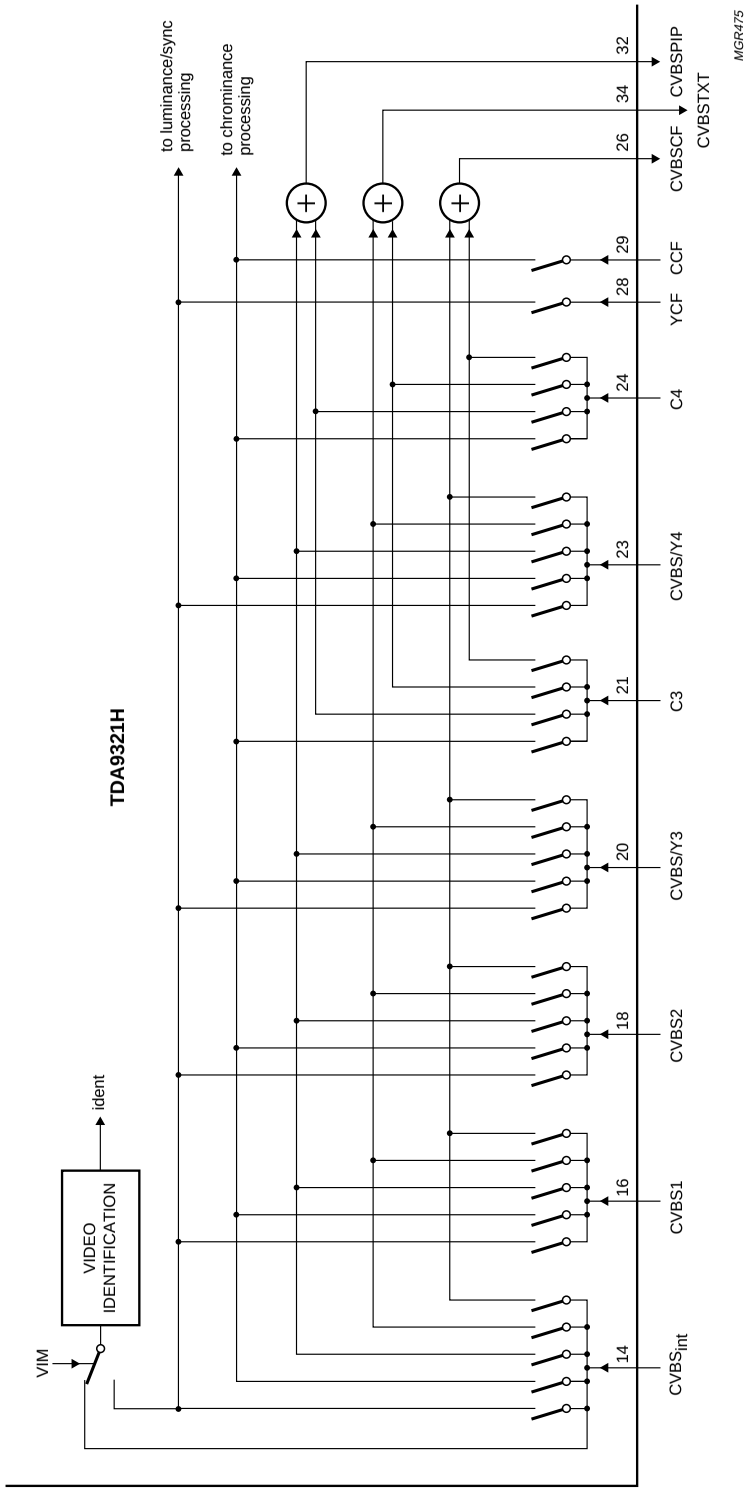


Fig.3 Video switches and interfacing of video ident.

RGB switch and matrix

The IC has 2 RGB inputs with fast switching. The switching of the various sourcing is controlled via the I²C-bus and the condition of the switch inputs can be read from the I²C-bus status bytes. If the RGB signals are not synchronous with the selected decoder input signal, an external clamp pulse has to be supplied to the HA/CLP input. The IC must be set in this mode via the I²C-bus. In that case the vertical pulse is suppressed by switching the VA output in a high-impedance off-state.

When an external RGB signal is mixed with the internal YUV signal it is necessary to switch-off the PALplus demodulation. To detect the presence of a fast blanking a circuit is added which forces bits MACP and HD to zero if a blanking pulse is detected in 2 consecutive lines. This system is chosen to prevent switching-off at every spike which is detected on the fast blanking input.

The IC has the possibility to use the RGB1 input as YUV input. This function can be enabled by means of bit YUV in subaddress 0A (D3). When switched to the YUV input the input signals must have the same amplitude and polarity as the YUV output signals. The Y signal has to be supplied to the GI1 input, the U signal to the BI1 input and the V signal to the RI1 input.

Synchronization circuit

The sync separator is preceded by a controlled amplifier which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage which operates at 50% of the amplitude. The separated sync pulses are fed to the phase detector and to the coincidence detector. This coincidence detector is used to detect whether the line oscillator is synchronized and can also be used for transmitter identification. This circuit can be made less sensitive with bit STM. This mode can be used during search tuning to avoid the tuning system stopping at very weak input signals. The PLL has a very high statical steepness so that the phase of the picture is independent of the line frequency.

For the horizontal output pulse 2 conditions are possible:

- An HA pulse which has a phase and width which is identical to the incoming horizontal sync pulse
- A clamp pulse (CLP) which has a phase and width which is identical to the clamp pulse in the sandcastle pulse.

The HA/CLP signal is generated by means of an oscillator which is running at a frequency of $440 \times f_{hor}$. Its frequency is divided by 440 to lock the first loop to the incoming signal. The time constant of the loop can be forced by the I²C-bus (fast or slow).

If required the IC can select the time constant depending on the noise content of the incoming video signal.

The free-running frequency of the oscillator is determined by a digital control circuit which is locked to the reference signal of the colour decoder. When the IC is switched on the HA/CLP is suppressed and the oscillator is calibrated as soon as all subaddress bytes have been sent. When the frequency of the oscillator is correct the HA/CLP signal is switched on again. When the coincidence detector indicates an out-of-lock situation the calibration procedure is repeated.

The VA pulse is obtained via a vertical count-down circuit. The count-down circuit has various windows depending on the incoming signal (50 or 60 Hz standard or non-standard). The count-down circuit can be forced in various modes via the I²C-bus. To obtain short switching times of the count-down circuit during a channel change the divider can be forced in the search window by means of bit NCIN.

I²C-BUS SPECIFICATION

The slave address of the IC is given in Table 1. Bit A1 is controlled via pin AS. When pin AS is connected to pin GND2 it is at logic 0 and when connected to V_{P2} it is at logic 1. When pin AS is left open-circuit it is connected to ground via an internal pull-up resistor. The circuit operates at clock frequencies of up to 400 kHz.

Table 1 Slave address bits

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	1/0	1	1/0

Start-up procedure

Read the status bytes until bit POR = 0 and send all subaddress bytes. It is advised to check the I²C-bus transmission by reading the output status bits SXA to SXD. This ensures a good operation of the calibration system of the horizontal oscillator. The horizontal output signal is switched on when the oscillator is calibrated.

Each time before the data in the IC is refreshed, the status bytes must be read. If bit POR = 1, then the procedure mentioned above must be carried out to restart the IC. When this procedure is not carried out the horizontal frequency may be incorrect after power-up or after a power dip.

The valid subaddresses are 00 to 0E. Subaddresses FE and FF are reserved for test purposes. Auto-increment mode is available for the subaddresses.

Inputs and outputs

Table 2 Input status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Colour decoder 0	00	CM3	CM2	CM1	CM0	XD	XC	XB	XA
Colour decoder 1	01	MACP	HOB	HBC	HD	FCO	ACL	CB	BPS
Luminance	02	0	0	GAI1	GAI0	YD3	YD2	YD1	YD0
Hue control	03	0	0	A5	A4	A3	A2	A1	A0
Spare	04	0	0	0	0	0	0	0	0
Synchronization 0	05	FORF	FORS	FOA	FOB	0	VIM	POC	VID
Synchronization 1	06	0	0	0	0	BSY	HO	EMG	NCIN
Spare	07	0	0	0	0	0	0	0	0
Video switches 0	08	0	0	0	ECMB	DEC3	DEC2	DEC1	DEC0
Video switches 1	09	0	PIP2	PIP1	PIP0	0	TXT2	TXT1	TXT0
RGB switch	0A	0	0	0	0	YUV	ECL	IE2	IE1
Output switches	0B	0	0	0	0	0	0	OS1	OS0
Vision IF	0C	FFI	IFO	GD	MOD	AFW	IFS	STM	VSW
Tuner takeover	0D	0	0	A5	A4	A3	A2	A1	A0
Adjustment IF-PLL	0E	L'FA	A6	A5	A4	A3	A2	A1	A0

INPUT CONTROL BITS

Table 3 Colour decoder mode

CM3	CM2	CM1	CM0	DECODER MODE	XTAL
0	0	0	0	PAL/NTSC/SECAM	A
0	0	0	1	PAL/NTSC	A
0	0	1	0	PAL	A
0	0	1	1	NTSC	A
0	1	0	0	SECAM	A
0	1	0	1	PAL/NTSC	B
0	1	1	0	PAL	B
0	1	1	1	NTSC	B
1	0	0	0	PAL/NTSC/SECAM	A/B/C/D
1	0	0	1	PAL/NTSC	C
1	0	1	0	PAL	C
1	0	1	1	NTSC	C
1	1	0	0	PAL/NTSC	A/B/C/D
1	1	0	1	PAL/NTSC	D
1	1	1	0	PAL	D
1	1	1	1	NTSC	D

Table 4 Crystal indication

XA to XD	CONDITION
0	crystal not present
1	crystal present; note 1

Note

1. When a comb filter is used, the various crystals must be connected to the IC as indicated in the pinning diagram. This is required because the ident system switches automatically to the comb filter when a signal is identified which can be combed (correct combination of colour standard and crystal frequency). For applications without comb filter only the crystal on pin XTALA is important (4.43 MHz); to pins XTALB to XTALD an arbitrary 3.5 MHz crystal can be connected.

Table 5 Motion Adaptive Colour Plus (MACP)

MACP	MODE
0	internal 4.43 MHz trap used
1	external MACP chrominance filtering used; 4.43 MHz trap bypassed and black set-up 200 mV; note 1

Note

1. The black set-up will only be present in a norm sync condition.

Table 6 Helper output blanking (PALplus/EDTV-2)

HOB	HBC	SNR	BLANKING
0	X(1)	X(1)	off
1	0	X(1)	on
1	1	0	off
1	1	1	on

Note

1. X = don't care.

Table 7 PALplus helper demodulation active

HD	CONDITIONS
0	off
1	on; PALplus mode with helper set-up 400 mV and black set-up 200 mV; note 1

Note

1. Black and helper set-up will only be present in a norm sync condition.

Table 8 Forced colour on

FCO	MODE
0	not active
1	active

Table 9 Automatic colour limiting

ACL	COLOUR LIMITING
0	not active
1	active

Table 10 Chrominance band-pass centre frequency

CB	CENTRE FREQUENCY
0	f_c
1	$1.1 \times f_c$

Table 11 Bypass of chrominance baseband delay line

BPS	DELAY LINE MODE
0	active
1	bypassed

Table 12 Gain luminance channel

GAI1	GAI0	GAIN SETTING
0	0	–1 dB
0	1	0 dB
1	0	+1 dB
1	1	+2 dB

Table 13 Y-delay adjustment; note 1

YD0 to YD3	Y-DELAY
YD3	YD3 × 160 ns +
YD2	YD2 × 160 ns +
YD1	YD1 × 80 ns +
YD0	YD0 × 40 ns

Note

1. For an equal delay of the luminance and chrominance signal the delay must be set at a value of 280 ns (YD3 to YD0 = 1011). This is only valid for a CVBS signal without group delay distortions.

Table 14 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto (60 Hz when line not synchronized)
0	1	forced 60 Hz; note 1
1	0	keep last detected field frequency
1	1	auto (50 Hz when line not synchronized)

Note

1. When switched to this mode the divider will directly switch to forced 60 Hz only.

Table 15 Phase 1 (φ_1) time constant; see also Table 57

FOA	FOB	MODE
0	0	normal
0	1	slow
1	0	slow or fast
1	1	fast

Table 16 Video ident mode

VIM	MODE
0	ident coupled to internal CVBS (pin 14)
1	ident coupled to selected CVBS

Table 17 Synchronization mode

POC	MODE
0	active
1	not active

Table 18 Video ident mode

VID	VIDEO IDENT MODE
0	φ_1 loop switched-on and off
1	not active

Table 19 Blanked sync on pin YO

BSY	CONDITIONS
0	unblanked sync; note 1
1	blanked sync

Note

1. Except for PALplus with black set-up.

Table 20 Condition of horizontal output

HO	CONDITIONS
0	clamp pulse available on pin HA/CLP
1	horizontal pulse available on pin HA/CLP

Table 21 Enable ‘Macrovision/subtitle’ gating

EMG	MODE
0	disable gating
1	enable gating

Table 22 Vertical divider mode

NCIN	VERTICAL DIVIDER MODE
0	normal operation
1	switched to search window

Table 23 Video switch control

ECMB[1]	DEC3	DEC2	DEC1	DEC0	SELECTED SIGNAL	SIGNAL TO COMB
0	0	0	0	X[2]	$CVBS_{int}$	$CVBS_{int}$
0	0	0	1	0	CVBS1	CVBS1
0	0	0	1	1	CVBS2	CVBS2
0	0	1	0	0	CVBS3	CVBS3
0	0	1	0	1	Y3/C3	Y3 + C3
0	0	1	1	0	CVBS4	CVBS4
0	0	1	1	1	Y4/C4	Y4 + C4
0	1	1	0	0	AUTO Y3/C3; note 3	CVBS3 or Y3 + C3
0	1	1	1	0	AUTO Y4/C4; note 3	CVBS4 or Y4 + C4
1	0	0	0	X[2]	YCF/CCF	$CVBS_{int}$
1	0	0	1	0	YCF/CCF	CVBS1
1	0	0	1	1	YCF/CCF	CVBS2
1	0	1	0	0	YCF/CCF	CVBS3
1	0	1	1	0	YCF/CCF	CVBS4
1	1	1	0	0	AUTO COMB3; note 4	CVBS3 or Y3 + C3
1	1	1	1	0	AUTO COMB4; note 4	CVBS4 or Y4 + C4

Notes

1. When bit ECMB = 1 the subcarrier frequency is present on pin 30. The YCF and CCF signals coming from the comb filter are only switched on when a signal is received that can be combed.
2. X = don't care.
3. AUTO YC means the decoder switches between CVBS and Y/C depending on the presence of the burst signal on these signals.
4. AUTO COMB means the decoder switches to Y/C mode if the burst is present on the C input and to the comb filter output if the burst is present on the CVBS signal.

Table 24 Video switch outputs

TXT2 PIP2	TXT1 PIP1	TXT0 PIP0	OUTPUT SIGNAL TXT OUTPUT SIGNAL PIP
0	0	–	$CVBS_{int}$
0	1	0	CVBS1
0	1	1	CVBS2
1	0	0	CVBS3
1	0	1	Y3 + C3
1	1	0	CVBS4
1	1	1	Y4 + C4

Table 25 Enable YUV input (on RGB1 input)

YUV	MODE
0	RGB1 input active
1	YUV input active

Table 26 External RGB clamp mode

ECL	MODE
0	off; internal clamp pulse used
1	on; external clamp pulse has to be supplied to pin HA/CLP

Table 27 Enable fast blanking RGB1

IE1	FAST BLANKING
0	not active
1	active

Table 28 Enable fast blanking RGB2

IE2	FAST BLANKING
0	not active
1	active

Table 29 Output switches OS0 and OS1

OS0; OS1	CONDITIONS
0	output = LOW
1	output = HIGH

Table 30 Fast filter IF-PLL

FFI	CONDITIONS
0	normal time constant
1	fast time constant

Table 31 IF circuit not active

IFO	MODE
0	normal operation of IF amplifier
1	IF amplifier switched off

Table 32 Group delay correction

GD	GROUP DELAY CHARACTERISTIC
0	flat
1	according to BG standard

Table 33 Modulation standard

MOD	MODULATION
0	negative
1	positive

Table 34 AFC window

AFW	AFC WINDOW
0	normal
1	enlarged

Table 35 IF sensitivity

IFS	IF SENSITIVITY
0	normal
1	reduced

Table 36 Search tuning mode

STM	MODE
0	normal operation
1	reduced sensitivity of video ident circuit

Table 37 Video mute

VSW	STATE
0	normal operation
1	VIF signal switched off

Table 38 PLL demodulator frequency shift

L'FA	MODE
0	normal IF frequency
1	frequency shift for L' standard

Table 39 Output status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	X[1]	X[1]	X[1]	SNR	FSI	SL	IVW
	01	CD3	CD2	CD1	CD0	SXD	SXC	SXB	SXA
	02	IN1	IN2	CMB	YC	S2A	S2B	S1A	S1B
	03	ID3	ID2	ID1	ID0	IFI	PL	AFA	AFB

Note

1. X = don't care.

OUTPUT CONTROL BITS

Table 40 Power-on reset

POR	MODE
0	normal
1	power-down

Table 41 Signal-to-noise ratio of sync signal

SNR	SIGNAL-TO-NOISE RATIO
0	S/N > 20 dB
1	S/N < 20 dB

Table 42 Field frequency indication

FSI	FREQUENCY
0	50 Hz
1	60 Hz

Table 43 Phase 1 (φ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 44 Condition vertical divider

IVW	STANDARD VIDEO SIGNAL
0	no standard video signal
1	standard video signal in 'narrow window' or standard TV norm (525 or 625 lines)

Table 45 Crystal indication (SXA to SXD)

SXA to SXD	CONDITIONS
0	no crystal connected
1	crystal connected

Table 46 Colour decoder mode

CD3	CD2	CD1	CD0	STANDARD	XTAL
0	0	0	0	no colour standard identified	A/B/C/D
0	0	0	1	NTSC	A
0	0	1	0	PAL	A
0	0	1	1	NTSC	B
0	1	0	0	PAL	B
0	1	0	1	NTSC	C
0	1	1	0	PAL	C
0	1	1	1	NTSC	D
1	0	0	0	PAL	D
1	0	0	1	SECAM	A
1	0	1	0	illegal forced mode; note 1	–

Note

1. This mode is generated when trying (e.g. via software control) to force the decoder to a standard with a crystal which is not connected to the IC.

Table 47 Indication RGB1/RGB2 insertion

IN1; IN2	RGB INSERTION
0	no insertion
1	full insertion

Table 48 Condition YCF/CCF inputs from comb filter

CMB	CONDITION YCF/CCF INPUTS
0	not selected
1	selected

Table 49 Input signal condition; note 1

YC	CONDITIONS
0	CVBS signal available
1	Y/C signal available

Note

1. During the search mode for the colour system, bit YC will indicate logic 1.

Table 50 Condition of AV1 and AV2 inputs

S1A; S2A	S1B; S2B	CONDITIONS
0	0	no external source
0	1	external source with 4 : 3 input signal
1	0	external source with 16 : 9 input signal

Table 51 Output video identification

IFI	VIDEO SIGNAL
0	no video signal identified
1	video signal identified

Table 52 In-lock indication IF-PLL

PL	CONDITIONS
0	PLL not locked
1	PLL locked

Table 53 AFC output

AFA	AFB	CONDITIONS
0	0	outside window; too low
0	1	outside window; too high
1	0	in window; below reference
1	1	in window; above reference

Table 54 IC version indication

ID3	ID2	ID1	ID0	IC TYPE
0	0	0	1	TDA9321HN1
1	0	0	1	TDA9321HN2

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage on pins V_{P1} and V_{P2}		–	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–25	+70	°C
T_{sld}	soldering temperature	for 5 s	–	260	°C
T_j	junction temperature		–	150	°C
V_{es}	electrostatic handling on all pins	notes 1 and 2	–3000	+3000	V
		notes 1 and 3	–300	+300	V

Notes

1. All pins are protected against ESD by means of internal clamping diodes.
2. Human Body Model (HBM): R = 1.5 kΩ; C = 100 pF.
3. Machine Model (MM): R = 0 Ω; C = 200 pF.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	50	K/W

QUALITY SPECIFICATION

Quality specification in accordance with *"SNW-FQ-611E"*.

Latch-up performance

At an ambient temperature of 70 °C all pins meet the following specification:

- Positive stress test: $I_{trigger} \geq 100$ mA or $V_{pin} \geq 1.5 \times V_{P(max)}$
- Negative stress test: $I_{trigger} \leq -100$ mA or $V_{pin} \leq -0.5 \times V_{P(max)}$.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{P1} and V_{P2}); note 1						
V_P	supply voltage (pins V_{P1} and V_{P2})		7.2	8.0	8.8	V
I_P	supply current (pins V_{P1} and V_{P2})		–	120	140	mA
P_{tot}	total power dissipation		–	960	–	mW
Vision IF circuit						
VISION IF AMPLIFIER INPUTS (PINS VIF1 AND VIF2)						
$V_{i(rms)}$	input sensitivity (RMS value)	note 2				
		$f_{i(VIF)}$ = 38.90 MHz	–	35	100	µV
		$f_{i(VIF)}$ = 45.75 MHz	–	35	100	µV
		$f_{i(VIF)}$ = 58.75 MHz	–	40	100	µV
$V_{i(max)(rms)}$	maximum input signal (RMS value)		150	200	–	mV
$R_{i(dif)}$	differential input resistance	note 3	–	2	–	kΩ
$C_{i(dif)}$	differential input capacitance	note 3	–	3	–	pF
ΔG_v	voltage gain control range		70	75	80	dB
PLL DEMODULATOR (PLL FILTER ON PIN VIFPLL); note 4						
f_{PLL}	PLL frequency range		32	–	60	MHz
$f_{cr(PLL)}$	PLL catching range		2.0	2.7	3.3	MHz
$t_{acq(PLL)}$	PLL acquisition time		–	–	20	ms
$\Delta f_{VCO}/\Delta T$	VCO frequency dependency with temperature	notes 5 and 6	–	–	$\pm 20 \times 10^{-6}$	K^{-1}
$f_{tune(VCO)}$	VCO tuning frequency range	via I²C-bus	3.0	3.7	4.2	MHz
Δf_{DAC}	frequency variation per step of the DAC (A0 to A6)		23	29	33	kHz
f_{shift}	frequency shift	with bit L'FA	–	5.5	–	MHz
VIDEO AMPLIFIER OUTPUT (PIN VIFO); note 7						
$V_{o(z)}$	zero signal output level	note 8				
		negative modulation	4.6	4.7	4.8	V
		positive modulation	1.9	2.0	2.1	V
$V_{o(ts)}$	top-sync level	negative modulation	1.9	2.0	2.1	V
$V_{o(w)}$	white level	positive modulation	4.4	4.5	4.6	V
ΔV_o	difference in amplitude between negative and positive modulation		–	0	15	%
$Z_{o(v)}$	video output impedance		–	50	–	Ω
$I_{bias(int)}$	internal bias current of NPN emitter follower output transistor		1.0	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{source(max)}$	maximum source current		–	–	5	mA
$B_{v(-3dB)}$	−3 dB bandwidth of demodulated output signal		6	8	10	MHz
G_{dif}	differential gain	note 9	–	–	1.5	%
φ_{dif}	differential phase	notes 6 and 9	–	–	2.5	deg
NL_{vid}	video non-linearity	note 10	–	2.5	5	%
V_{clamp}	white spot clamping level		–	6.0	–	V
N_{clamp}	noise inverter clamping level	note 11	–	1.5	–	V
N_{ins}	noise inverter insertion level (identical to black level)	note 11	–	2.7	–	V
d_{blue}	intermodulation at ‘blue’	notes 6 and 12				
		f = 0.92 or 1.1 MHz	60	66	–	dB
		f = 2.66 or 3.3 MHz	60	66	–	dB
d_{yellow}	intermodulation at ‘yellow’	notes 6 and 12				
		f = 0.92 or 1.1 MHz	56	62	–	dB
		f = 2.66 or 3.3 MHz	60	66	–	dB
S/N_W	weighted signal-to-noise ratio	notes 6 and 13	56	60	65	dB
S/N_{UW}	unweighted signal-to-noise ratio	notes 6 and 13	49	53	–	dB
ΔV_{rc}	residual carrier signal	note 6	–	5.5	–	mV
$\Delta V_{rc(2H)}$	2nd harmonic of residual carrier signal	note 6	–	2.5	–	mV
PSRR	power supply ripple rejection	at the output	–	40	–	dB
VIF AND TUNER AGC; note 14						
Timing of VIF-AGC with a 2.2 µF capacitor (pin DEC_{VIF})						
MVI	modulated video interference	60% AM for 1 to 100 mV; 0 to 200 Hz; system B/G	–	–	10	%
t_{res}	response time	VIF input signal amplitude increase of 52 dB; positive and negative modulation	–	2	–	ms
		VIF input signal amplitude decrease of 52 dB				
		negative modulation	–	50	–	ms
		positive modulation	–	100	–	ms
I_L	leakage current of the capacitor on pin 4	negative modulation	–	–	10	µA
		positive modulation	–	–	200	nA
$\Delta V_{o(v)}$	change in video output signal amplitude over 1 vertical period for peak white AGC at positive modulation	capacitor on pin 4 is 0.5 µF	–	–	2	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner takeover point adjustment (via I²C-bus)						
$V_{strt(min)(rms)}$	minimum start level (RMS value)		–	0.4	0.8	mV
$V_{strt(max)(rms)}$	maximum start level (RMS value)		100	150	–	mV
$\Delta V_{max}/T$	maximum variation with temperature	T_{amb} = 0 to 70 °C	–	6	8	dB
Tuner control output (pin TAGC)						
$V_{o(max)}$	maximum output voltage	maximum tuner gain; note 3	–	–	9	V
$V_{o(sat)}$	output saturation voltage	minimum tuner gain; I_o = 2 mA	–	–	300	mV
$I_{o(max)}$	maximum output current swing		5	–	–	mA
I_L	leakage current	for RF AGC	–	–	1	µA
ΔV_i	input signal variation	for complete tuner control	0.5	2	4	dB
AFC OUTPUT (VIA I²C-BUS); note 15						
RES_{AFC}	AFC resolution		–	2	–	bits
Δf_w	window sensitivity	normal window mode	65	80	100	kHz
		enlarged window mode	195	240	300	kHz
VIDEO IDENTIFICATION OUTPUT (VIA I²C-BUS)						
t_d	delay time	for identification after the AGC has stabilized on a new transmitter	–	–	10	ms
Sound IF circuit						
SOUND IF AMPLIFIER (PINS SIF1 AND SIF2)						
$V_{i(rms)}$	input sensitivity (RMS value)	FM mode (–3 dB)	–	30	70	µV
		AM mode (–3 dB)	–	70	100	µV
$V_{i(max)(rms)}$	maximum input signal (RMS value)	FM mode	50	70	–	mV
		AM mode	80	140	–	mV
$R_{i(dif)}$	differential input resistance	note 3	–	2	–	kΩ
$C_{i(dif)}$	differential input capacitance	note 3	–	3	–	pF
ΔG_v	voltage gain control range		64	–	–	dB
$\alpha_{ct(SIF-VIF)}$	crosstalk between inputs SIF and VIF		50	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
QSS AND AM SOUND OUTPUT (PIN QSS/AM)						
General						
R_o	output resistance		–	–	250	Ω
V_O	DC output voltage		–	3.3	–	V
$I_{bias(int)}$	internal bias current of emitter follower		0.7	1.0	–	mA
$I_{sink(max)}$	maximum AC and DC sink current		–	0.7	–	mA
$I_{source(max)}$	maximum AC and DC source current		–	2.0	–	mA
QSS output signal						
$V_{o(rms)}$	output signal amplitude (RMS value)	SC1 on; SC2 off	75	100	125	mV
B_{-3dB}	−3 dB bandwidth		7.5	9	–	MHz
$\Delta V_{r(SC)(rms)}$	residual IF sound carrier (RMS value)		–	2	–	mV
S/N_W	weighted signal-to-noise ratio (SC1/SC2)	ratio of PC/SC1 at VIF input of 40 dB or higher; note 16				
		black picture	53/48	58/55	–	dB
		white picture	52/47	55/53	–	dB
		6 kHz sine wave (black-to-white modulation)	44/42	48/46	–	dB
		250 kHz sine wave (black-to-white modulation)	44/25	48/30	–	dB
		SC subharmonics (f = 2.75 MHz ±3 kHz)	45/44	51/50	–	dB
		SC subharmonics (f = 2.87 MHz ±3 kHz)	46/45	52/51	–	dB
AM output signal						
$V_{o(rms)}$	output signal amplitude (RMS value)	54% modulation	400	500	600	mV
THD	total harmonic distortion		–	0.5	1.0	%
B_{-3dB}	−3 dB bandwidth		100	125	–	kHz
S/N_W	weighted signal-to-noise ratio		47	53	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video switches and comb filter interface						
VIDEO SWITCHES FOR CVBS, Y AND C SIGNALS						
Signal on pins $CVBS_{int}$, CVBS1, CVBS2, CVBS/Y3 and CVBS/Y4						
$V_{i(n)(p-p)}$	input voltage (peak-to-peak value)	note 17	–	1.0	1.43	V
$I_{i(n)}$	input current		–	4	–	μA
$Z_{source(max)}$	maximum source impedance		–	–	1.0	kΩ
$\alpha_{sup(n)}$	suppression of non-selected signals	f_i = 0 to 5 MHz; note 6	50	–	–	dB
Signal on pins C3 and C4						
$V_{i(n)(p-p)}$	input voltage (peak-to-peak value)	notes 3 and 18	–	0.3	1.0	V
$Z_{i(n)}$	input impedance		–	50	–	kΩ
Signal on pin CVBSTXT						
$V_{o(p-p)}$	output signal amplitude (peak-to-peak value)		1.6	2.0	2.4	V
V_{bl}	black level		–	2.6	–	V
$\Delta V_{bl}/\Delta T$	black level dependency with temperature		–	4	–	mV/K
Z_o	output impedance		–	–	250	Ω
Signal on pin CVBSPIP						
$V_{o(p-p)}$	output signal amplitude (peak-to-peak value)		0.8	1.0	1.2	V
V_{bl}	black level		–	3.6	–	V
$\Delta V_{bl}/\Delta T$	black level dependency with temperature		–	9	–	mV/K
Z_o	output impedance		–	–	250	Ω
COMB FILTER INTERFACE; note 19						
Signal on pin CVBSCF						
$V_{o(p-p)}$	output signal amplitude (peak-to-peak value)		0.8	1.0	1.2	V
Z_o	output impedance		–	–	250	Ω
V_{bl}	black level		–	3.6	–	V
$\Delta V_{bl}/\Delta T$	black level dependency with temperature		–	9	–	mV/K
Signal on pin YCF						
$V_{i(p-p)}$	input voltage (peak-to-peak value)		–	1.0	1.43	V
I_i	input current		–	4	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Signal on pin CCF						
V_i	input voltage	burst amplitude	–	0.3	1.0	V
Z_i	input impedance		–	50	–	kΩ
Reference signal output (pin REFO); note 20						
$V_{o(p-p)}$	output signal amplitude (peak-to-peak value)	C_L = 15 pF	0.2	0.25	0.3	V
$V_{O(en)}$	DC output level to enable comb filter		4.0	4.2	4.6	V
$V_{O(dis)}$	DC output level to disable comb filter		–	0.1	1.4	V
Switching levels of SYS1 and SYS2 outputs (pins SYS1 and SYS2); note 21						
V_{OH}	HIGH-level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW-level output voltage		–	0.1	0.4	V
$I_{o(sink)}$	output sink current		2	–	–	mA
$I_{o(source)}$	output source current		2	–	–	mA
DETECTION OF STATUS LEVELS OF SCART PLUG PIN 8; note 22						
$V_{det(int-ext)}$	detection voltage between internal and external (16 : 9) source		2.0	2.2	2.4	V
$V_{det(ext-ext)}$	detection voltage between external (16 : 9) and external (4 : 3) source		5.3	5.5	5.7	V
R_i	input resistance		60	100	–	kΩ
Chrominance and luminance filters and delay lines						
CHROMINANCE TRAP CIRCUIT; note 23						
f_{trap}	trap frequency			f_{osc} ±1%		MHz
		during SECAM reception		4.3 ±1.5%		MHz
B_{-3dB}	−3 dB bandwidth	f_{SC} = 3.58 MHz	2.6	2.8	3.0	MHz
		f_{SC} = 4.43 MHz	3.2	3.4	3.6	MHz
		during SECAM reception	2.9	3.1	3.3	MHz
CSR	colour subcarrier rejection		26	–	–	dB
CHROMINANCE BAND-PASS CIRCUIT						
f_c	centre frequency	bit CB = 0	–	f_{osc}	–	MHz
		bit CB = 1	–	$1.1f_{osc}$	–	MHz
Q_{bp}	band-pass quality factor		–	3	–	
CLOCHE FILTER						
f_c	centre frequency		4.26	4.29	4.31	MHz
B	bandwidth		241	268	295	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Y-DELAY LINE						
t_d	delay time	bits YD3 to YD0 = 1011; note 6				
		crystal A	490	520	550	ns
		crystal B, C or D	530	560	590	ns
$t_{d(tr)}$	tuning range delay time	with respect to 520/560 ns; 12 settings; see Table 13	–280	–	+160	ns
B	bandwidth	note 6	8	–	–	MHz
GROUP DELAY CORRECTION (PINS GDI AND GDO); note 24						
$V_{i(GDI)(p-p)}$	input signal amplitude on pin GDI (peak-to-peak value)		–	2.0	–	V
$I_{i(GDI)}$	input current on pin GDI		–	0.1	1.0	μA
$V_{o(GDO)(p-p)}$	output signal amplitude on pin GDO (peak-to-peak value)		1.8	2.0	2.2	V
$V_{o(GDO)}$	output top-sync level on pin GDO		–	2.4	–	V
$\Delta V_{o(GDO)}/\Delta T$	top-sync level on pin GDO variation with temperature		–	5	–	mV/K
$Z_{o(GDO)}$	output impedance on pin GDO		–	–	250	Ω
Colour demodulation part						
CHROMINANCE AMPLIFIER						
CR_{ACC}	ACC control range	note 25	26	–	–	dB
$\Delta V_{o(CRACC)}$	change in amplitude of the output signals over CR_{ACC}		–	–	2	dB
$TH_{ck(on)}$	threshold colour killer ON	colour killer from OFF to ON	–40	–	–35	dB
$hys_{ck(off)}$	hysteresis colour killer OFF	note 6				
		strong signal; S/N ≥ 40 dB	–	3	–	dB
		noisy input signals	–	1	–	dB
ACL CIRCUIT; note 26						
C/C_{ACL}	ACL chrominance burst ratio	when the ACL starts to operate	–	3.0	–	
REFERENCE PART						
Phase-locked loop; note 27						
f_{cr}	catching range		±360	±600	–	Hz
$\Delta\varphi$	phase shift	for a ±400 Hz deviation of the oscillator frequency; note 6	–	–	2	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
TC_{fosc}	temperature coefficient of oscillator frequency	note 6	–	–	1	Hz/K
$\Delta f_{osc}/V_P$	oscillator frequency variation with respect to the supply voltage	V_P = 8 V ±10%; note 6	–	–	25	Hz
$R_{neg(min)}$	minimum negative resistance		–	–	1.0	kΩ
$C_{L(max)}$	maximum load capacitance		–	–	15	pF
HUE CONTROL; note 28						
CR_{hue}	hue control range	63 steps; see Fig.4	±35	±40	–	deg
$\Delta hue/\Delta V_P$	hue dependency with respect to the supply voltage	V_P ±10%; note 6	–	0	–	deg
$\Delta hue/\Delta T$	hue dependency with temperature	T_{amb} = 0 to 70 °C; note 6	–	0	–	deg
DEMODULATORS						
General						
$\Delta V/\Delta V$	spread of signal amplitude ratio between standards	note 6	–1	–	+1	dB
PAL/NTSC demodulator						
$G_{(B-Y)(R-Y)}$	gain between both demodulators (B – Y) and (R – Y)		1.60	1.78	1.96	
$B_{-3dB(dem)}$	–3 dB bandwidth of demodulators	note 29	–	650	–	kHz
$\Delta V_{o(rc)(p-p)}$	residual carrier output (peak-to-peak value)	f = f_{osc}; (R – Y) output	–	–	5	mV
		f = f_{osc}; (B – Y) output	–	–	5	mV
		f = $2f_{osc}$; (R – Y) output	–	–	5	mV
		f = $2f_{osc}$; (B – Y) output	–	–	5	mV
$RR_{H/2(p-p)}$	H/2 ripple rejection (peak-to-peak value)	at (R – Y) output	–	–	25	mV
$\Delta V_o/T$	output voltage variation with temperature	note 6	–	0.1	–	%/K
$\Delta V_o/V_P$	output voltage variation with respect to the supply voltage	note 6	–	–	0.3	dB/V
φ_e	phase error in the demodulated signals	note 6	–	–	±5	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SECAM demodulator						
f_{blos}	black level offset frequency		–	–	7	kHz
f_{blos}/T	black level offset frequency variation with temperature		–	–	60	Hz/K
f_p	pole frequency of de-emphasis		77	85	93	kHz
f_p/f_z	ratio pole and zero frequency		–	3	–	
NL	non-linearity		–	–	3	%
V_{cal}	calibration voltage		3	4	5	V
Baseband delay line						
ΔV_o	variation of output signal	for adjacent time samples at constant input signals	–0.1	–	0.1	dB
$\Delta V_{r(clk)(p-p)}$	residual clock signal (peak-to-peak value)		–	–	5	mV
t_d	delay	delayed signal	63.94	64.0	64.06	µs
		non-delayed signal	40	60	80	ns
ΔV_o	difference in output amplitude	when delay line is bypassed or not (with bit BPS)	–	–	5	%
PALplus helper demodulator						
$V_{o(helper)(p-p)}$	helper output voltage (peak-to-peak value)		610	686	770	mV
$V_{su(helper)}$	helper set-up amplitude	only helper lines 22 and 23	380	400	420	mV
$t_{d(g)}$	group delay	within pass band	–	–	10	ns
$\varphi_{e(dem)}$	demodulation phase error	including H/2 phase error	–	–	5	deg
α_{sup}	suppression	for modulated helper in demodulated 0 to 1 MHz signal	–36	–	–	dB
ΔV_r	residual signal	at 4.43 MHz signal	–36	–	–	dB
THD	total harmonic distortion	in ACC	–36	–	–	dB
$t_{o(helper-Y)}$	helper output timing to Y output		–	–	10	ns
V_{offset}	offset voltage	for demodulated mid grey to inserted mid grey level; mid grey line 23 to line 22	–	–	5	mV
$t_{W(su)(helper)}$	helper set-up pulse width		–	52.8	–	µs
t_d	delay between mid sync of input and start of helper set-up	bits YD3 to YD0 = 1011; note 30	–	8.6	–	µs
	delay between start of black set-up and start of helper set-up	only lines 22 and 23	–	30.8	–	µs
$B_{helper(-3dB)}$	−3 dB bandwidth of helper baseband		–	2.6	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB switch and YUV switch						
RGB SWITCH (PINS RI1 TO BI1 AND RI2 TO BI2)						
$V_{i(p-p)}$	input signal amplitude (peak-to-peak value)		–	0.7	1.0	V
$Z_{source(max)}$	maximum source impedance		–	–	1.0	kΩ
$\Delta V_{bl(int-ext)}$	difference between black level of internal and external signals at the outputs		–	–	10	mV
I_i	input current	no clamping; note 3	–	0.1	1	μA
Δt_d	delay difference between the three channels	note 6	–	0	20	ns
YUV INPUTS (WHEN ACTIVATED)						
$V_{i(Y)(p-p)}$	Y input signal amplitude (peak-to-peak value)		–	1.0	–	V
$V_{i(U)(p-p)}$	U input signal amplitude (peak-to-peak value)		–	1.33	–	V
$V_{i(V)(p-p)}$	V input signal amplitude (peak-to-peak value)		–	1.05	–	V
$Z_{source(max)}$	maximum source impedance		–	–	1.0	kΩ
$\Delta V_{bl(int-ext)}$	difference between black level of internal and external signals at the outputs		–	–	10	mV
I_i	input current	no clamping; note 3	–	0.1	1	μA
FAST BLANKING (PINS RGB1 AND RGB2)						
V_i	input voltage	no data insertion	–	–	0.4	V
		data insertion	0.9	–	–	V
$V_{i(max)}$	maximum input pulse		–	–	3.5	V
I_i	input current		–	–	0.2	mA
$\Delta t_{d(blank-RGB)}$	delay difference between blanking and RGB signals	note 6	–	–	tbf	ns
$\alpha_{sup(int)}$	suppression of internal YUV signals	data insertion; f_i = 0 to 5 MHz; note 6	55	–	–	dB
$\alpha_{sup(ext)}$	suppression of external RGB signals	no data insertion; f_i = 0 to 5 MHz; note 6	55	–	–	dB
$t_{d(blank-YUV)}$	delay between blanking input and YUV outputs		–	–	tbf	ns
LUMINANCE OUTPUT (PIN YO); note 31						
$V_{o(p-p)}$	output signal amplitude (peak-to-peak value)	black-to-white	–	1.0	–	V
V_o	output voltage during PALplus	black-to-white	–	0.8	–	V
$\Delta V_{bl(YUV-RGB)}$	difference in black level between YUV and RGB mode		–	–	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_o	output impedance		–	–	250	Ω
V_O	output DC voltage level	black level	2.8	3.0	3.2	V
$B_{RGB(-3dB)}$	−3 dB bandwidth of the RGB switch circuit		7	–	–	MHz
S/N	signal-to-noise ratio	f_i = 0 to 5 MHz	–	52	–	dB
$V_{su(bl)}$	black set-up amplitude	bit MACP = 1 or bit HD = 1	190	200	210	mV
$t_{W(su)(bl)}$	black set-up pulse width		–	52.8	–	µs
t_d	delay between mid sync at input and black set-up	note 30	–	8.8	–	µs
V_{offset}	offset voltage	Y_{bl} to re-inserted black	–	–	10	mV
$G_{(Y/CVBS-YO)}$	gain from internal Y/CVBS to YO		1.35	1.43	1.50	
		bit MACP = 1 or bit HD = 1	1.08	1.14	1.20	
UO AND VO SIGNAL OUTPUTS (PINS UO AND VO)						
$V_{o(VO)(p-p)}$	output voltage on pin VO (peak-to-peak value)	standard EBU colour bar	0.88	1.05	1.25	V
$V_{o(UO)(p-p)}$	output voltage on pin UO (peak-to-peak value)	standard EBU colour bar	1.12	1.33	1.58	V
Z_o	output impedance		–	–	250	Ω
V_O	output DC voltage level		2.2	2.4	2.6	V
$\Delta V_{bl(YUV-RGB)}$	difference in black level between YUV and RGB mode		–	–	10	mV
COLOUR MATRIX FROM RGB TO YUV						
G	gain					
	from RI to YO		0.40	0.43	0.46	
	from GI to YO		0.79	0.84	0.90	
	from BI to YO		0.15	0.16	0.17	
	from RI to UO		0.40	0.43	0.46	
	from GI to UO		0.79	0.84	0.90	
	from BI to UO		1.19	1.27	1.35	
	from RI to VO		0.94	1.00	1.07	
	from GI to VO		0.79	0.84	0.90	
	from BI to VO		0.15	0.16	0.17	
Horizontal and vertical synchronization						
SYNC VIDEO INPUTS						
V_{sync}	sync pulse amplitude	note 3	35	300	350	mV
SL_{hor}	slicing level for horizontal sync	note 32	50	55	60	%
SL_{vert}	slicing level for vertical sync	note 32	35	40	45	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL OSCILLATOR						
f_{fr}	free-running frequency		–	15625	–	Hz
Δf_{fr}	spread on free-running frequency		–	–	±2	%
$\Delta f/\Delta V_P$	frequency dependency with respect to the supply voltage	V_P = 8.0 V ±10%; note 6	–	0.2	0.5	%
$\Delta f/T$	frequency variation with temperature	T_{amb} = 0 to 70 °C; note 6	–	–	80	Hz
FIRST CONTROL LOOP (PIN PH1LF); note 33						
$f_{hr(PLL)}$	PLL holding range		–	±0.9	±1.2	kHz
$f_{cr(PLL)}$	PLL catching range	note 6	±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio	for the video input signal at which the time constant is switched	15	17	19	dB
hys_{sw}	hysteresis at the switching point		2	3	4	dB
σ_φ	sigma value of phase jitter	in automatic mode; ±3 σ	–	–	5	ns
HORIZONTAL PULSE OUTPUT AND CLAMP PULSE INPUT/OUTPUT (PIN HA/CLP)						
Switched to HA output (bit HO = 1)						
V_{OH}	HIGH-level output voltage	$I_{o(source)}$ = 2 mA	4.0	5.0	5.5	V
V_{OL}	LOW-level output voltage	$I_{o(sink)}$ = 2 mA	–	0.2	0.4	V
$I_{o(sink)}$	output sink current		2	–	–	mA
$I_{o(source)}$	output source current		2	–	–	mA
t_W	pulse width	at nominal horizontal frequency	4.6	4.7	4.8	µs
t_d	delay between mid sync of input and mid HA pulse	note 30	0.3	0.45	0.6	µs
Switched to CLP output (bit HO = 0)						
t_W	pulse width	at nominal horizontal frequency	3.5	3.6	3.7	µs
t_{d1}	delay between start of CLP pulse to start of black set-up	bit HD = 1 or bit MACP = 1; bits YD3 to YD0 = 1011; at nominal horizontal frequency	5.2	5.3	5.4	µs
t_{d2}	delay between mid sync of input and start CLP pulse	note 30	3.0	3.2	3.4	µs
Switched to CLP input (bit ECL = 1)						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.4	–	5.5	V
$t_{W(clamp)}$	clamping pulse width		1.8	3.5	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta V_{(clamp)(n)}$	clamping offset between pins UO and VO		–	–	10	mV
Z_i	input impedance		3	–	–	MΩ
VERTICAL OSCILLATOR; note 34						
f_{fr}	free-running frequency	50 Hz mode	–	50	–	Hz
		60 Hz mode	–	60	–	Hz
f_{lock}	frequency locking range		45	–	64.5	Hz
D/D	divider ratio	not locked	–	625/525	–	lines
LR	locking range		488	–	722	lines/ frame
VERTICAL PULSE OUTPUT (PIN VA)						
V_{OH}	HIGH-level output voltage	$I_{o(source)}$ = 2 mA	4.0	5.0	5.5	V
V_{OL}	LOW-level output voltage	$I_{o(sink)}$ = 2 mA	–	0.2	0.4	V
$I_{o(sink)}$	output sink current		2	–	–	mA
$I_{o(source)}$	output source current		2	–	–	mA
t_W	pulse width	f_{VA} = 50 Hz	–	2.5	–	lines
		f_{VA} = 60 Hz	–	3.0	–	lines
t_d	delay between start of vertical sync of input and positive edge of vertical pulse on pin VA	note 35	–	37.7	–	µs
Z_o	output impedance	bit ECL = 1	3	–	–	MΩ
SANDCASTLE OUTPUT (PIN SCO)						
General						
V_z	zero level voltage		0	0.5	1.0	V
$I_{o(sink)}$	output sink current		–	0.5	–	mA
Horizontal/vertical blanking						
V_o	output voltage level		2.2	2.5	2.8	V
$I_{o(source)}$	output source current		–	0.7	–	mA
$t_{W(h)}$	horizontal blanking pulse width		–	10	–	µs
t_d	delay between start horizontal blanking and start clamping pulse		–	6.4	–	µs
Clamping pulse						
V_o	output voltage level		4.2	4.5	4.8	V
$I_{o(source)}$	output source current		–	0.7	–	mA
t_W	pulse width		–	3.6	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_d	delay between mid sync of input and start of clamping pulse	note 30	3.0	3.2	3.4	µs
I²C-BUS CONTROL						
SCL AND SDA INPUTS/OUTPUTS (PINS SCL AND SDA)						
V_i	input voltage range		0	–	5.5	V
V_{IL}	LOW-level input voltage		–	–	1.5	V
V_{IH}	HIGH-level input voltage		3.5	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–10	µA
I_{IH}	HIGH-level input current	V_{IH} = 5.5 V	–	–	10	µA
$V_{OL(SDA)}$	LOW-level output voltage on pin SDA	$I_{OL(SDA)}$ = 3 mA	–	–	0.4	V
SW0 AND SW1 OUTPUTS (PINS SW0 AND SW1); note 36						
V_{OH}	HIGH-level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW-level output voltage		–	0.2	0.4	V
$I_{O(sink)}$	output sink current		2	–	–	mA
$I_{O(source)}$	output source current		2	–	–	mA

Notes to the characteristics

1. The two supply pins V_{P1} and V_{P2} must be decoupled separately but they must be connected to a single power supply to avoid too big differences between them.
2. On set AGC.
3. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
4. Loop filter bandwidth B_{lpf} = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2; calculated with top sync level as f_{PLL} input signal level). LC-VCO circuit between pins 7 and 8: Q_0 = 60; C_{int} = 30 pF.
5. The optimum temperature stability of the PLL can be obtained when a TOKO coil as given in Table 55 is applied.
6. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
7. Measured at 10 mV (RMS value) top sync input signal.
8. So called projected zero point, i.e. with switched demodulator.
9. Measured in accordance with the test line given in Fig.5. For the differential phase test the peak white setting is reduced to 87%.

   The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.

   The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
10. This figure is valid for the complete video signal amplitude (peak white-to-black). See Fig.6.
11. The noise inverter is only active in the ‘strong signal mode’ (no noise detected in the incoming signal).

12. The input conditions and test set-up are given in Figs 8 and 9. The figures are measured with an input signal of 10 mV (RMS value). The intermodulation figures are defined:

    $\alpha_{0.92} = 20 \log\left(\frac{V_0 \text{ at } 3.58 \text{ MHz}}{V_0 \text{ at } 0.92 \text{ MHz}}\right) + 3.6$ dB ; $\alpha_{0.92}$ value at 0.92 MHz referenced to black or white signal;

    $\alpha_{2.76} = 20 \log\left(\frac{V_0 \text{ at } 3.58 \text{ MHz}}{V_0 \text{ at } 2.76 \text{ MHz}}\right)$; $\alpha_{2.76}$ value at 2.76 MHz referenced to colour carrier.

13. Measured at an input signal of 10 mV (RMS value). The S/N is the ratio of black-to-white amplitude with respect to the black level noise voltage (RMS value). B = 5 MHz. Weighted in accordance with CCIR 567.
14. The AGC response time also depends on the acquisition time of the PLL demodulator. The values given are valid when the PLL is in lock.
15. The AFC control voltage is obtained from the control voltage of the VCO of the PLL demodulator. The tuning information is supplied to the tuning system via the I²C-bus. Two bits are reserved for this function. The AFC value is valid only when bit PL = 1.
16. The weighted S/N ratio is measured under the following conditions:
    a) The VIF modulator must meet the following specifications:
       - Incidental phase modulation for black-to-white jumps less than 0.5 degrees.
       - QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 27 kHz) for 6 kHz sine wave black-to-white modulation.
       - Picture-to-sound carrier ratio: PC/SC1 = 13 dB (transmitter).

    b) The measurements must be carried out with the Siemens SAW filters G3962 for VIF and G9350 for SIF. Input level for SIF at 10 mV (RMS value) with 27 kHz deviation.

    c) The PC/SC ratio at the VIF input is calculated as the addition of the TV transmitter ratio and the SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N_W values as indicated.
17. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
18. Indicated is a signal for a colour bar with 75% saturation (chrominance to burst amplitude ratio = 2.2 : 1).
19. When a signal is identified which can be combed (correct combination of colour standard and reference crystal) the comb filter is switched to that mode via pins 25 and 27 and then the filter is activated by switching on the reference carrier signal and connecting the output signals of the comb filter (pins 28 and 29) to the video processing circuits.
20. The subcarrier output signal can be used as a reference signal for external comb filter ICs (e.g. SAA4961). When bit ECMB = 0 the subcarrier signal is suppressed and the DC level is LOW. When bit ECMB = 1 the output level is HIGH and the subcarrier signal is present.
21. The outputs SYS1 and SYS2 can be used to switch the comb filter to the different colour standards (e.g. PAL-M, PAL-N, PAL-B/G and NTSC-M) and are controlled by the colour decoder identification circuit.

    The setting of the outputs for the various standards is given in Table 56.
22. For the detection of the status of the incoming SCART signal a voltage divider with a ratio of 2 : 3 has to be connected between pin 8 of the SCART plug and the detection input. The impedance of the voltage divider should not be too high-ohmic because of the input impedance of 100 kΩ.
23. When the decoder is forced to a fixed subcarrier frequency (via bits XA to XD or bit CM) the chrominance trap is always switched on, also when no colour signal is identified. When 2 crystals are active the chrominance trap is switched off if no colour signal is identified.
24. The typical group delay characteristic for the B/G standard is given in Fig.7.
25. At a chrominance input voltage of 660 mV (p-p) [colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)] the dynamic range of the ACC is +6 and −20 dB.
26. The ACL function can be activated by bit ACL. The ACL circuit reduces the gain of the chrominance amplifier for input signals with a C/C_{ACL} which exceeds a value of 3.0.

27. All frequency variations are referenced to 3.58 or 4.43 MHz carrier frequency. All oscillator specifications are measured with the Philips crystal series 9922 520 with a series capacitance C_s = 18 pF. The oscillator circuit is rather insensitive to the spurious responses of the crystal. As long as the resonance resistance of the third overtone is higher than that of the fundamental frequency the oscillator will operate at the correct frequency. The typical crystal parameters for the crystal series are:

    a) Load resonance frequencies f_L: 4.433619, 3.579545, 3.582056 and 3.575611 MHz; C_s = 20 pF.

    b) Motional capacitance C_{mot} = 20.6 fF (4.43 MHz crystal) or C_{mot} = 14.7 fF (3.58 MHz crystal).

    c) Parallel capacitance C_p = 5.0 pF.

    The minimum detuning range can only be specified if both the IC and the crystal tolerances are known and therefore the figures regarding catching range are only valid for the specified crystal series. In this figure tolerances of the crystal with respect to the nominal frequency, motional capacitance and ageing have been taken into account and have been counted for gaussic addition. Whenever different typical crystal parameters are used the following equation might be helpful for calculating the impact on the tuning capabilities:

    $$\text{Detuning range} = \frac{C_{mot}}{\left(1 + \frac{C_p}{C_s}\right)^2}$$

    The resulting detuning range should be corrected for temperature shift and supply voltage deviation of both the IC and the crystal. To guarantee a catching range of ±300 Hz on 4.43 MHz the minimum motional capacitance of the crystal must have a value 13.2 fF or higher. For a catching range of 250 Hz with the 3.58 MHz crystal the minimum motional capacitance must have a value of 9 fF. The actual series capacitance in the application should be C_s = 18 pF to account for parasitic capacitances on-chip and off-chip.

28. The hue control is active for NTSC on the demodulated colour difference signals and for PALplus on the demodulated helper signal.

29. This parameter indicates the bandwidth of the complete chrominance circuit including the chrominance band-pass filter. The bandwidth of the low-pass filter of the demodulator is approximately 1 MHz.

30. This delay is partially caused by the low-pass filter at the sync separator input.

31. The internal luminance signal (signal which is derived from the incoming CVBS or Y/C signals) has a separate gain control setting (controlled by the I²C-bus bits GAI1 and GAI0 and with a gain variation between –1 and +2 dB) which can be used to get an optimal input signal amplitude for the feature box.

32. The slicing level is independent of sync pulse amplitude. The given percentage is the distance between the slicing level and the black level (back porch). When the amplitude of the sync pulse exceeds the value of 350 mV the sync separator will slice the sync pulse at a level of 175 mV above top sync. The maximum sync pulse amplitude is 4 V (peak-to-peak value).

33. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition and the condition of the I²C-bus. Therefore the circuit contains a noise detector and the time constant is switched to the slow mode when too much noise is present in the signal. In the fast mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible. Switching between the two modes can be automatic or overruled by the I²C-bus.

    The circuit contains a video identification circuit which is independent of the first control loop. This identification circuit can be used to close or open the first control loop when a video signal is present or not present on the input. This enables a stable On Screen Display (OSD) when just noise is present at the input. The coupling of the video identification circuit with the first control loop can be revoked via the I²C-bus.

To prevent the horizontal synchronization being disturbed by anti copy signals such as Macrovision the phase detector is gated during the vertical retrace period from line 11 to 17 (60 Hz signal) or from line 11 to 22 (50 Hz signal) so that pulses during scan have no effect on the output voltage. The width of the gate pulse is approximately 22 μs. During weak signal conditions (noise detector active) the gating is active during the complete scan period and the width of the gate pulse is reduced to 5.7 μs so that the effect of noise is reduced to a minimum.

The output current of the phase detector in the various conditions is shown in Table 57.

34. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 3 modes of operation:
    a) Search mode large window.

       This mode is switched on when the circuit is not synchronized or when a non-standard signal [number of lines per frame outside the range between 311 and 314 (50 Hz mode) or between 261 and 264 (60 Hz mode)] is received. In the search mode the divider can be triggered between line 244 and line 361 (approximately 43.3 to 64.5 Hz).

    b) Standard mode narrow window.

       This mode is switched on when more than 15 succeeding vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

    c) Standard TV-norm [divider ratio 525 (60 Hz) or 625 (50 Hz)].

       When the system is switched to the narrow window a check is performed to establish whether the incoming vertical sync pulses are in accordance with the TV-norm. When 15 standard TV-norm pulses are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.

       When 3 vertical sync pulses are missed the system switches back to the narrow window and when also in this window no sync pulses are found (condition 3 missing pulses) the system switches over to the search window.

    The vertical divider needs some waiting time during channel-switching of the tuner. When a fast reaction of the divider is required during channel-switching the system can be forced to the search window by means of bit NCIN in subaddress 06.

35. The delay between the positive edge of VA and the positive edge of CLP (≈ negative edge of HA) after VA is 32.0 μs for field 1 and 0 μs for field 2. Especially for PALplus signals the regenerated VA pulses must have a fixed and known phase relation to the undisturbed VA pulses of the incoming video signal. This relationship must remain correct as long as the vertical divider is in the standard mode (indirect sync mode). Therefore the coincidence window used here must be a half line window. With a well defined phase relationship of the generated VA pulses to the generated HA pulses a correct field identification and all the required timing signals referring to a certain line in each frame can be generated externally in the PALplus decoder environment.

36. Pins 19 and 22 are for general purpose outputs that can be used to switch external circuits e.g. sound traps, etc. They are controlled via the I²C-bus by bits OS0 (pin 19) and OS1 (pin 22).

Table 55 Coil data for the VIF-PLL demodulator (approximated coil values)

f_{VIF} (MHz)	f_{VCO} (MHz)	L (nH)	TOKO SAMPLE NUMBER	REMARKS
38.9	77.8	150	P369INAS-159HM	∅ 5 mm; 5 km long; TC = 30 ±100 ppm/°C
45.75	91.5	100	P369INAS-160HM	
58.75	117.5	70	P369INAS-161HM	

Table 56 Switching conditions of pins SYS1 and SYS2

COLOUR STANDARD	SYS1	SYS2	ACTIVE CRYSTAL
PAL-M	LOW	LOW	C
PAL-B, G, H, D and I	LOW	HIGH	A
NTSC-M	HIGH	LOW	D
PAL-N	HIGH	HIGH	B

Table 57 Output current of the phase detector in the various conditions

I²C-BUS COMMANDS				IC CONDITIONS			φ-1 CURRENT/MODE			
VID	POC	FOA	FOB	IDENT	COIN	NOISE	SCAN	V-RETR	GATING	MODE
–	0	0	0	yes	yes	no	180	270	no[1]	auto
–	0	0	0	yes	yes	yes	30	30	yes	auto
–	0	0	0	yes	no	–	180	270	no	auto
–	0	0	1	yes	yes	–	30	30	yes	slow
–	0	0	1	yes	no	–	180	270	no	slow
–	0	1	0	yes	yes	no	180	270	yes	fast
–	0	1	0	yes	yes	yes	30	30	yes	slow
–	–	1	1	–	–	–	180	270	no	fast
0	0	–	–	no	–	–	6	6	no	OSD
–	1	–	–	–	–	–	–	–	–	off

Note

1. When the Macrovision is active a gating is present during a part of the vertical retrace, pulse width 22 μs. In the other gating conditions the pulse width is 5.7 μs and the gating is continuous.

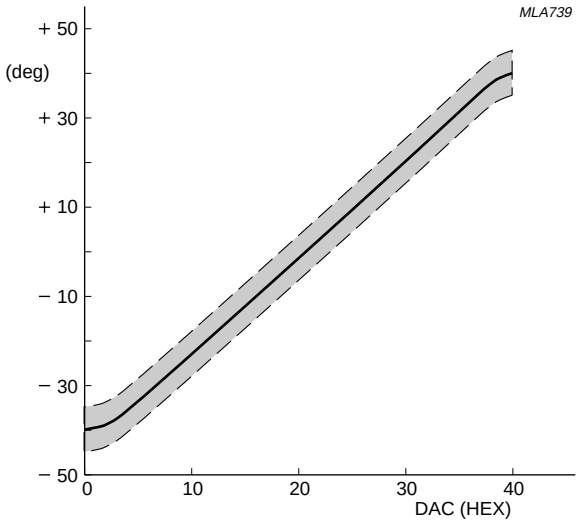


Fig.4 Hue control curve.

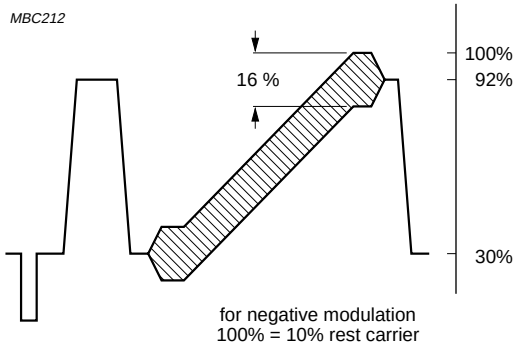


Fig.5 Video output signal.

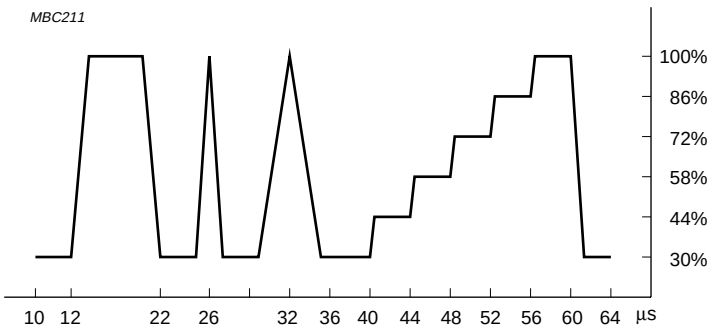


Fig.6 Test signal waveform.

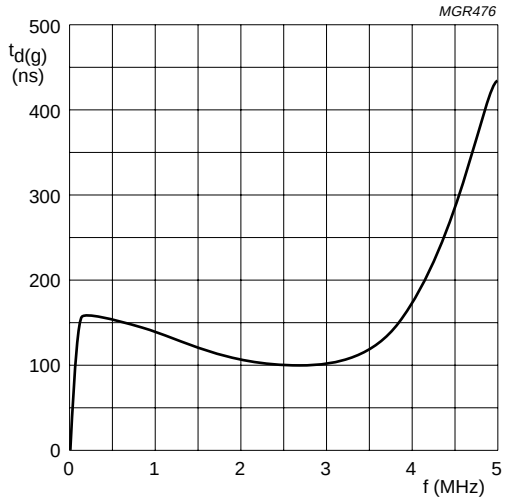
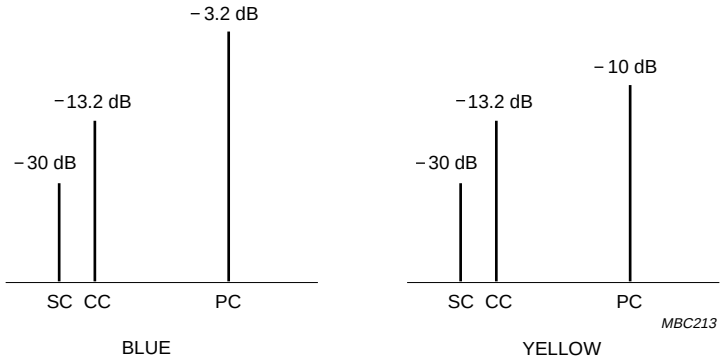


Fig.7 Group delay characteristic.



SC = sound carrier, with respect to top sync level.
CC = colour carrier, with respect to top sync level.
PC = picture carrier, with respect to top sync level.

Fig.8 Input signal conditions.

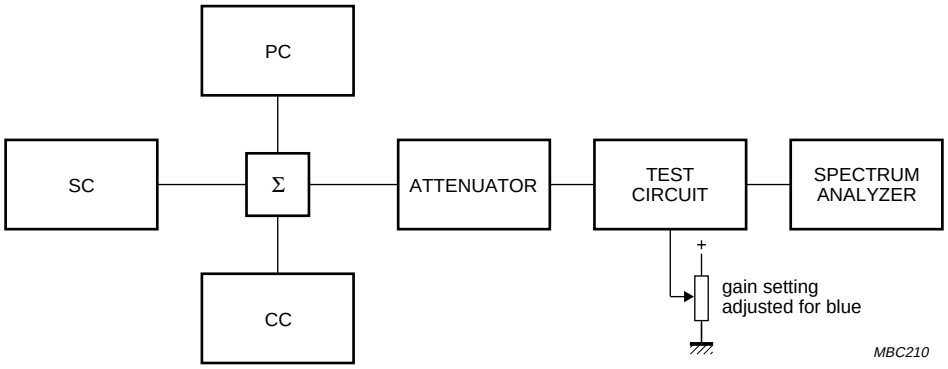


Fig.9 Test set-up intermodulation.

TEST AND APPLICATION INFORMATION

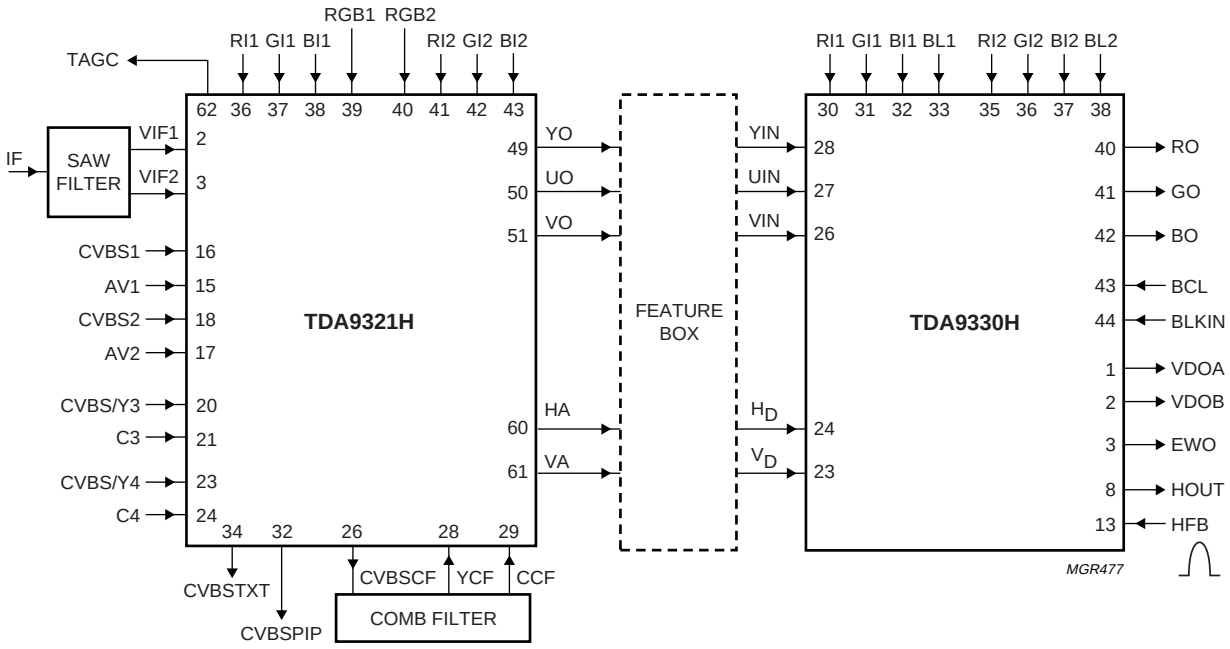
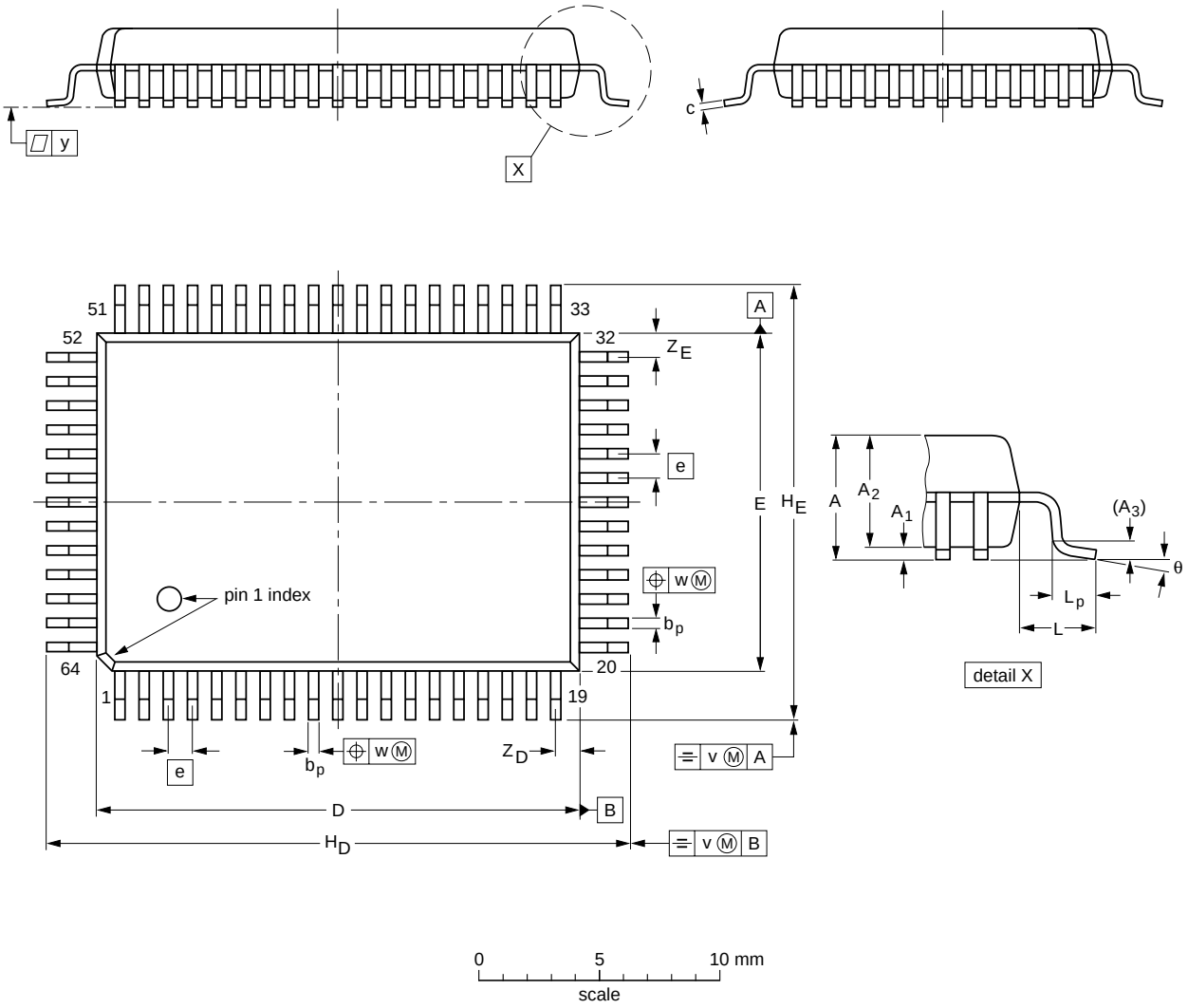


Fig.10 Application diagram.

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
HLQFP, HSQFP, HSOP, SMS	not suitable(2)	suitable
PLCC(3), SO	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SQFP	not suitable	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
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