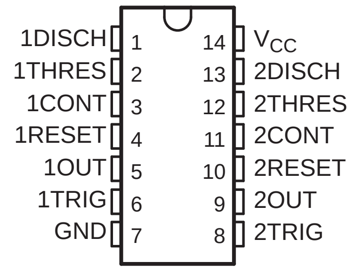
Jameco Part Number 904114

FEATURES

- **Two Precision Timing Circuits Per Package**
- **Astable or Monostable Operation**
- **TTL-Compatible Output Can Sink or Source up to 150 mA**
- **Active Pullup or Pulldown**
- **Designed to Be Interchangeable With Signetics NE556, SA556, and SE556**

NA556...D OR N PACKAGE
NE556...D, N, OR NS PACKAGE
SA556...D OR N PACKAGE
SE556...J PACKAGE
(TOP VIEW)



APPLICATIONS

- **Precision Timers From Microseconds to Hours**
- **Pulse-Shaping Circuits**
- **Missing-Pulse Detectors**
- **Tone-Burst Generators**
- **Pulse-Width Modulators**
- **Pulse-Position Modulators**
- **Sequential Timers**
- **Pulse Generators**
- **Frequency Dividers**
- **Application Timers**
- **Industrial Controls**
- **Touch-Tone Encoders**

DESCRIPTION/ORDERING INFORMATION

These devices provide two independent timing circuits of the NA555, NE555, SA555, or SE555 type in each package. These circuits can be operated in the astable or the monostable mode with external resistor-capacitor (RC) timing control. The basic timing provided by the RC time constant can be controlled actively by modulating the bias of the control-voltage input.

The threshold (THRES) and trigger (TRIG) levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by using the control voltage (CONT) terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset, and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between the discharge (DISCH) terminal and ground (GND).

ORDERING INFORMATION

T_A	V_T (MAX) V_{CC} = 15 V	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	11.2 V	PDIP – N	Tube of 25	NE556N	NE556N
		SOIC – D	Tube of 50	NE556D	NE556
			Reel of 2500	NE556DR	
		SOP – NS	Reel of 2000	NE556NSR	NE556
–40°C to 85°C	11.2 V	PDIP – N	Tube of 25	SA556N	SA556N
–40°C to 105°C	11.2 V	PDIP – N	Tube of 25	NA556N	NA556N
		SOIC – D	Tube of 50	NA556D	NA556
			Reel of 2500	NA556DR	
–55°C to 125°C	10.6 V	CDIP – J	Tube of 25	SE556J	SE556J
				SE556JB	SE556JB

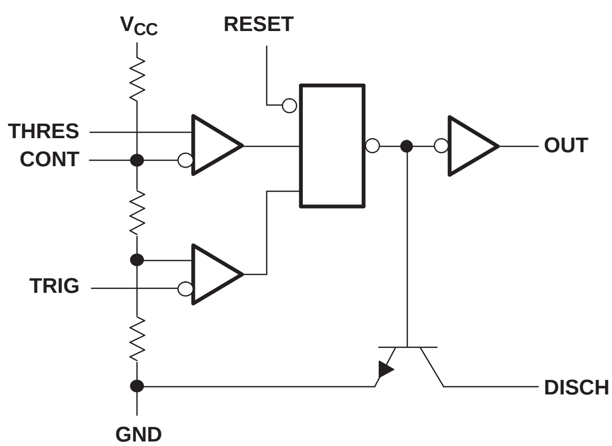
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each timer)

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{DD}	Irrelevant	High	Off
High	>1/3 V_{DD}	>2/3 V_{DD}	Low	On
High	>1/3 V_{DD}	<2/3 V_{DD}	As previously established	

(1) Voltage levels shown are nominal.

FUNCTIONAL BLOCK DIAGRAM, EACH TIMER



RESET can override TRIG, which can override THRES.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]			18	V
V_I	Input voltage	CONT, RESET, THRES, and TRIG		V_{CC}	V
I_O	Output current			±225	mA
θ_{JA}	Package thermal impedance[3][4]	D package		86	°C/W
		N package		80	
		NS package		76	
θ_{JC}	Package thermal impedance[5][6]	J package		15.05	°C/W
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 60 s	J package		300	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s	D, N, or NS package		260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with MIL-STD-883.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	NA556, NE556, SA556	4.5	16	V
		SE556	4.5	18	
V_I	Input voltage	CONT, RESET, THRES, and TRIG		V_{CC}	V
I_O	Output current			±200	mA
T_A	Operating free-air temperature	NA556	–40	105	°C
		NE556	0	70	
		SA556	–40	85	
		SE556	–55	125	

Electrical Characteristics

V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		NA556 NE556 SA556			SE556			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Threshold voltage level	V_{CC} = 15 V		8.8	10	11.2	9.4	10	10.6	V
		V_{CC} = 5 V		2.4	3.3	4.2	2.7	3.3	4	
I_T	Threshold current[1]				30	250		30	250	nA
V_{TRIG}	Trigger voltage level	V_{CC} = 15 V		4.5	5	5.6	4.8	5	5.2	V
			T_A = –55°C to 125°C				3		6	
		V_{CC} = 5 V		1.1	1.67	2.2	1.45	1.67	1.9	
			T_A = –55°C to 125°C						1.9	
I_{TRIG}	Trigger current	TRIG at 0 V			0.5	2		0.5	0.9	µA
V_{RESET}	Reset voltage level			0.3	0.7	1	0.3	0.7	1	V
		T_A = –55°C to 125°C							1.1	
I_{RESET}	Reset current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
		RESET at 0 V			–0.4	1.5		–0.4	–1	
I_{DISCH}	Discharge switch off-state current				20	100		20	100	nA
V_{CONT}	Control voltage (open circuit)	V_{CC} = 15 V		9	10	11	9.6	10	10.4	V
			T_A = –55°C to 125°C				9.6		10.4	
		V_{CC} = 5 V		2.6	3.3	4	2.9	3.3	3.8	
			T_A = –55°C to 125°C				2.9		3.8	
V_{OL}	Low-level output voltage	V_{CC} = 15 V, I_{OL} = 10 mA			0.1	0.25		0.1	0.15	V
			T_A = –55°C to 125°C						0.2	
		V_{CC} = 15 V, I_{OL} = 50 mA			0.4	0.75		0.4	0.5	
			T_A = –55°C to 125°C						1	
		V_{CC} = 15 V, I_{OL} = 100 mA			2	2.5		2	2.2	
			T_A = –55°C to 125°C						2.7	
		V_{CC} = 15 V, I_{OL} = 200 mA			2.5			2.5		
		V_{CC} = 5 V, I_{OL} = 3.5 mA	T_A = –55°C to 125°C						0.35	
		V_{CC} = 5 V, I_{OL} = 5 mA			0.1	0.25		0.1	0.15	
			T_A = –55°C to 125°C						0.8	
		V_{CC} = 5 V, I_{OL} = 8 mA			0.15	0.3		0.15	0.25	
V_{OH}	High-level output voltage	V_{CC} = 15 V, I_{OH} = –100 mA		12.75	13.3		13	13.3		V
			T_A = –55°C to 125°C				12			
		V_{CC} = 15 V, I_{OH} = –200 mA			12.5			12.5		
		V_{CC} = 5 V, I_{OH} = –100 mA		2.75	3.3		3	3.3		
			T_A = –55°C to 125°C				2			
I_{CC}	Supply current	Output low, No load	V_{CC} = 15 V		20	30		20	24	mA
			V_{CC} = 5 V		6	12		6	10	
		Output high, No load	V_{CC} = 15 V		18	26		18	20	
			V_{CC} = 5 V		4	10		4	8	

(1) This parameter influences the maximum value of the timing resistors R and R_B in the circuit of Figure 1. For example, when V_{CC} = 5 V, the maximum value is R = $R_A + R_B \approx 3.4\ M\Omega$, and for V_{CC} = 15 V, the maximum value is ≈ 10 MΩ.

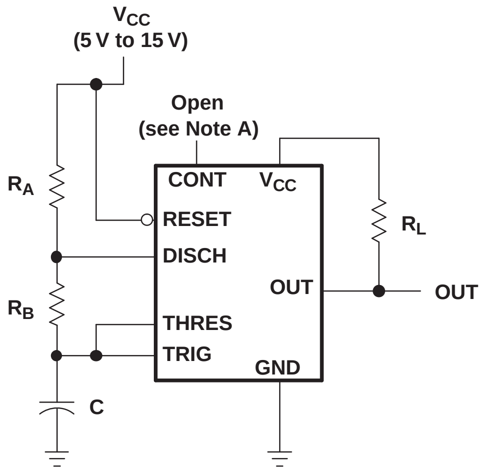
Operating Characteristics

V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS(1)	NA556 NE556 SA556			SE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval(2)	Each timer, monostable(3)	T_A = 25°C		1	3		0.5	1.5(4)	
	Each timer, astable(5)			2.25%			1.5%		
	Timer 1 – Timer 2			±1			±0.5		
Temperature coefficient of timing interval	Each timer, monostable(3)	T_A = MIN to MAX		50			30	100(4)	ppm/°C
	Each timer, astable(5)			150			90		
	Timer 1 – Timer 2			±10			±10		
Supply voltage sensitivity of timing interval	Each timer, monostable(3)	T_A = 25°C		0.1	0.5		0.05	0.2(4)	%/V
	Each timer, astable(5)			0.3			0.15		
	Timer 1 – Timer 2			±0.2			±0.1		
Output-pulse rise time		C_L = 15 pF, T_A = 25°C		100	300		100	200(4)	ns
Output-pulse fall time		C_L = 15 pF, T_A = 25°C		100	300		100	200(4)	ns

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) Timing-interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
(3) Values specified are for a device in a monostable circuit similar to Figure 2, with the following component values: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(5) Values specified are for a device in an astable circuit similar to Figure 1, with the following component values: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

APPLICATION INFORMATION



NOTE A: Bypassing the control-voltage input to ground with a capacitor might improve operation. This should be evaluated for individual applications.

Figure 1. Circuit for Astable Operation

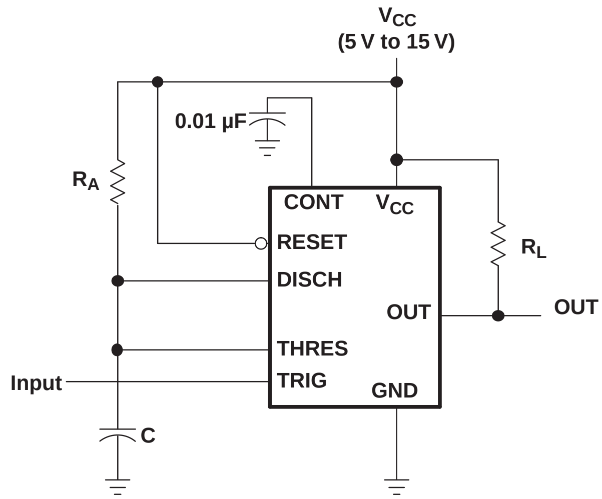


Figure 2. Circuit for Monostable Operation

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
JM38510/10902BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
NA556D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA556DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA556DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA556DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA556N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NA556NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE556D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE556DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE556DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE556DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE556DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE556DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE556N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE556NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE556NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE556NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA556D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SA556DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SA556N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SA556NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SE556FKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SE556J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SE556JB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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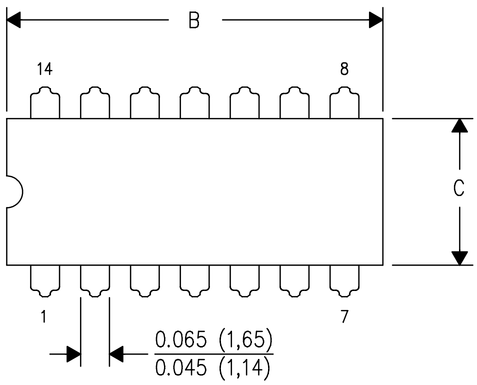
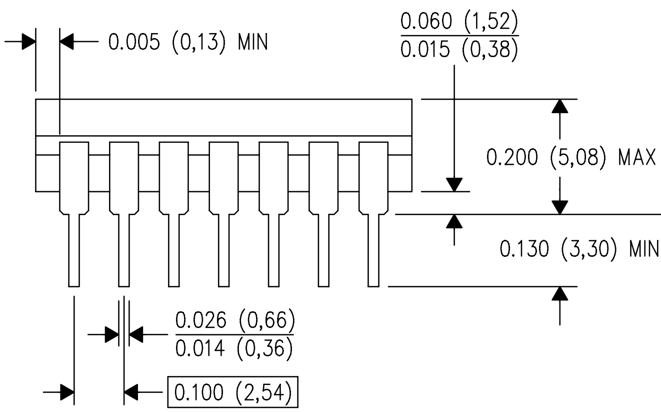
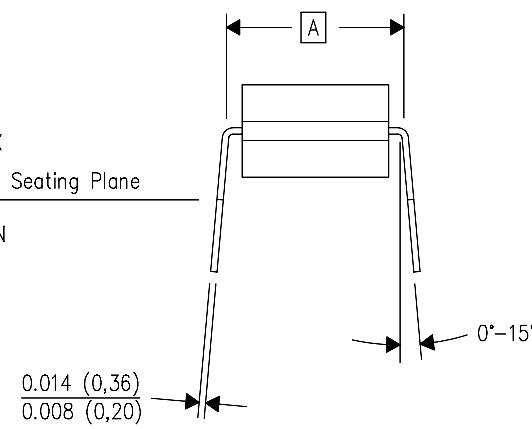
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



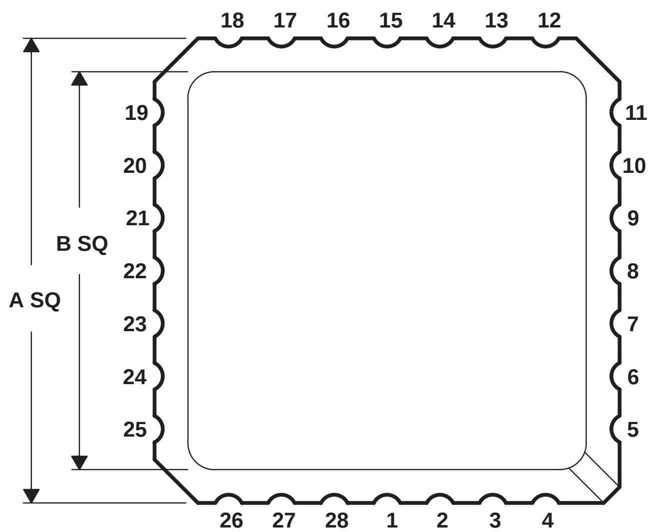


4040083/F 03/03

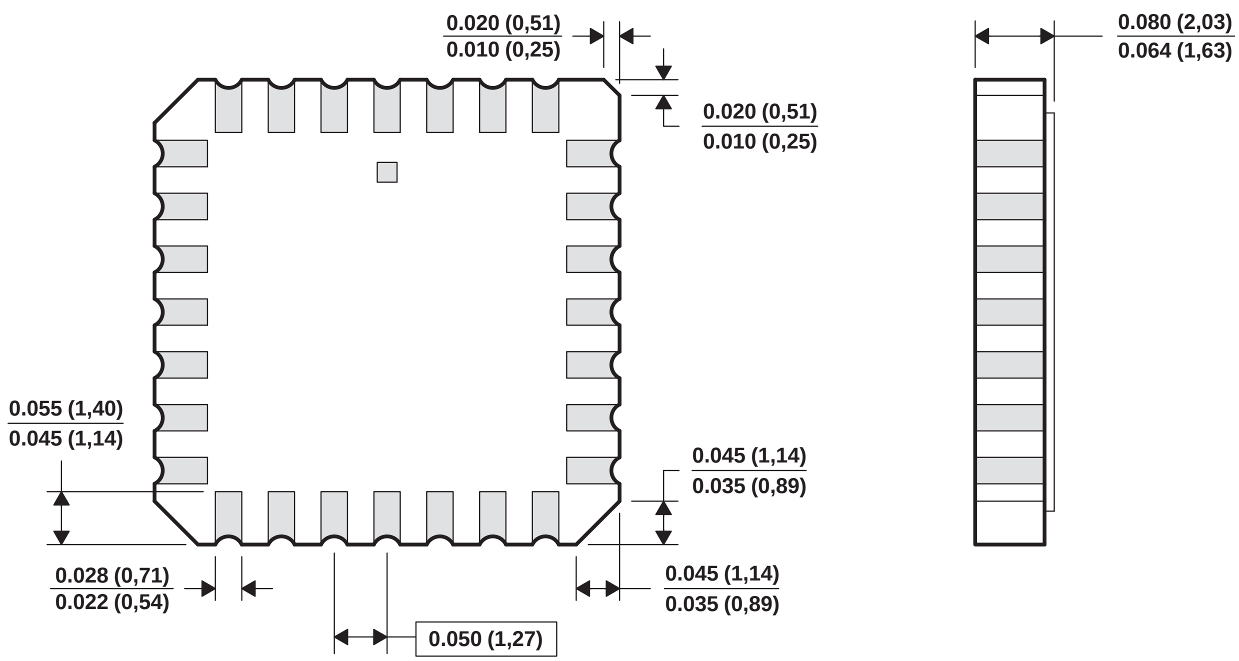
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

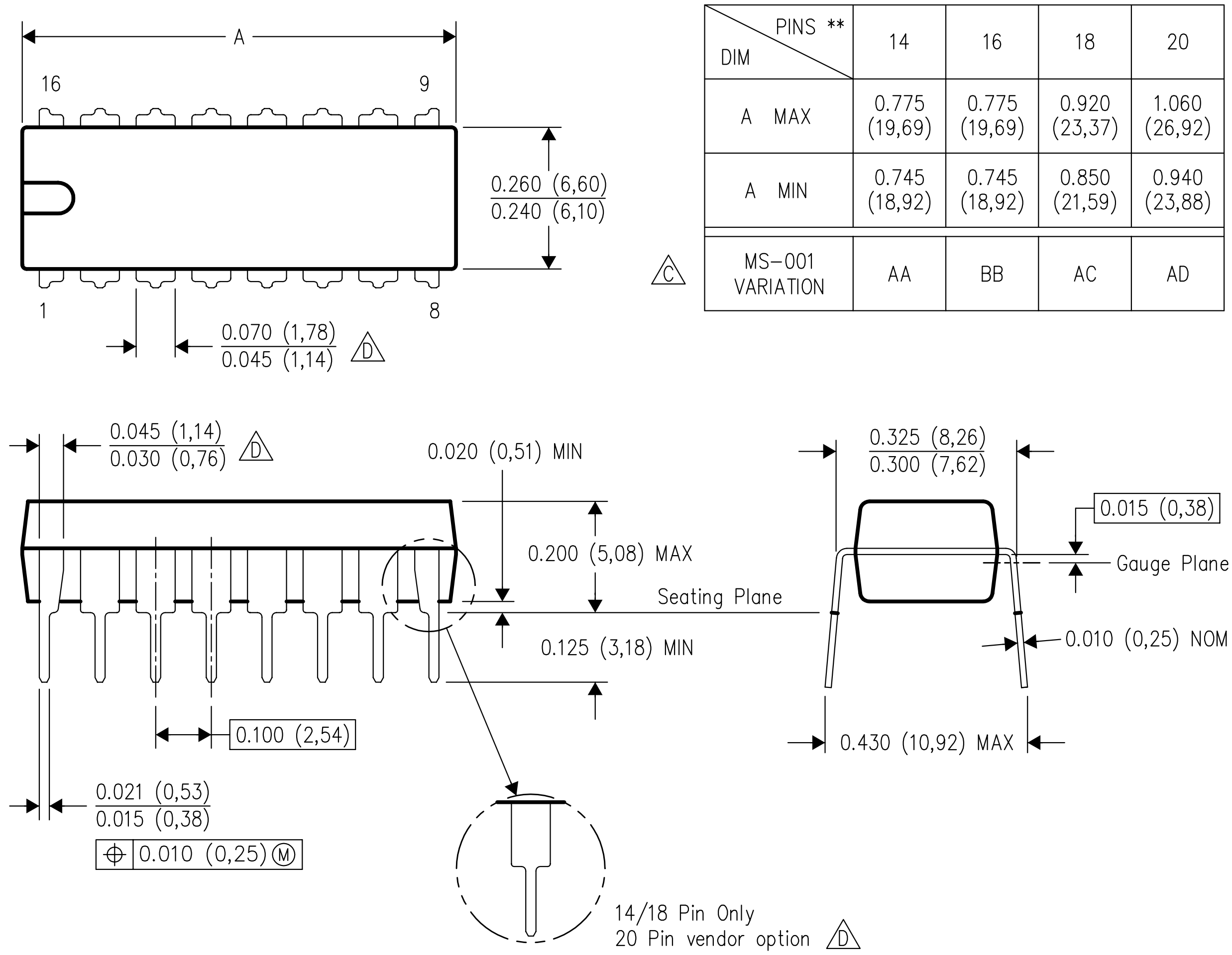


4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

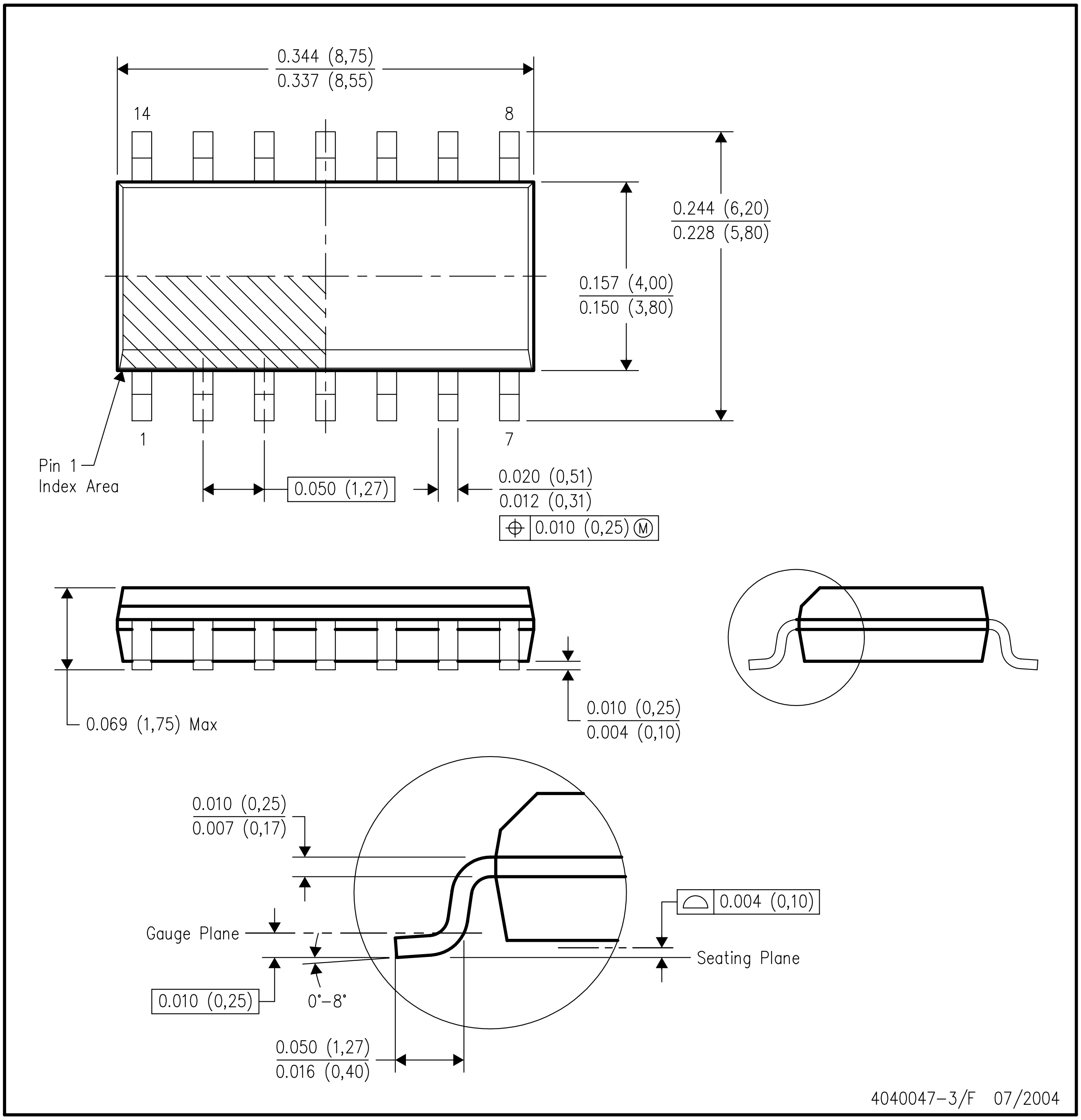


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

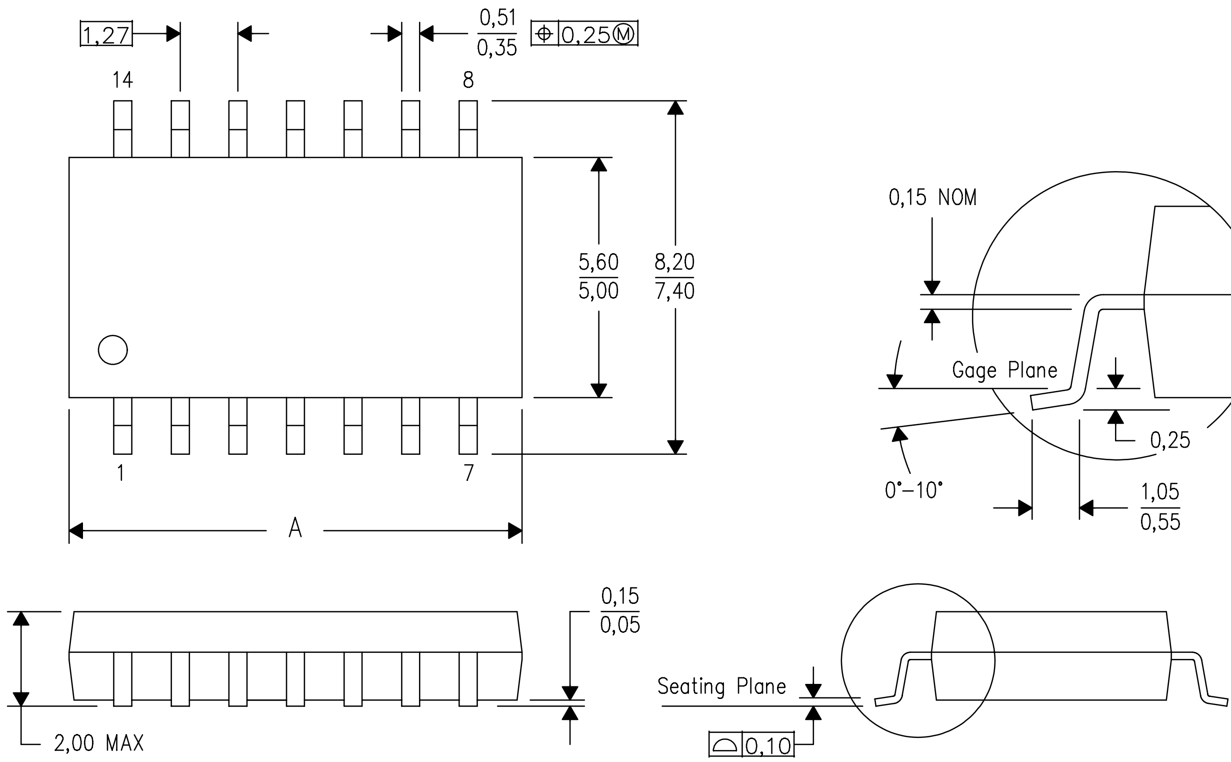
D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



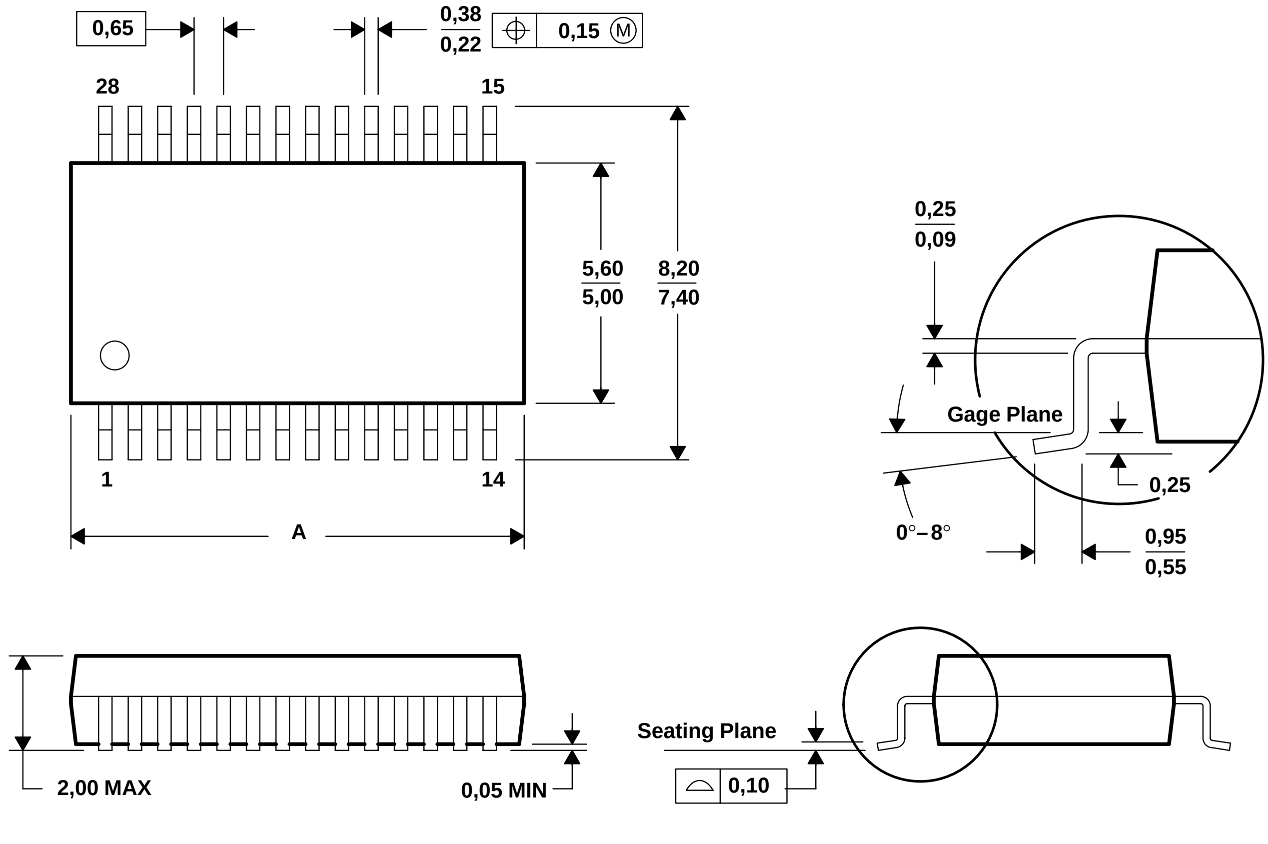
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

IMPORTANT NOTICE

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Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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