CDP1853, CDP1853C

March 1997

N-Bit 1 of 8 Decoder

Features

- **Provides Direct Control of Up to 7 Input and 7 Output Devices**
- **CHIP ENABLE (CE) Allows Easy Expansion for Multi-level I/O Systems**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1853CE	CDP1853E	E16.3
Burn-In		CDP1853CEX	-	E16.3
SBDIP	-40°C to +85°C	CDP1853CD	CDP1853D	D16.3
Burn-In		CDP1853CDX	-	D16.3

Description

The CDP1853 and CDP1853C are 1 of 8 decoders designed for use in general purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-series microprocessors without additional components. The CDP1853 has a recommended operating voltage range of 4V to 10.5V, and the CDP1853C has a recommended operating voltage range of 4V to 6.5V.

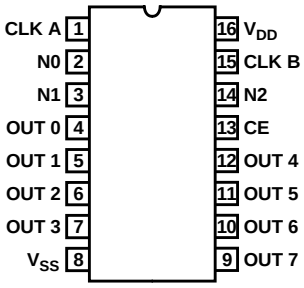
When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE = 0) and during conditions of CLOCK A and CLOCK B as shown in Figure 2. The CDP1853 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to an 1800-series microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Figure 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Figure 6.

The CDP1853 can also be used as a general 1 of 8 decoder for I/O and memory system applications as shown in Figure 4.

The CDP1853 and CDP1853C are supplied in hermetic 16-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

Pinout

16 LEAD DIP
TOP VIEW



CDP1853 Functional Diagram

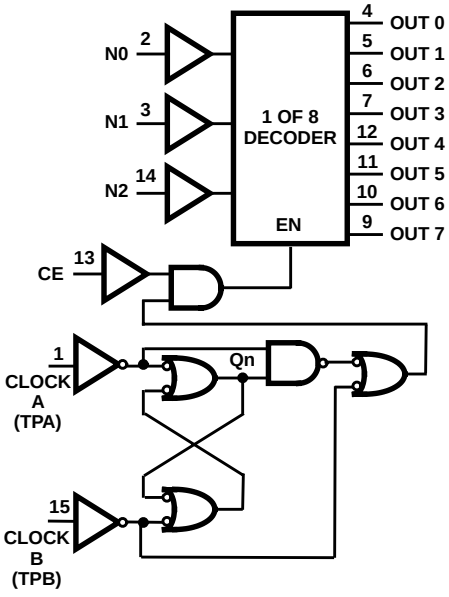


FIGURE 1.

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1†
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1 = High level, 0 = Low level, X = Don't care
† Qn-1 = Enable remains in previous state.

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1853 . . . . . -0.5V to +11V
CDP1853C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
PDIP Package	85	N/A
SBDIP Package	85	22

Operating Temperature Range (T_A)
Ceramic Packages (D Suffix Types) . . . . . -55^{o}C to +125^{o}C
Plastic Packages (E Suffix Types) . . . . . -40^{o}C to +85^{o}C
Storage Temperature Range (T_{STG}) . . . . . -65^{o}C to +150^{o}C
Lead Temperature (During Soldering). . . . . +265^{o}C
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications At T_A = -40 to +85^{o}C, Unless Otherwise Specified

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1853			CDP1853C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE1) TYP	MAX	MIN	(NOTE1) TYP	MAX	
Quiescent Device Current	I_L	-	-	5	-	1	10	-	5	50	µA
		-	-	10	-	10	100	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	2.6	5.2	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.6	-5.2	-	-	-	-	mA
Output Voltage Low Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		1, 9	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±1	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	0, 5	0, 5	5	-	50	100	-	50	100	µA
		0, 10	0, 10	10	-	150	300	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25^{o}C and nominal voltage.
2. I_{OL} = I_{OH} = 1µA
3. Operating current measured in a CDP1802 system at 2MHz with outputs floating.

Spec Number

Recommended Operating Conditions At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1853		CDP1853C		
	MIN	MAX	MIN	MAX	
Supply Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} = ±5%, V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}, t_R, t_F = 20ns, C_L = 100pF, Unless Otherwise Specified

PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1853			CDP1853C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time:									
CE to Output	t_{EOH}, t_{EOL}	5	-	175	275	-	175	275	ns
		10	-	90	150	-	-	-	ns
N to Output	t_{NOH}, t_{NOL}	5	-	225	350	-	225	350	ns
		10	-	120	200	-	-	-	ns
Clock A to Output	t_{AO}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
Clock B to Output	t_{BO}	5	-	175	275	-	175	275	ns
		10	-	90	150	-	-	-	ns
Minimum Pulse Widths:									ns
Clock A	t_{CACA}	5	-	50	75	-	50	75	ns
		10	-	25	50	-	-	-	ns
Clock B	t_{CBCB}	5	-	50	75	-	50	75	ns
		10	-	25	50	-	-	-	ns

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for T_A = +25°C and nominal voltages.

Timing Diagrams

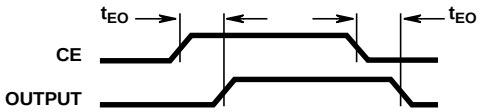


FIGURE 2A. CE TO OUTPUT (0-7) DELAY TIME

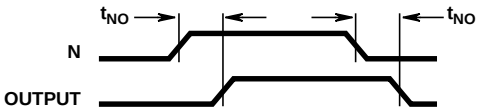


FIGURE 2B. N LINES TO OUTPUT (0-7) DELAY TIME

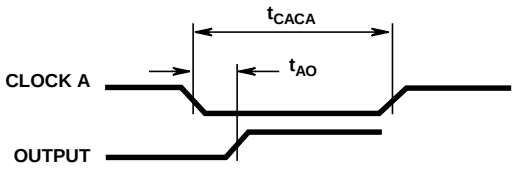


FIGURE 2C. CLOCK A TO OUTPUT (0-7) DELAY TIME

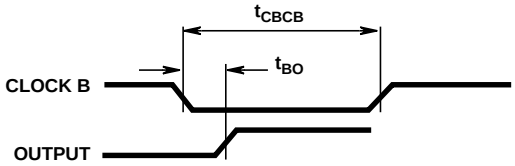
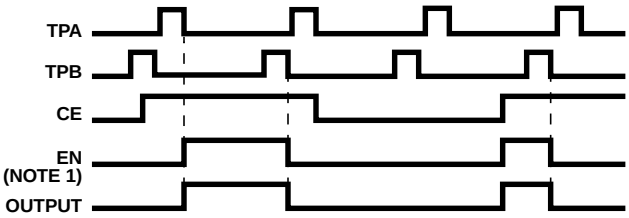


FIGURE 2D. CLOCK B TO OUTPUT (0-7) DELAY TIME

FIGURE 2. PROPAGATION DELAY TIME DIAGRAMS



NOTE 1. OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR
REFERENCE ONLY (SEE FIGURE 1)

FIGURE 3. TIMING DIAGRAM

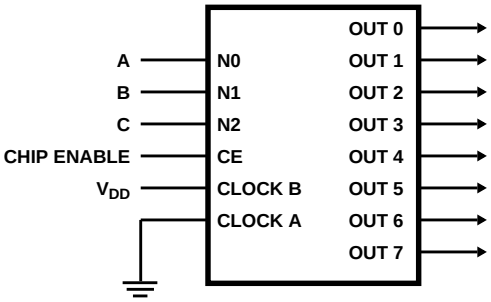


FIGURE 4. N-BIT DECODER USED AS A 1 OF 8 DECODER

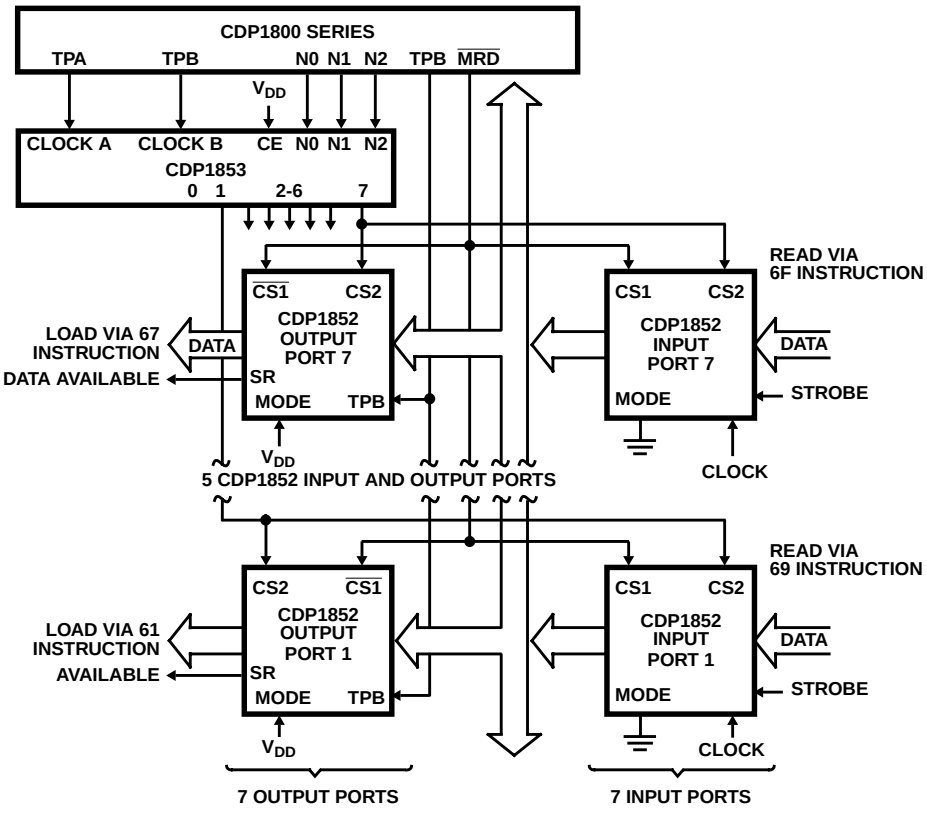


FIGURE 5. N-BIT DECODER IN A ONE-LEVEL I/O SYSTEM

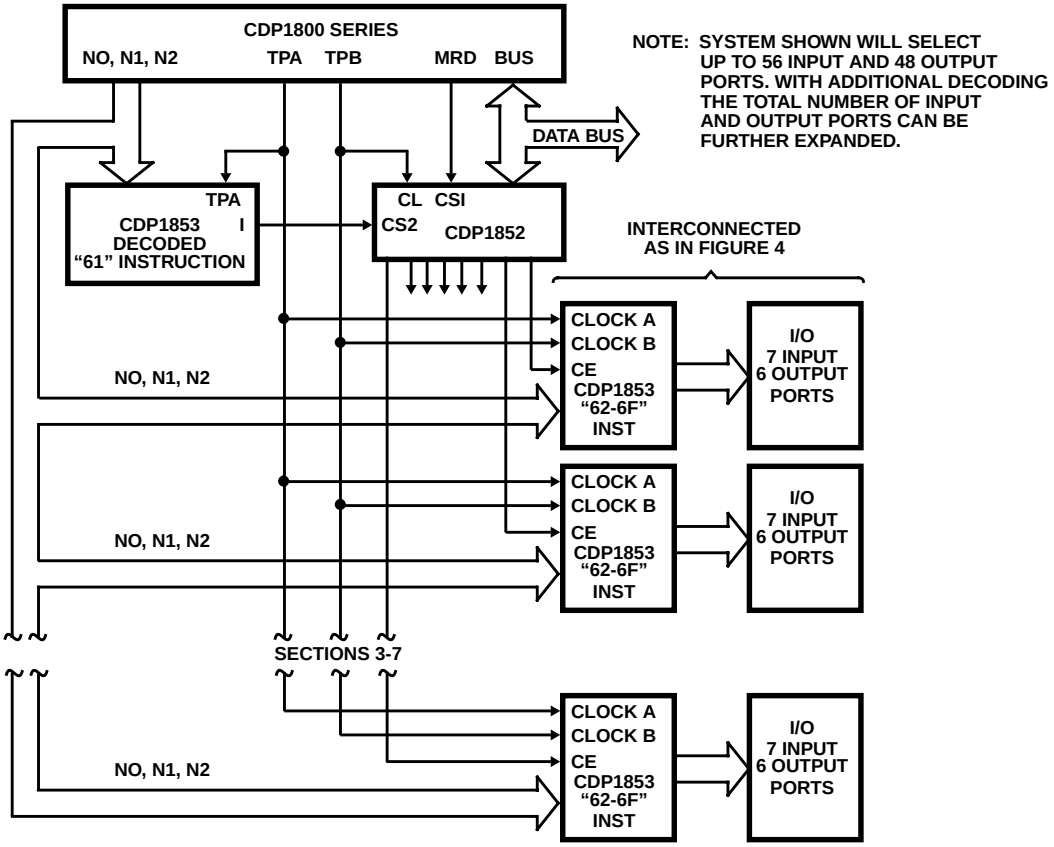


FIGURE 6. TWO-LEVEL I/O USING CDP1853 AND CDP1852

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