

# DATA SHEET

## **TEA1507** **GreenChip™II SMPS control IC**

Preliminary specification  
File under Integrated Circuits, IC11

2000 Dec 05

# GreenChip™II SMPS control IC

# TEA1507

## FEATURES

### Distinctive features

- Universal mains supply operation (70 to 276 V AC)
- High level of integration, giving a very low external component count.

### Green features

- Valley/zero voltage switching for minimum switching losses
- Efficient quasi-resonant operation at high power levels
- Frequency reduction at low power standby for improved system efficiency (<3 W)
- Burst mode operation for very low standby levels (<1 W)
- On-chip start-up current source.

### Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection (zero switch-on current)
- Accurate and adjustable overvoltage protection
- Short winding protection
- Undervoltage protection (foldback during overload)
- Overtemperature protection
- Low and adjustable overcurrent protection trip level
- Soft (re)start
- Mains voltage-dependent operation-enabling level.

## APPLICATIONS

Besides typical application areas, i.e. TV and Monitor supplies, the device can be used in all applications that demand an efficient and cost-effective solution up to 250 W.

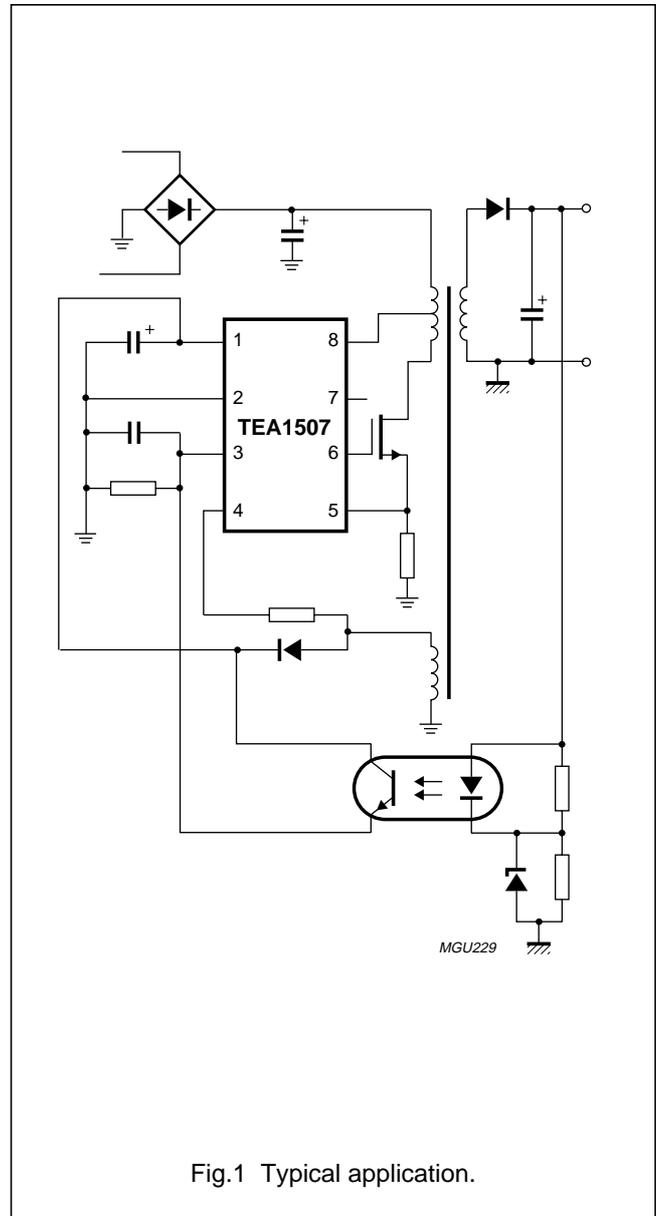


Fig.1 Typical application.

# GreenChip™II SMPS control IC

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## GENERAL DESCRIPTION

The GreenChip™II is the second generation of green Switched Mode Power Supply (SMPS) controller ICs operating directly from the rectified universal mains. A high level of integration leads to a cost effective power supply with a very low number of external components.

The special built-in green functions allow the efficiency to be optimum at all power levels. This holds for quasi-resonant operation at high power levels, as well as fixed frequency operation with valley switching at medium power levels. At low power (standby) levels, the system operates at reduced frequency and with valley detection.

If burst mode operation is applied, the standby power level can even be reduced to below 1 W.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified mains voltage in an effective and green way. A second low voltage BICMOS IC is used for accurate, high speed protection functions and control.

Highly efficient, reliable supplies can easily be designed using the GreenChip™II controller.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1507P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

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BLOCK DIAGRAM

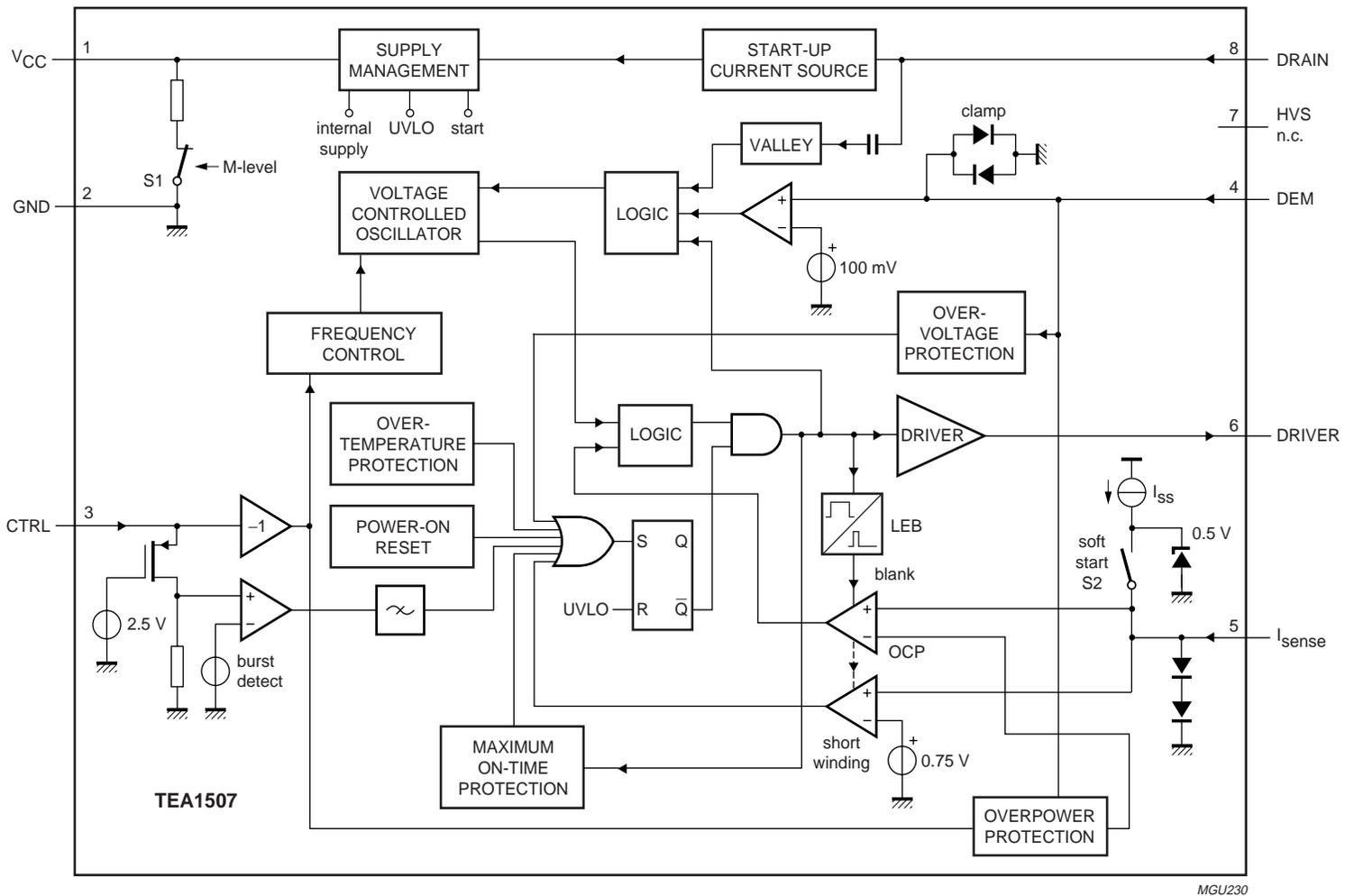


Fig.2 Block diagram.

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### PINNING

SYMBOL	PIN	DESCRIPTION
V <sub>CC</sub>	1	supply voltage
GND	2	ground
CTRL	3	control input
DEM	4	input from auxiliary winding for demagnetization timing, OVP and OPP
I <sub>sense</sub>	5	programmable current sense input
DRIVER	6	gate driver output
HVS	7	high voltage safety spacer, not connected
DRAIN	8	drain of external MOS switch, input for start-up current and valley sensing

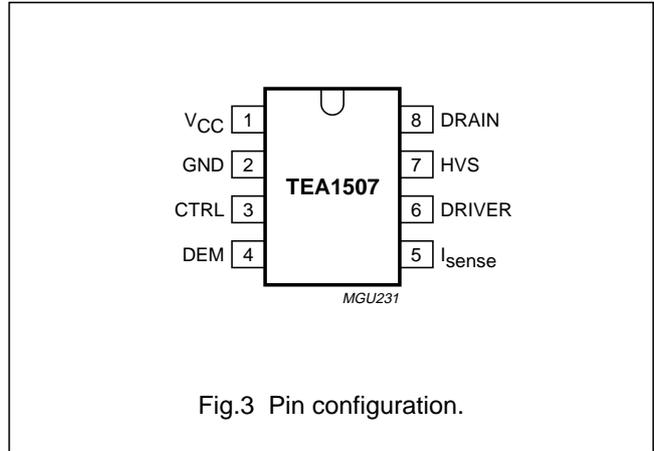


Fig.3 Pin configuration.

### FUNCTIONAL DESCRIPTION

The TEA1507 is the controller of a compact flyback converter, with the IC situated at the primary side. An auxiliary winding of the transformer provides demagnetization detection and powers the IC after start-up.

The TEA1507 operates in multi modes.

The next converter stroke is started only after demagnetization of the transformer current (zero current switching), while the drain voltage has reached the lowest voltage to prevent switching losses (green function). The primary resonant circuit of primary inductance and drain capacitor ensures this quasi-resonant operation. The design can be optimized in such a way that zero voltage switching can be reached over almost the universal mains range.

To prevent very high frequency operation at lower loads, the quasi-resonant operation changes smoothly in fixed frequency PWM control.

At very low power (standby) levels, the frequency is controlled down, via the VCO, to a minimum frequency of about 6 kHz. Typically, 3 Watts can be achieved for a 75 W converter with an output power of 100 mW.

#### Start-up, mains enabling operation level and undervoltage lock out (see Figs. 10 and 11)

Initially, the IC is self supplying from the rectified mains voltage via pin DRAIN. Supply capacitor C<sub>VCC</sub> is charged by the internal start-up current source to a level of about 4 V or higher, depending on the drain voltage. Once the drain voltage exceeds the M-level (mains-dependent operation-enabling level), the start-up current source will

continue charging capacitor C<sub>VCC</sub> (switch S1 will be opened), see Fig.2. The IC will activate the power converter as soon as the voltage on pin V<sub>CC</sub> passes the V<sub>CC(start)</sub> level. The IC supply is taken over by the auxiliary winding as soon as the output voltage reaches its intended level and the IC supply from the mains voltage is subsequently stopped for high efficiency operation (green function).

The moment the voltage on pin V<sub>CC</sub> drops below the V<sub>UVLO</sub> (undervoltage lock out) level, the IC stops switching and enters a safe restart from the rectified mains voltage. Inhibiting the auxiliary supply by external means causes the converter to operate in a stable, well-defined burst mode.

#### Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

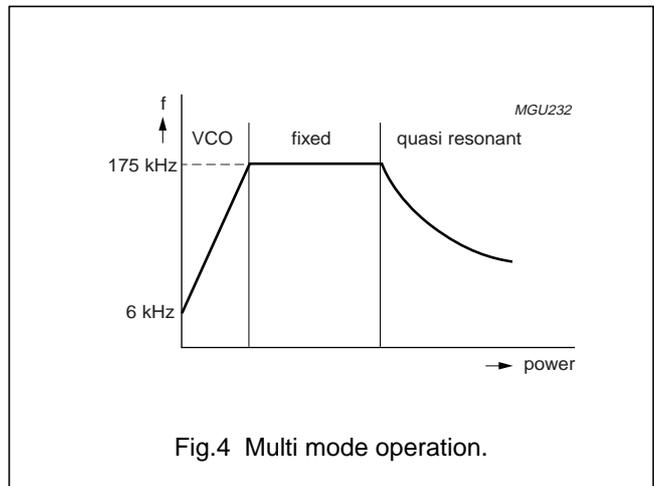


Fig.4 Multi mode operation.

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### Current mode control

Current mode control is used for its good line regulation behaviour.

The 'on-time' is controlled by the internally inverted control pin voltage, which is compared with the primary current information. The primary current is sensed across an external resistor. The driver output is latched in the logic, preventing multiple switch-on.

The internal control voltage is inversely proportional to the external control pin voltage, with an offset of 1.5 V. This means that a voltage range from 1 to 1.5 V on pin CTRL will result in an internal control voltage range from 0.5 to 0 V (the maximum external control voltage results in a minimum duty cycle).

### Oscillator

The maximum fixed frequency of the oscillator is set by an internal current source and capacitor. The maximum frequency is reduced once the control voltage enters the VCO control window. Then, the maximum frequency changes linearly with the control voltage until the minimum frequency is reached (see Figs 5 and 6).

### Valley switching (see Fig.7)

A new cycle starts when the power switch is switched on. After the 'on-time' (which is determined by the 'sense' voltage and the internal control voltage), the switch is opened and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation

with a frequency of approximately 
$$\frac{1}{(2 \times \pi \times \sqrt{(L_p \times C_d)})}$$

where  $L_p$  is the primary self inductance of the transformer and  $C_d$  is the capacitance on the drain node.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. This method is called valley detection. Figure 7 shows the drain voltage together with the valley signal, the signal indicating the secondary stroke and the oscillator signal.

In an optimum design, the reflected secondary voltage on the primary side will force the drain voltage to zero. Thus, zero voltage switching is very possible, preventing large

capacitive switching losses  $(P = \frac{1}{2} \times C \times V^2 \times f)$ , and

allowing high frequency operation, which results in small and cost effective inductors.

### Demagnetization

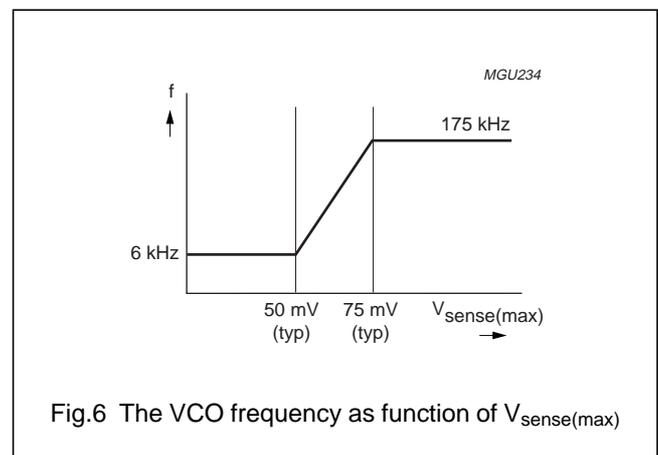
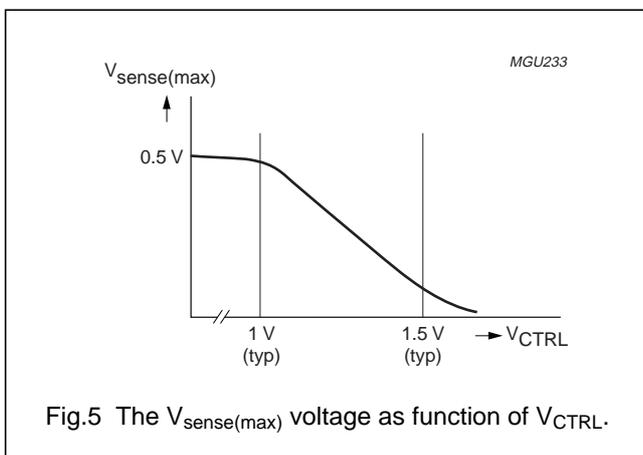
The system will be in discontinuous conduction mode all the time. The oscillator will not start a new primary stroke until the secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first  $t_{suppr}$  time. This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages/start-up.

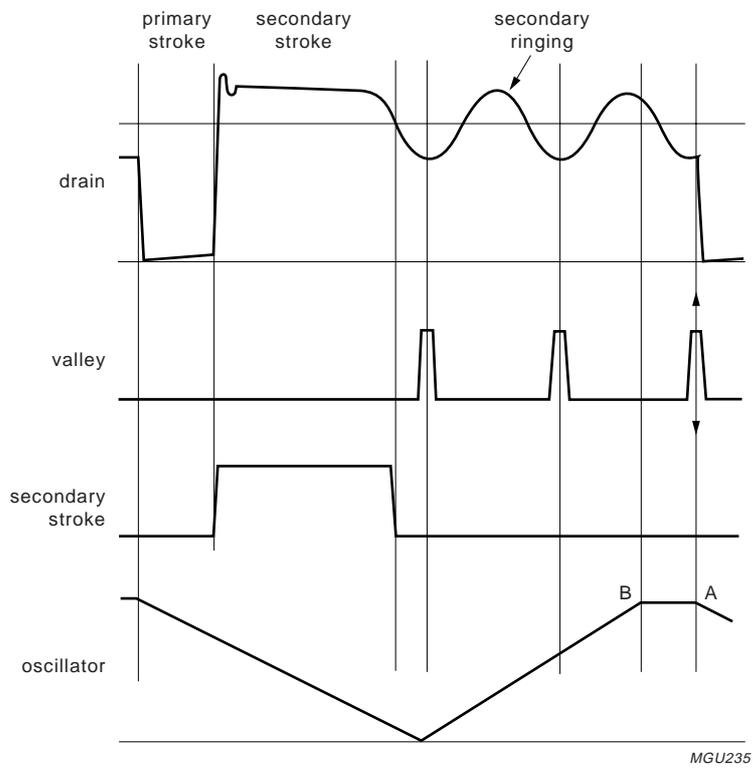
### Minimum and maximum 'on-time'

The minimum 'on-time' of the SMPS is determined by the Leading Edge Blanking (LEB) time. The IC limits the 'on-time' to 50  $\mu$ s. When the system desires an 'on-time' longer than 50  $\mu$ s, a fault condition is assumed (e.g. removed  $C_i$ ), the IC will stop switching and enter the safe restart mode.



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MGU235

- A: Start of new cycle at lowest drain voltage.
- B: Start of new cycle in a classical PWM system at high drain voltage.

Fig.7 Signals for valley switching.

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### OverVoltage Protection (OVP)

An OVP mode is implemented in the GreenChip™ series. For the TEA1507, this works by sensing the auxiliary voltage via the current flowing into pin DEM during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. Any voltage spikes are averaged by an internal filter.

If the output voltage exceeds the OVP trip level, the OVP circuit switches the power MOSFET off. Next, the controller waits until the UVLO level is reached on pin V<sub>CC</sub>. This is followed by a safe restart cycle, after which switching starts again. This process is repeated as long as the OVP condition exists.

The output voltage at which the OVP function trips, V<sub>o(OVP)</sub> can be set by the demagnetization resistor, R<sub>DEM</sub>:

$$V_{o(OVP)} = \frac{N_s}{N_{aux}} \times (I_{(OVP)(DEM)} \times R_{DEM} + V_{clamp(DEM)(pos)})$$

Where N<sub>s</sub> is the number of secondary turns and N<sub>aux</sub> is the number of auxiliary turns of the transformer.

Current I<sub>ref</sub> is internally trimmed.

The value of the demagnetization resistor (R<sub>DEM</sub>) can be adjusted to the turns ratio of the transformer, thus making an accurate OVP possible.

### OverCurrent Protection (OCP)

The cycle-by-cycle peak drain current limit circuit uses the external source resistor to measure the current accurately. This allows optimum size determination of the transformer core (cost issue). The circuit is activated after the leading edge blanking time, t<sub>leb</sub>. The OCP protection circuit limits the 'sense' voltage to an internal level.

### OverPower Protection (OPP)

During the primary stroke, the rectified mains input voltage is measured by sensing the current drawn from pin DEM. This current is dependent on the mains voltage, according

to the following formula:  $I_{(DEM)} \approx \frac{V_{aux}}{R_{DEM}} \approx \frac{N \times V_{mains}}{R_{DEM}}$

Where:  $N = \frac{N_{aux}}{N_p}$

The current information is used to adjust the peak drain current, which is measured via pin I<sub>sense</sub>. The internal compensation is such that an almost mains independent maximum output power can be realized.

The OPP curve is given in Fig.8.

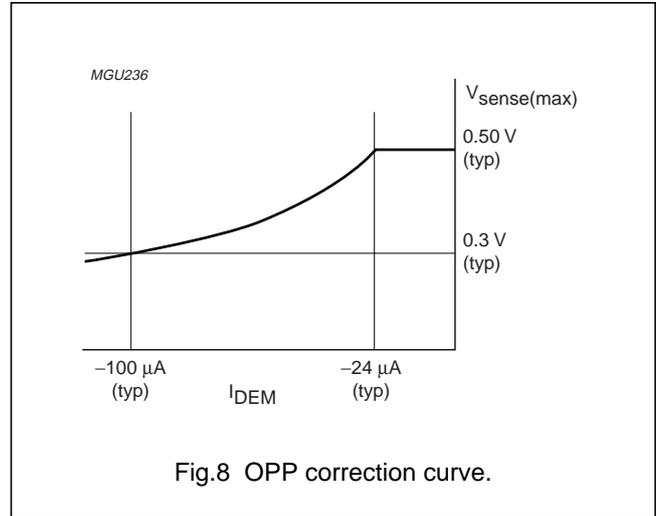


Fig.8 OPP correction curve.

### Short winding protection

After the leading edge blanking time, the short winding protection circuit is also activated. If the 'sense' voltage exceeds the short winding protection voltage V<sub>swp</sub>, the converter will stop switching. Once V<sub>CC</sub> drops below the UVLO level, capacitor C<sub>VCC</sub> will be recharged and the supply will restart again. This cycle will be repeated until the short circuit is removed (safe restart mode).

The short winding protection will also protect in case of a secondary diode short circuit.

### Overtemperature protection

An accurate temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the IC will stop switching. When V<sub>CC</sub> drops to UVLO, capacitor C<sub>VCC</sub> will be recharged to the V<sub>start</sub> level. If the temperature is still too high, V<sub>CC</sub> will drop again to the UVLO level, etc. (safe restart mode).

Operation recommences when the junction temperature drops 8 degrees typically.

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**Burst mode standby**

Pin CTRL (pin 3) is also used to implement the burst mode standby. In burst mode standby, the power supply enters a special low dissipation state, where it typically consumes less than 1 W of input power ( $P_o < 100 \text{ mW}$ ), but is still able to supply a microprocessor, for example. Figure 12 shows a flyback converter using the burst mode standby function. The system enters burst mode standby when the microprocessor closes switches S2 and S3 on the secondary side. Switch S2 connects the high voltage output secondary winding to the low voltage microprocessor capacitor ( $C_{\mu C}$ ), bypassing  $C_o$ .

When the voltage on  $C_{\mu C}$  exceeds the Zener voltage, the opto-coupler is activated, sending a large current signal to CTRL. In response to this signal, the IC stops switching and enters a ‘hiccup’ mode. This burst activation signal should be present for longer than the ‘burst blank’ period (typically  $30 \mu\text{s}$ ): the blanking time prevents false burst triggering due to spikes. Figure 11 shows the burst-mode standby signals. The hiccup mode during burst mode standby operation does not differ from the hiccup mode in safe-restart mode during a system fault condition (e.g. OVP or output short circuit). The power is reduced during soft-restart mode.

Burst mode standby operation continues until the microcontroller opens switches S2 and S3. The system then enters the start-up sequence and begins normal switching behaviour.

$$I_{\text{burstmode}} = \frac{V_{\text{th}}}{R_{\text{CTRL}}} + I_{\text{th(on)}}$$

(For burst mode specification, see Figs 11 and 12.)

**Soft start-up (pin  $I_{\text{sense}}$ )**

To prevent transformer rattle during hiccup, the transformer peak current is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin  $I_{\text{sense}}$  (pin 5) and the sense resistor. An internal current source charges the capacitor to  $V = I_{\text{SS}} \times R_{\text{SS}}$ , with a maximum of about 0.5 V.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of  $R_{\text{SS}}$  and  $C_{\text{SS}}$ .

$$I_{\text{primary(max)}} = \frac{V_{\text{ocp}} - (I_{\text{SS}} \times R_{\text{SS}})}{R_{\text{sense}}}$$

$$\tau = R_{\text{SS}} \times C_{\text{SS}}$$

The charging current  $I_{\text{SS}}$  will flow as long as the voltage on pin  $I_{\text{sense}}$  is below approximately 0.5 V. If the voltage on pin  $I_{\text{sense}}$  exceeds the 0.5 V, the soft start current source will start limiting the current  $I_{\text{SS}}$ . At the  $V_{\text{CC(start)}}$  level, the  $I_{\text{SS}}$  current source is completely switched off (see Fig.9).

Since the soft start current  $I_{\text{SS}}$  is subtracted from pin  $V_{\text{CC}}$  charging current, the  $R_{\text{SS}}$  value will affect the  $V_{\text{CC}}$  charging current level by a maximum of  $60 \mu\text{A}$  (typical value).

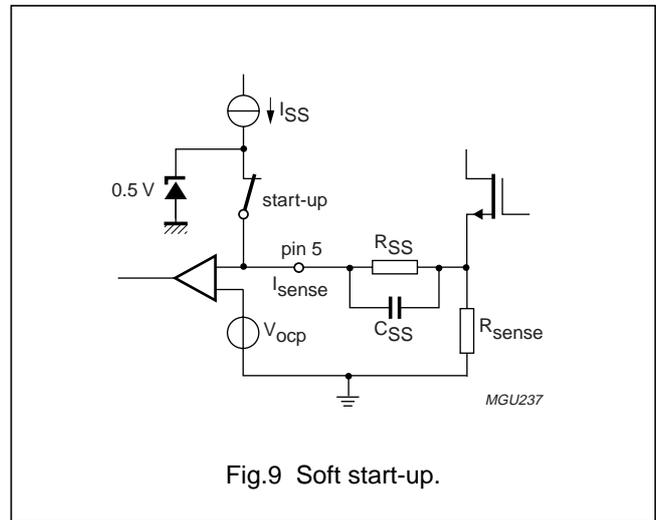


Fig.9 Soft start-up.

**Driver**

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 125 mA and a current sink capability of typical 540 mA. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

A low driver source current has been chosen to limit the  $\Delta V/\Delta t$  at switch-on. This reduces Electro Magnetic Interference (EMI) and also limits the current spikes across  $R_{\text{sense}}$ .

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip; pin 1 may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Voltages</b>					
V <sub>1</sub>	pin 1 (V <sub>CC</sub> )	continuous	-0.4	+20	V
V <sub>3</sub>	pin 3 (CTRL)		-0.4	+5	V
V <sub>4</sub>	pin 4 (DEM)	current limited	-0.4	-	V
V <sub>5</sub>	pin 5 (I <sub>sense</sub> )	current limited	-0.4	-	V
V <sub>8</sub>	pin 8 (DRAIN)		-0.4	+650	V
<b>Currents</b>					
I <sub>3</sub>	pin 3 (CTRL)	d < 10%	-	+50	mA
I <sub>4</sub>	pin 4 (DEM)		-250	+250	μA
I <sub>5</sub>	pin 5 (I <sub>sense</sub> )		-1	+10	mA
I <sub>6</sub>	pin 6 (DRIVER)	d < 10%	-0.8	+2	A
I <sub>8</sub>	pin 8 (DRAIN)		-	+5	mA
<b>General</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> < 55 °C	-	1.0	W
T <sub>stg</sub>	storage temperature		-55	+150	°C
T <sub>vj</sub>	virtual junction temperature		-20	+145	°C
<b>ESD</b>					
V <sub>ESD</sub>	electrostatic discharge voltage human body model	class 1			
		pins 1 to 6; note 1	-	1750	V
	pin 8 (DRAIN); note 1	-	1000	V	
	machine model	note 2	-	200	V

**Notes**

- Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
- Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air; note 1	100	K/W

**Note**

- With pin GND connected to sufficient copper area on the printed-circuit board.

**QUALITY SPECIFICATION**

In accordance with 'SNW-FQ-611-E'.

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**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$ ;  $V_{CC} = 15\text{ V}$ ; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Start-up current source (pin 8)</b>						
$I_{i(DRAIN)}$	supply current drawn from drain pin	$V_{CC} = 0\text{ V}$ ; $V_{DRAIN} > 100\text{ V}$	1.0	1.2	1.4	mA
		with auxiliary supply; $V_{DRAIN} > 100\text{ V}$	–	100	300	$\mu\text{A}$
$BV_{DSS}$	breakdown voltage		650	–	–	V
M-level	mains-dependent operation-enabling level		60	–	100	V
<b><math>V_{CC}</math> management (pin 1)</b>						
$V_{CC(start)}$	start-up voltage on $V_{CC}$		10.3	11	11.7	V
$V_{CC(UVLO)}$	under voltage lock-out on $V_{CC}$		8.1	8.7	9.3	V
$V_{CC(hys)}$	hysteresis voltage on $V_{CC}$	$V_{CC(start)} - V_{CC(UVLO)}$	2.0	2.3	2.6	V
$I_{i(VCC)H}$	pin $V_{CC}$ charging current	$V_{DRAIN} > 100\text{ V}$ ; $V_{CC} < 3\text{ V}$	–1.2	–1	–0.8	mA
$I_{i(VCC)L}$	pin $V_{CC}$ charging current	$V_{DRAIN} > 100\text{ V}$ ; $3\text{ V} < V_{CC} < V_{CC(UVLO)}$	–1.2	–0.75	–0.45	mA
$I_{VCC(restart)}$	pin $V_{CC}$ restart current	$V_{DRAIN} > 100\text{ V}$ ; $V_{CC(UVLO)} < V_{CC} < V_{CC(start)}$	–650	–550	–450	$\mu\text{A}$
$I_{CC(operate)}$	supply current under normal operation	no load on pin DRIVER	1.1	1.3	1.5	mA
<b>Demagnetization management (pin 4)</b>						
$V_{DEM}$	demagnetization comparator threshold voltage on pin DEM		50	100	150	mV
$I_{DEM}$	pin DEM current	$V_{DEM} = 50\text{ mV}$	–50 <sup>(1)</sup>	–	0	nA
$V_{clamp(DEM)(neg)}$	negative clamp voltage on pin DEM	at $I_{DEM} = -150\text{ }\mu\text{A}$	–0.5	–0.25	–0.05	V
$V_{clamp(DEM)(pos)}$	positive clamp voltage on pin DEM	at $I_{DEM} = 250\text{ }\mu\text{A}$	0.5	0.7	0.9	V
$t_{suppr}$	suppression of transformer ringing at start of secondary stroke		1.1	1.5	1.9	$\mu\text{s}$
<b>Pulse width modulator</b>						
$t_{on(min)}$	minimum on-time		–	$t_{ieb}$	–	ns
$t_{on(max)}$	maximum on-time	latched	40	50	60	$\mu\text{s}$
<b>Oscillator</b>						
$f_{oscL}$	oscillator low frequency (fixed frequency)	$V_{CTRL} > 1.5\text{ V}$	5	6.5	8	kHz
$f_{oscH}$	oscillator high frequency (fixed frequency)	$V_{CTRL} < 1\text{ V}$	145	175	205	kHz
$V_{vco(start)}$	peak voltage at pin $I_{sense}$ , where frequency reduction starts	see Fig.6	–	75	–	mV
$V_{vco(max)}$	peak voltage at pin $I_{sense}$ , where the frequency is equal to $f_{oscL}$		–	50	–	mV
<b>Duty cycle control (pin 3)</b>						
$V_{CTRL(min)}$	min. voltage on CTRL (max. duty cycle)		–	1.0	–	V
$V_{CTRL(max)}$	max. voltage on CTRL (min. duty cycle)		–	1.5	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Burst mode standby (pin 3)</b>						
$V_{th(burst)(on)}$	burst mode standby active threshold voltage	at $I_{burst} = 6 \text{ mA}$	3.3	3.8	4.3	V
$I_{th(burst)(on)}$	burst mode standby active current		16	–	–	mA
$I_{th(burst)(off)}$	burst mode standby inactive current		–	–	6	mA
$t_{(burst-blank)}$	burst mode standby blanking time		25	30	35	$\mu\text{s}$
<b>Valley switch (pin 8)</b>						
$\Delta V/\Delta t_{valley}$	$\Delta V/\Delta t$ for valley recognition		–85	–	+85	V/ $\mu\text{s}$
$t_{valley-swon}$	delay from valley recognition to switch-on		–	150 <sup>(1)</sup>	–	ns
<b>Current and short winding protection (pin 5)</b>						
$V_{sense(max)}$	maximum source voltage OCP	$\Delta V/\Delta t = 0.1 \text{ V}/\mu\text{s}$	0.48	0.52	0.56	V
$t_{propagation}$	delay from detecting $V_{sense(max)}$ to switch-off	$\Delta V/\Delta t = 0.5 \text{ V}/\mu\text{s}$	–	140	185	ns
$V_{swp}$	short winding protection voltage		0.83	0.88	0.96	V
$t_{leb}$	blanking time for current and short winding protection		300	370	440	ns
$I_{ss}$	soft start current	$V_{sense} < 0.5 \text{ V}$	45	60	75	$\mu\text{A}$
<b>Overvoltage protection (pin 4)</b>						
$I_{(OVP)(DEM)}$	OVP protection level at pin 4, set by the demagnetization resistor $R_{DEM}$ ; see Section “OverVoltage Protection (OVP)”		54	60	66	$\mu\text{A}$
<b>Overpower protection (pin 4)</b>						
$I_{(OPP)(DEM)}$	OPP current at pin 4, start of OPP correction. Set by the demagnetization resistor $R_{DEM}$ ; see Section “OverPower Protection (OPP)”		–	–24	–	$\mu\text{A}$
$I_{(OPP50\%)(DEM)}$	OPP current at pin 4 where maximum source voltage is limited to 0.3 V		–	–100	–	$\mu\text{A}$
<b>Driver (pin 6)</b>						
$I_{source}$	source current capability of driver	$V_{CC} = 9.5 \text{ V}; V_{DRIVER} = 2 \text{ V}$	–	–170	–88	mA
$I_{sink}$	sink current capability of driver	$V_{CC} = 9.5 \text{ V}; V_{DRIVER} = 2 \text{ V}$	–	300	–	mA
		$V_{CC} = 9.5 \text{ V}; V_{DRIVER} = 9.5 \text{ V}$	400	700	–	mA
$V_{o(driver)(max)}$	maximum output voltage of the driver	$V_{CC} > 12 \text{ V}$	–	11.5	12	V
<b>Temperature protection</b>						
$T_{prot(max)}$	maximum temperature threshold		130	140	150	$^{\circ}\text{C}$
$T_{prot(hyst)}$	hysteresis temperature		–	8 <sup>(1)</sup>	–	$^{\circ}\text{C}$

**Note**

1. Guaranteed by design.



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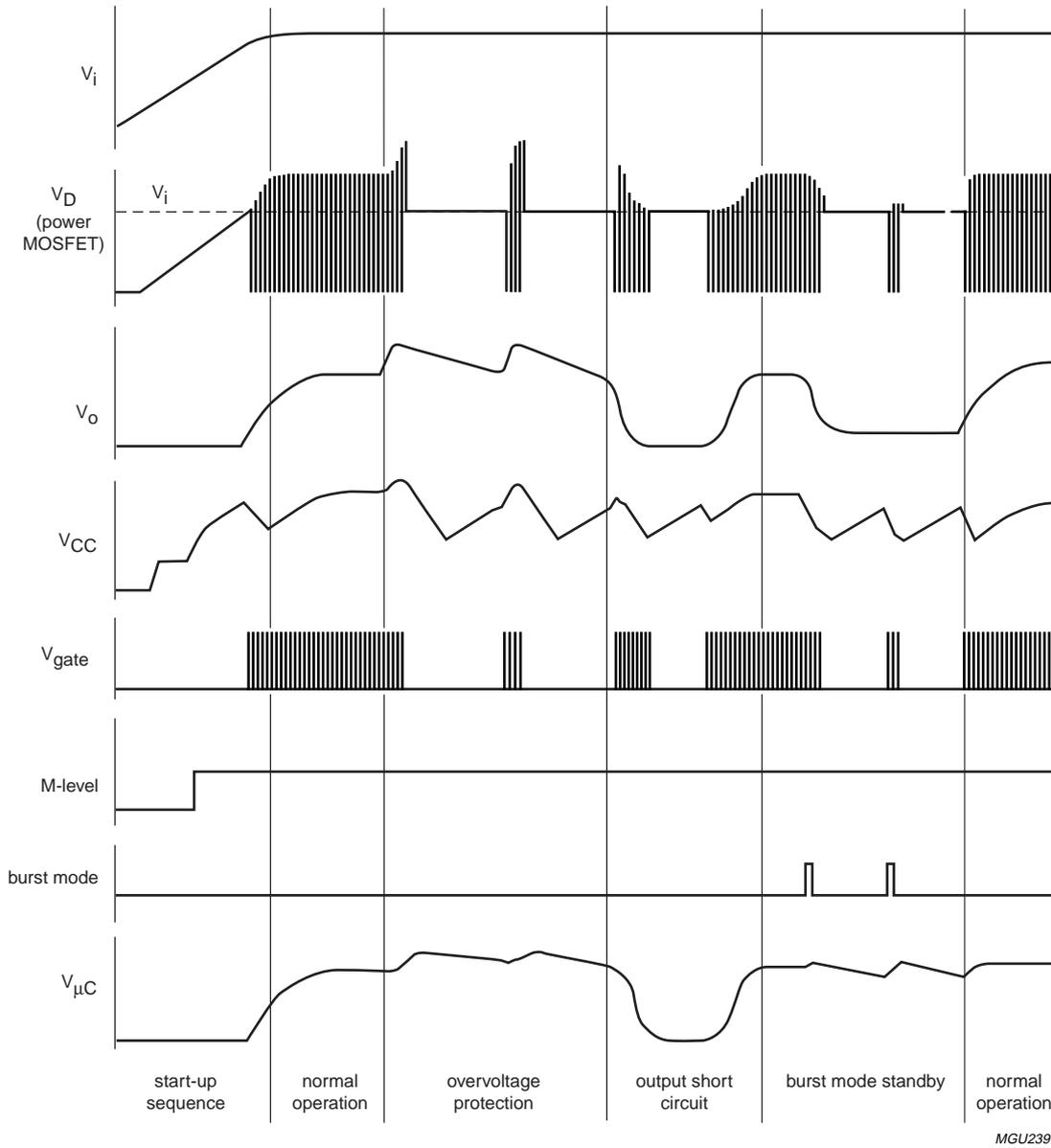


Fig.11 Typical waveforms.



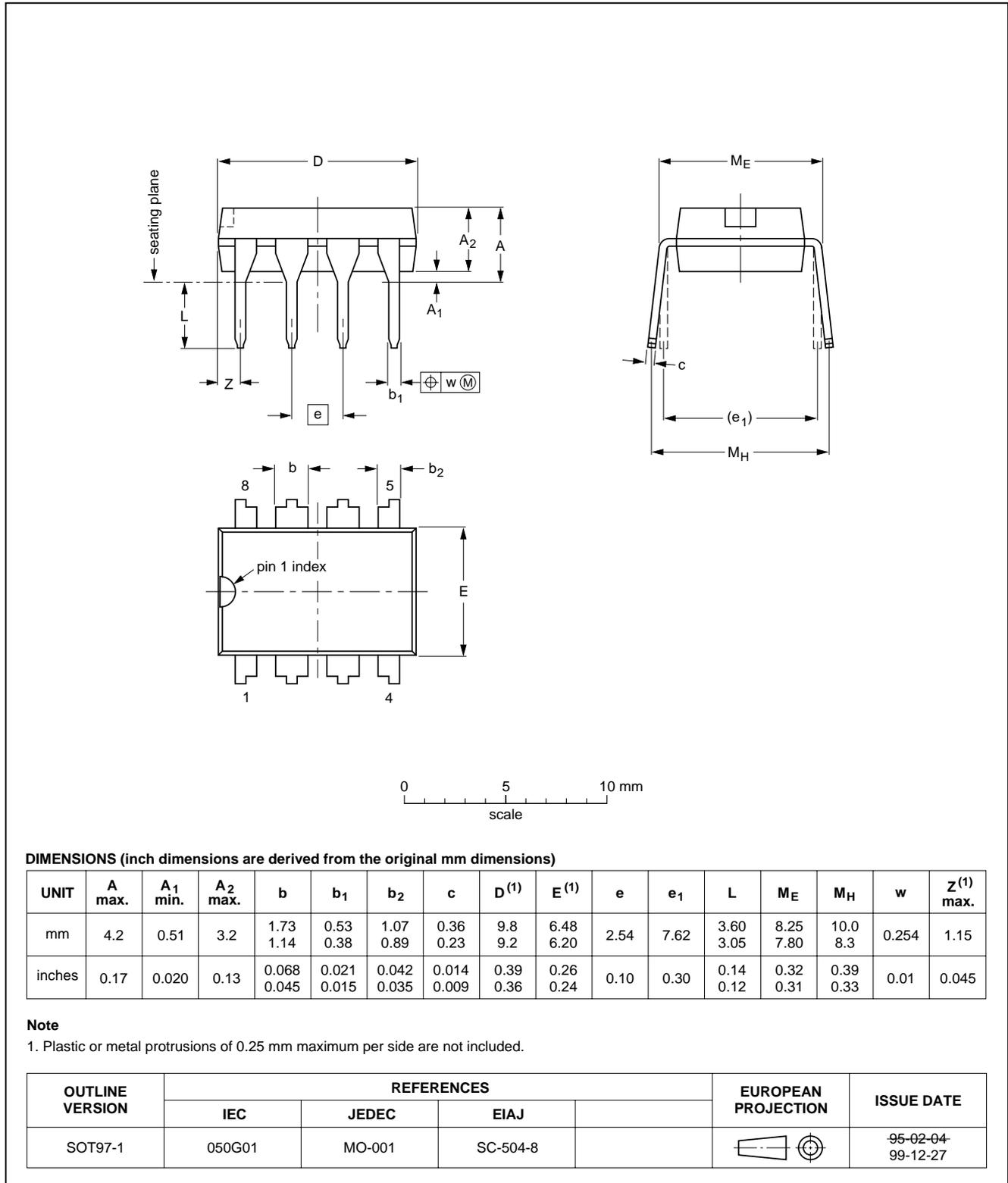
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PACKAGE OUTLINE

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT97-1	050G01	MO-001	SC-504-8		95-02-04 99-12-27

## GreenChip™II SMPS control IC

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**SOLDERING****Introduction to soldering through-hole mount packages**

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

**Soldering by dipping or by solder wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Manual soldering**

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**Suitability of through-hole mount IC packages for dipping and wave soldering methods**

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable <sup>(1)</sup>

**Note**

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

## GreenChip™II SMPS control IC

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## DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS <sup>(1)</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

## Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

## DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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